MC74LVXT4051

Product Preview

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVXT4051 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The LVXT4051 is similar in pinout to the LVX8051, HC4051A and the metal–gate MC14051B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The LVXT control inputs are compatible with TTL levels.

The control pin input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches, and High–Speed CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- TTL–Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal–Gate, HSL, or VHC Counterparts
- Low Noise
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Designed to Operate on a Single Supply with V_{EE} = GND, or Using Split Supplies up to ± 3.3 V

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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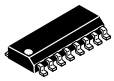
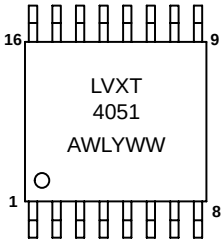
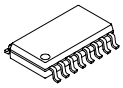
MARKING DIAGRAMS



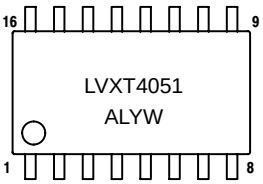
SOIC–16
D SUFFIX
CASE 751B

TSSOP–16
DT SUFFIX
CASE 948F





SOIC EIAJ–16
M SUFFIX
CASE 966

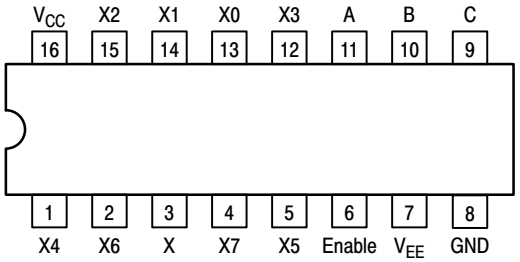


A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74LVXT4051D	SOIC–16	48 Units/Rail
MC74LVXT4051DR2	SOIC–16	2500 Units/Reel
MC74LVXT4051DT	TSSOP–16	96 Units/Rail
MC74LVXT4051DTR2	TSSOP–16	2500 Units/Reel
MC74LVXT4051M	SOIC EIAJ–16	48 Units/Rail
MC74LVXT4051MEL	SOIC EIAJ–16	2000 Units/Reel

PIN CONNECTION AND MARKING DIAGRAM (Top View)

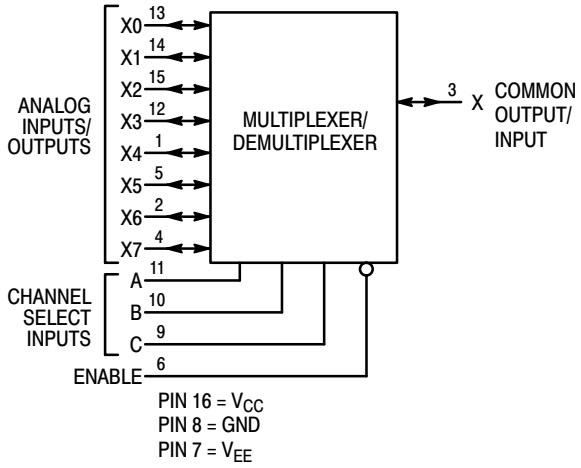


FUNCTION TABLE

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

LOGIC DIAGRAM
Single–Pole, 8–Position Plus Common Off



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

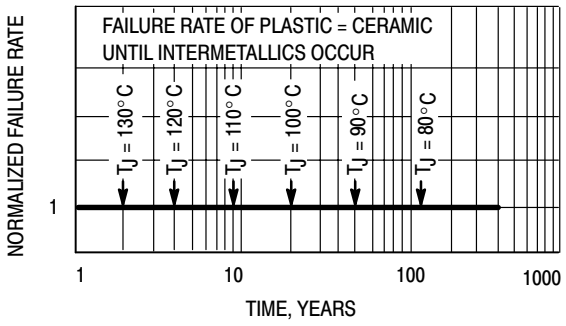
Symbol	Parameter	Min	Max	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	–6.0	GND	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	2.0 2.0	6.0 6.6	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	0	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0



Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	3.0 4.5 5.5	1.4 2.0 2.0	1.4 2.0 2.0	1.4 2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	3.0 4.5 5.5	0.53 0.80 0.80	0.53 0.80 0.80	0.53 0.80 0.80	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND,	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{in}= 0 V	5.5	4	40	160	μA
I_{CCT}	Quiescent Supply Current	Channel Select, Enable V_{IS} = V_{CC} or GND; V_{in}= 3.4 V	5.5	1.35	1.50	1.65	mA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to V_{EE} $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5 3.3	0 0 0 –3.3	20 10 7.0 4.0	25 15 10 10	30 20 15 15	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5 3.3	0 0 0 –3.3	20 10 7.0 4.0	25 15 10 10	30 20 15 15	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – V_{EE}) $\|I_S\|$ ≤ 10.0 mA	3.0 4.5 5.5 3.3	0 0 0 –3.3	5 1 1 1	5 1.2 1.2 1.2	5 1.5 1.5 1.5	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 3)	5.5 3.3	0 –3.3	1 1	10 10	1000 1000	nA
	Maximum Off–Channel Leakage Current, Common Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 4)	5.5 3.3	0 –3.3	1 1	10 10	1000 1000	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} or GND; (Figure 5)	5.5 3.3	0 –3.3	1 1	10 10	1000 1000	nA
t_{BBM}	Minimum Break–Before–Make Time§ (Figure 12)	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – V_{EE}) R_L = 300 Ω, C_L = 35 pF	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	1 0.2 0.2 0.2	TBD TBD TBD TBD	TBD TBD TBD TBD	ns

* Limits not tested. Determined by design and verified by qualification.

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	V_{EE} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0	0	30	35	40	ns
		3.0	0	20	25	30	
		4.5	0	15	18	22	
		5.5	0	15	18	20	
		3.3	–3.3	10	12	15	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	0	1.0	1.0	2.0	ns
		3.0	0	1.0	1.0	2.0	
		4.5	0	1.0	1.0	1.0	
		5.5	0	1.0	1.0	1.0	
		3.3	–3.3	1.0	1.0	1.0	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	0	30	35	40	ns
		3.0	0	20	25	30	
		4.5	0	15	18	22	
		5.5	0	15	18	20	
		3.3	–3.3	10	12	15	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	0	20	25	30	ns
		3.0	0	12	14	15	
		4.5	0	8.0	10	12	
		5.5	0	8.0	10	12	
		3.3	–3.3	5.0	8.0	10	
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs			10	10	10	pF
$C_{I/O}$	Maximum Capacitance (All Switches Off) Analog I/O			35	35	35	pF
	Common O/I			130	130	130	
	Feedthrough			1.0	1.0	1.0	

C_{PD}		**Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0V**	pF
	Power Dissipation Capacitance (Figure 17)*	45	

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	V_{IS} = ½ (V_{CC} – V_{EE}), Ref & Test Attn = 10 dB Source Amplitude = 0 dB	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	80 80 80 80	MHz
V_{ISO}	Off–Channel Feedthrough Isolation (Figure 7)	V_{IS} = ½ (V_{CC} – V_{EE}), Adjust Network Analyzer output to 10 dBm on each output from the power splitter	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	–93 –93 –93 –93	dB
V_{ISOC}	Common–Channel Feedthrough Isolation (Figure 8)	V_{IS} = ½ (V_{CC} – V_{EE}), Adjust Network Analyzer output to 10 dBm on each output from the power splitter	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	–93 –93 –93 –93	dB
V_{ONL}	Maximum Feedthrough On Loss (Figure 11)	V_{IS} = ½ (V_{CC} – V_{EE}), Adjust Network Analyzer output to 10 dBm on each output from the power splitter	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	–2 –2 –2 –2	dB
Q	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 9)	V_{IN} = V_{CC} to V_{EE}, f_{IS} = 1 MHz, t_r = t_f = 3 ns R_{IS} = 600 Ω, C_L= 50 pF	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	25 40 50 60	mV_{PP}
	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 9)	V_{IN} = V_{CC} to V_{EE}, f_{IS} = 1 MHz, t_r = t_f = 3 ns R_{IS} = 10 Ω, C_L= 10 pF	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	35 40 50 60	
Q	Feedthrough Noise.† Enable Input to Common I/O (Figure 10)	V_{IN} = V_{CC} to V_{EE}, f_{IS} = 1 MHz, t_r = t_f = 3 ns R_{IS} = 0 Ω, C_L= 1000 pF, Q = C_L * ΔV_{OUT}	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	TBD 3.0 3.0 TBD	pC
	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 9)	V_{IN} = V_{CC} to V_{EE}, f_{IS} = 1 MHz, t_r = t_f = 3 ns R_{IS} = 0 Ω, C_L= 1000 pF, Q = C_L * ΔV_{OUT}	3.0 4.5 5.5 3.3	0.0 0.0 0.0 –3.3	TBD TBD TBD TBD	
$V\Delta_{OUT}$	Maximum Shift in Output Voltage of Enabled Analog Channel due to injected Current on a Disabled Channel (Figure 16)	I_{IN}‡ ≤ 1 mA, R_S ≤ 3.9 KΩ I_{IN}‡ ≤ 10 mA, R_S ≤ 3.9 KΩ I_{IN}‡ ≤ 1 mA, R_S ≤ 20 KΩ I_{IN}‡ ≤ 10 mA, R_S ≤ 20 KΩ	5.0 5.0 5.0 5.0	0.0 0.0 0.0 0.0	TBD TBD TBD TBD	mV
THD	Total Harmonic Distortion THD = $THD_{MEASURED}$ – THD_{SOURCE} (Figure 18)	f_{IS} = 1 MHz, R_L = 10 KΩ, C_L = 50 pF, V_{IS} = 2.5 V_{PP} sine wave V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave V_{IS} = 6.0 V_{PP} sine wave	 3.0 4.5 5.5 3.3	 0.0 0.0 0.0 –3.3	 0.10 0.08 0.05 0.05	%

*Limits not tested. Determined by design and verified by qualification.
†Note: Some manufacturers may refer to this specification as Charge Injection.
‡Note: I_{IN} = Total current injected into all disabled channels.

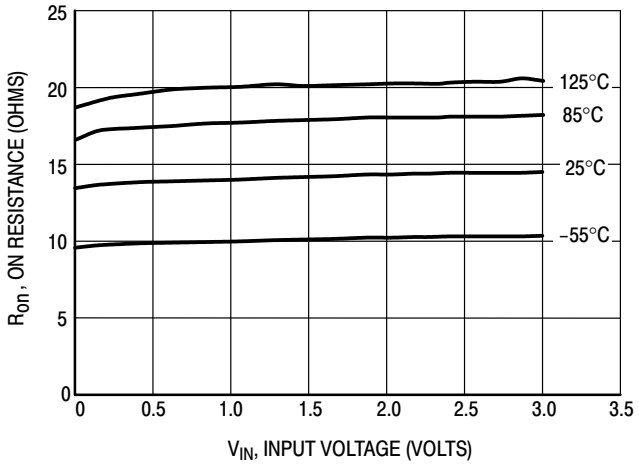


Figure 1a. Typical On Resistance, V_{CC} = 3.0 V, V_{EE} = 0V

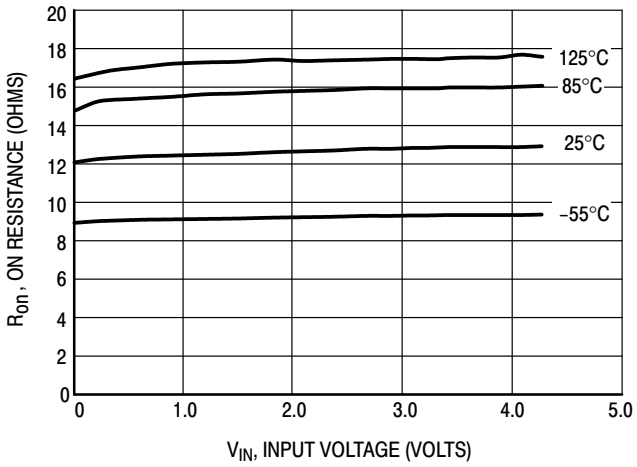


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V, V_{EE} = 0V

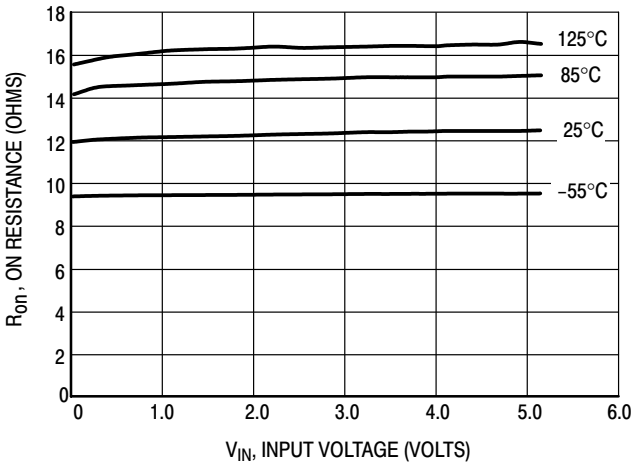


Figure 1c. Typical On Resistance, V_{CC} = 5.5 V, V_{EE} = 0V

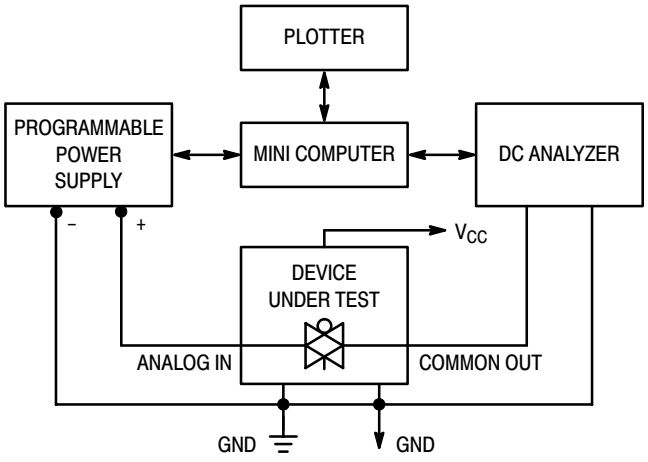


Figure 2. On Resistance Test Set–Up

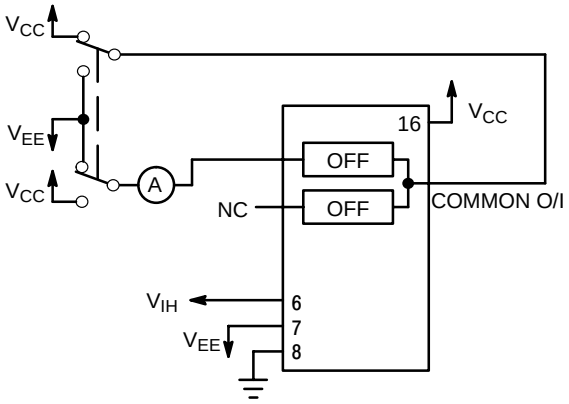


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

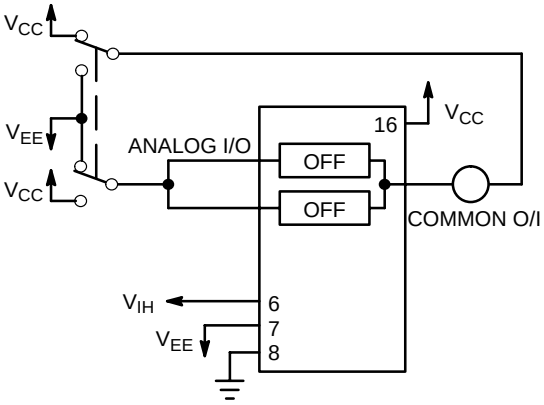


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

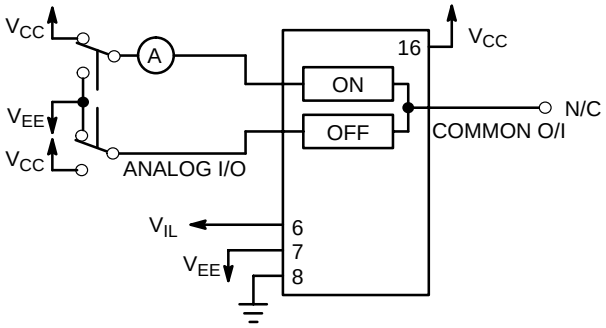


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

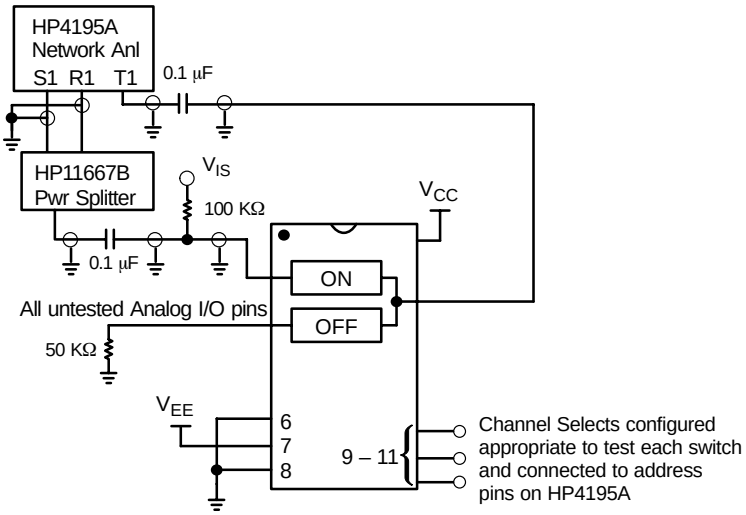
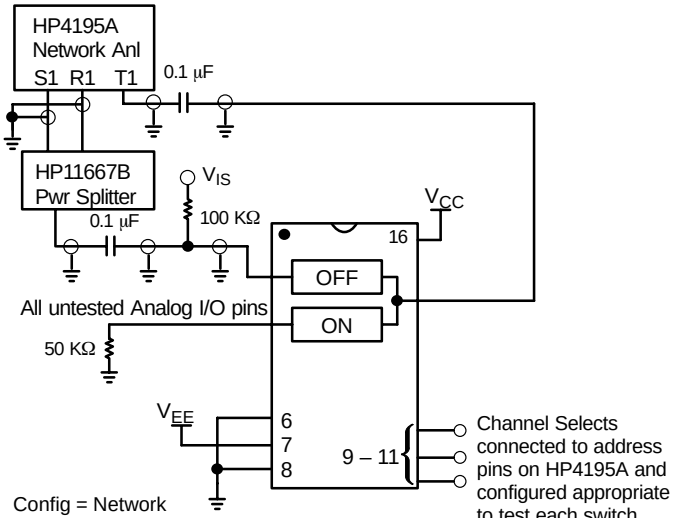


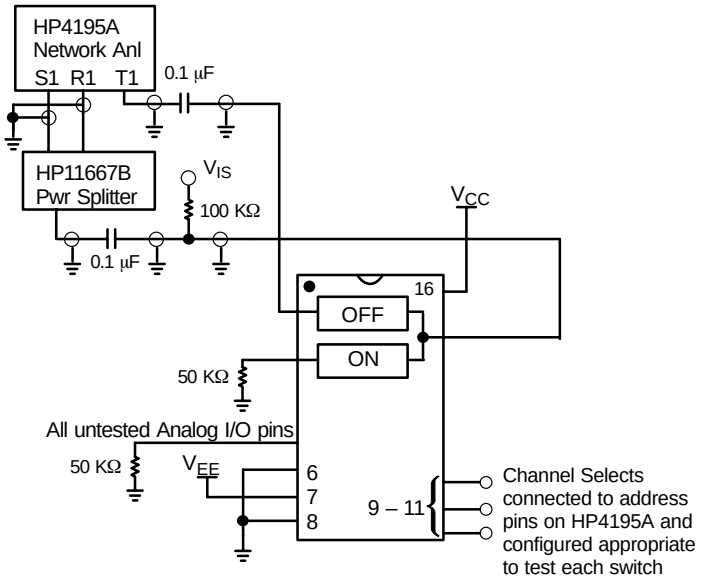
Figure 6. Maximum On Channel Bandwidth, Test Set–Up



Config = Network
Format = T/R (dB)
CAL = Trans Cal
Display = Rectan X–A+B
Scale Ref = Auto Scale
View = Off, Off, Off
Trig = Cont Mode
Source Amplitude = +13 dB
Reference Attenuation = 20 dB
Test Attenuation = 0 dB

$V_{ISO}(dB) = 20 \log (V_{T1}/V_{R1})$

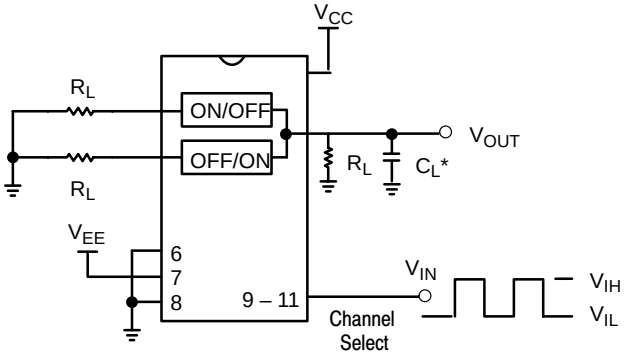
Figure 7. Maximum Off Channel Feedthrough Isolation,Test Set–Up



Config = Network
Format = T/R (dB)
CAL = Trans Cal
Display = Rectan X–A+B
Scale Ref = Auto Scale
View = Off, Off, Off
Trig = Cont Mode
Source Amplitude = +13 dB
Reference Attenuation = 20 dB
Test Attenuation = 0 dB

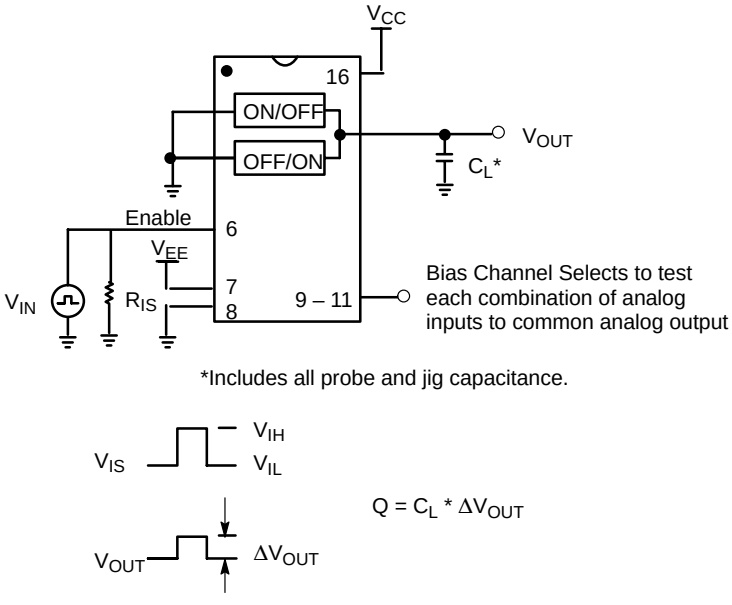
$V_{ISOC}(dB) = 20 \log (V_{T1}/V_{R1})$

Figure 8. Maximum Common–Channel Feedthrough Isolation Test Set–Up



*Includes all probe and jig capacitance.

Figure 9. Feedthrough Noise, Channel Select to Common Out, Test Set–Up



*Includes all probe and jig capacitance.

Figure 10. Feedthrough Noise, Enable to Common Out, Test Set–Up

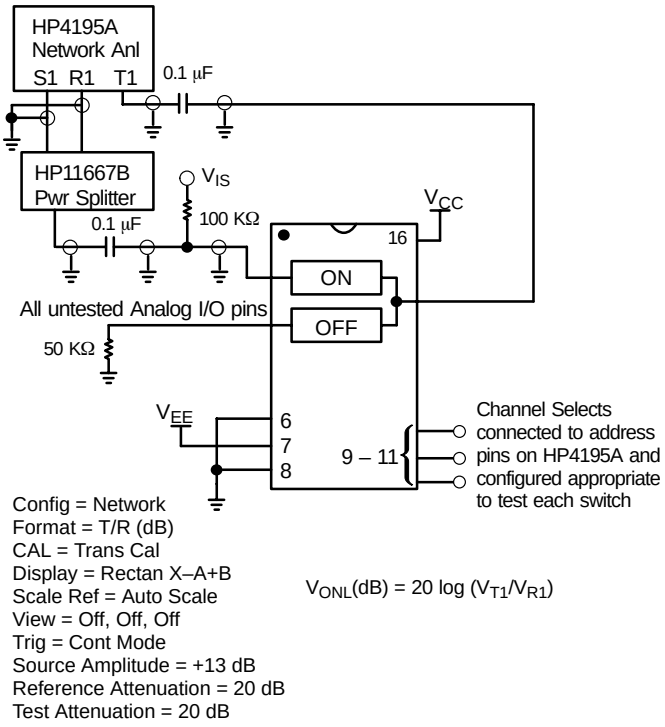


Figure 11. Maximum On Channel Feedthrough On Loss Test Set–Up

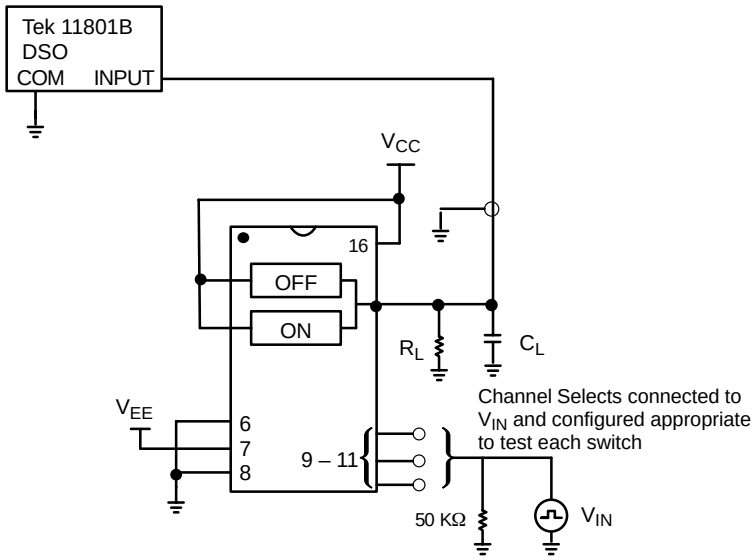


Figure 12a. Break–Before–Make Test Set–Up

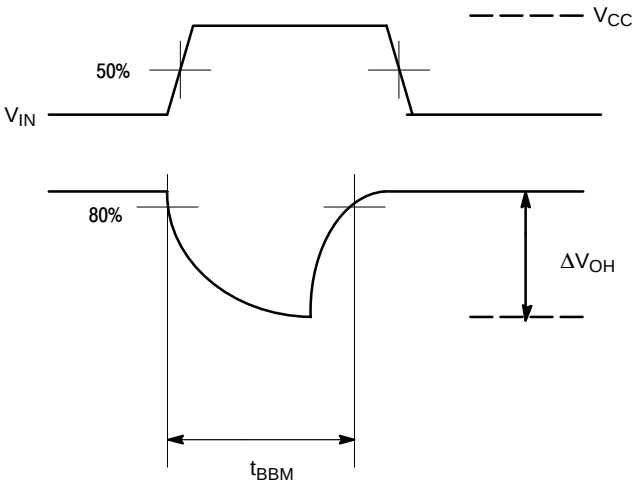


Figure 12b. Break–Before–Make Time

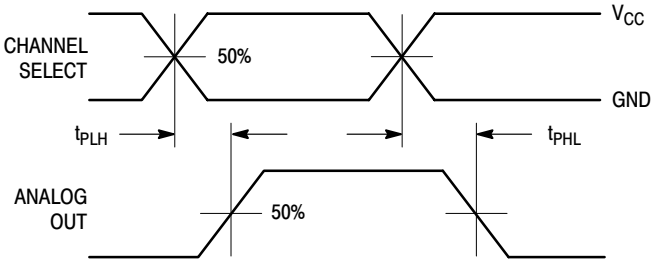
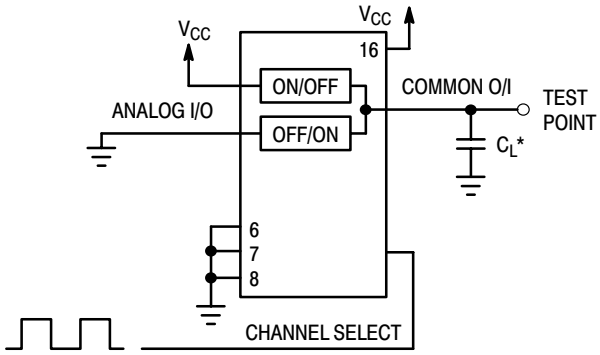


Figure 13a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 13b. Propagation Delay, Test Set–Up Channel Select to Analog Out

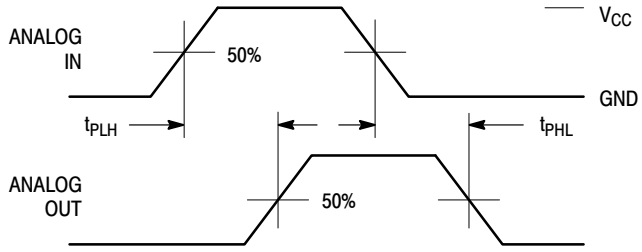
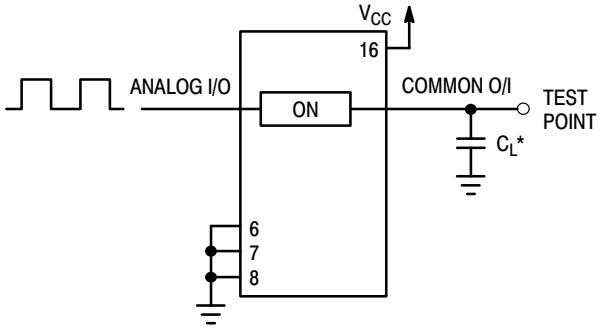


Figure 14a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 14b. Propagation Delay, Test Set–Up Analog In to Analog Out

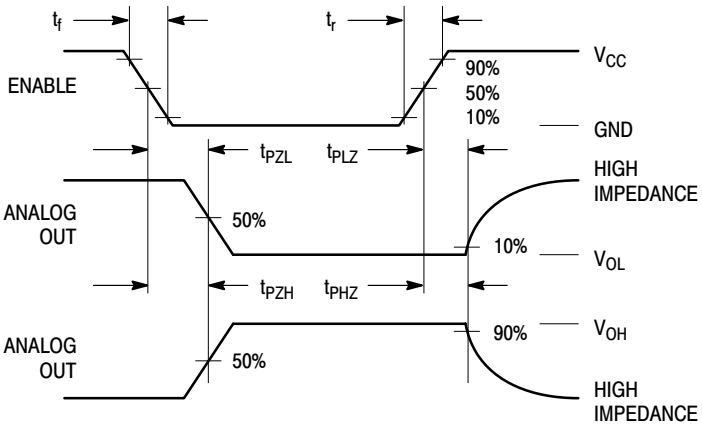


Figure 15a. Propagation Delays, Enable to Analog Out

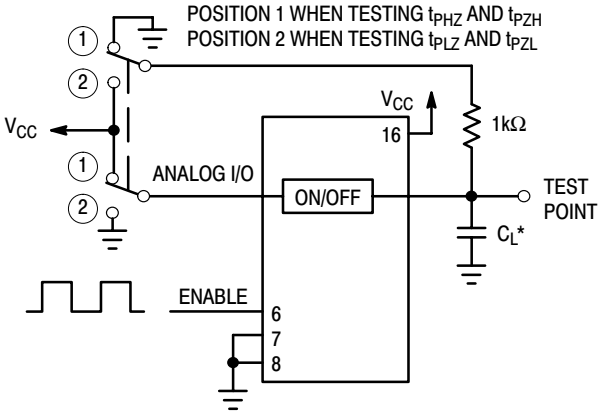


Figure 15b. Propagation Delay, Test Set–Up Enable to Analog Out

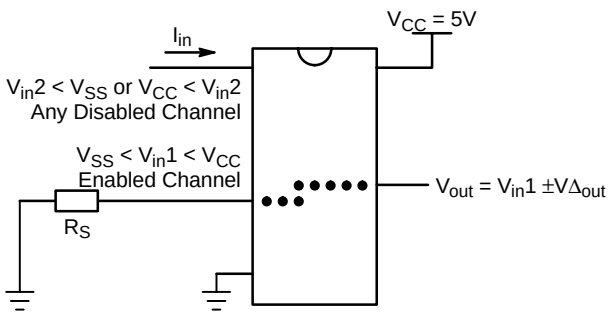


Figure 16. Maximum Shift in Output Voltage of Enabled Analog Channel due to Injected Current on a Disabled Channel Test Set–Up

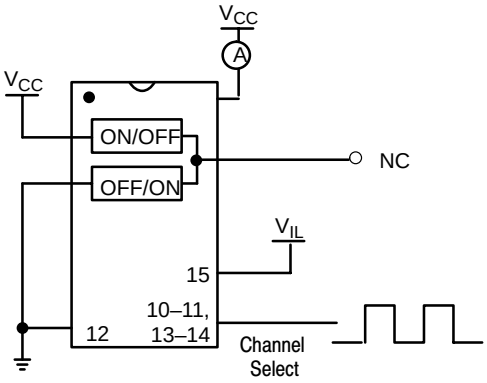


Figure 17. Power Dissipation Capacitance, Test Set–Up

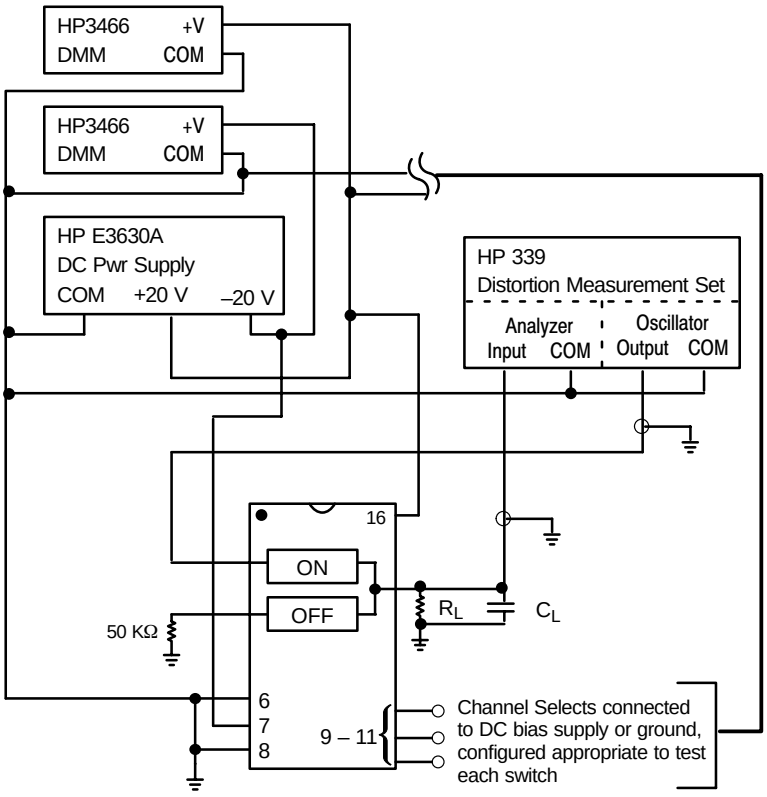


Figure 18a. Total Harmonic Distortion Test Set–Up

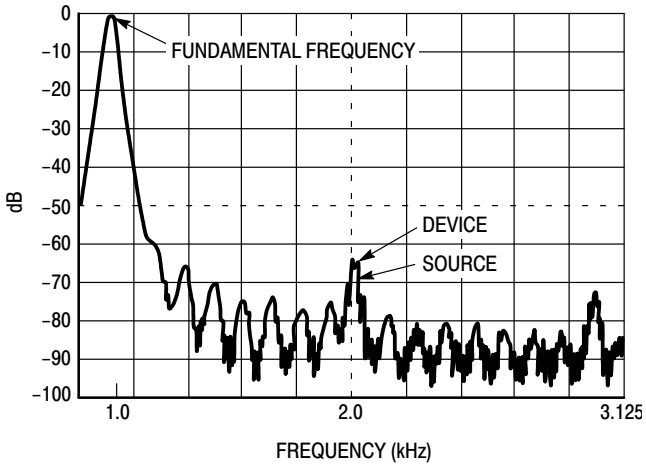


Figure 18b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swing is determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{EE} – GND = 0 to –6 volts
V_{CC} – GND = 2 to 6 volts
V_{CC} – V_{EE} = 2 to 6 volts
and $V_{EE} \leq$ GND

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

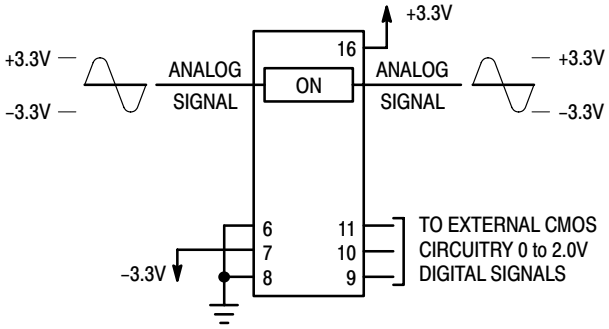


Figure 19a. Application Example

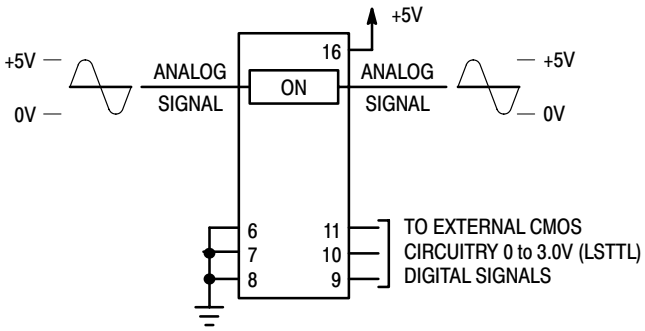


Figure 19b. Application Example

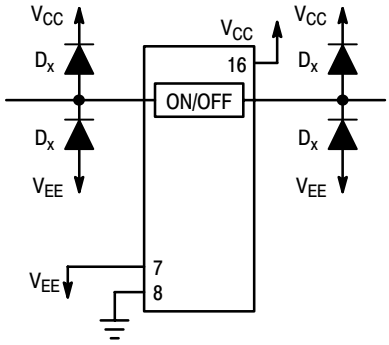


Figure 20. External Germanium or Schottky Clipping Diodes

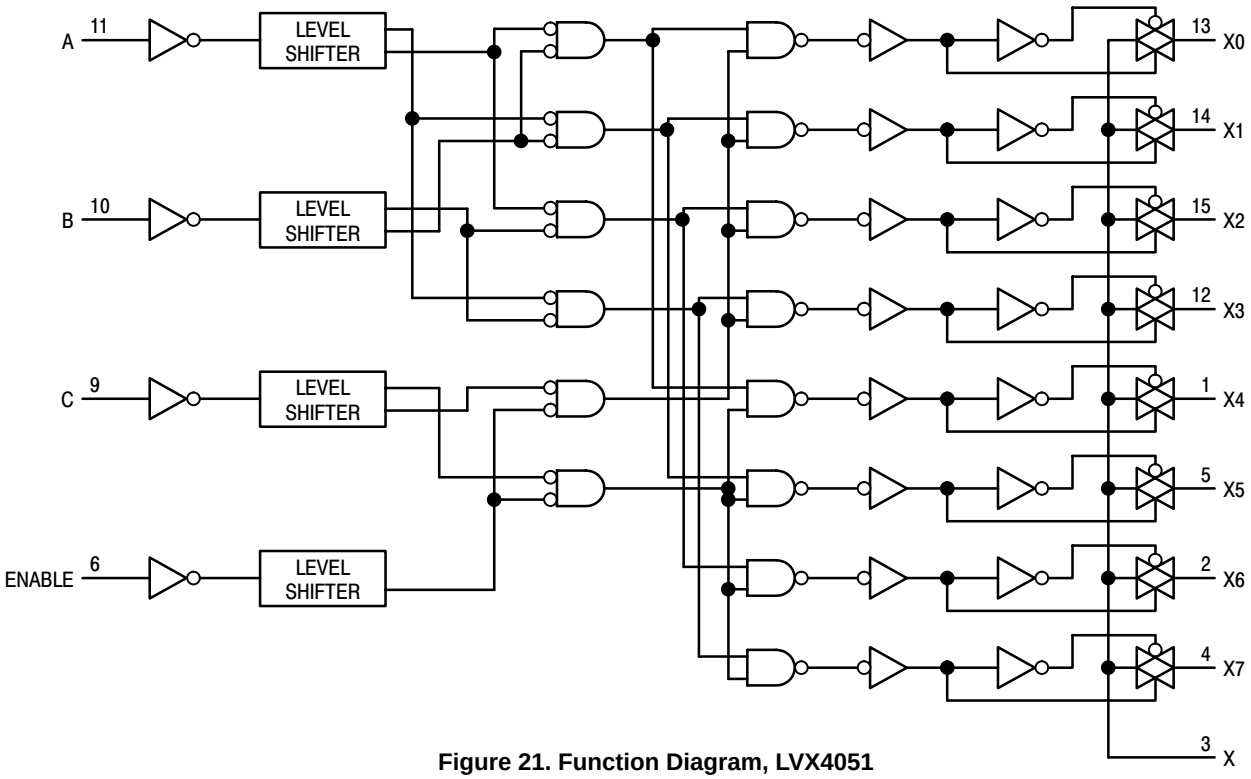
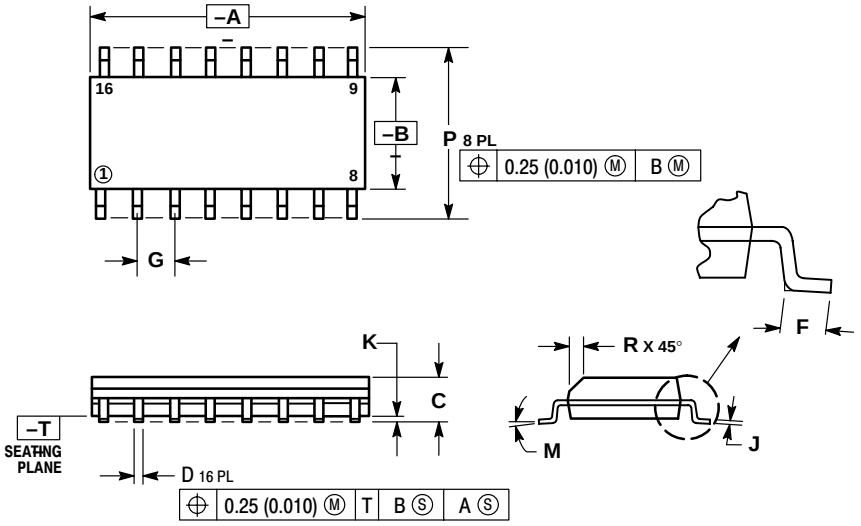


Figure 21. Function Diagram, LVX4051

PACKAGE DIMENSIONS

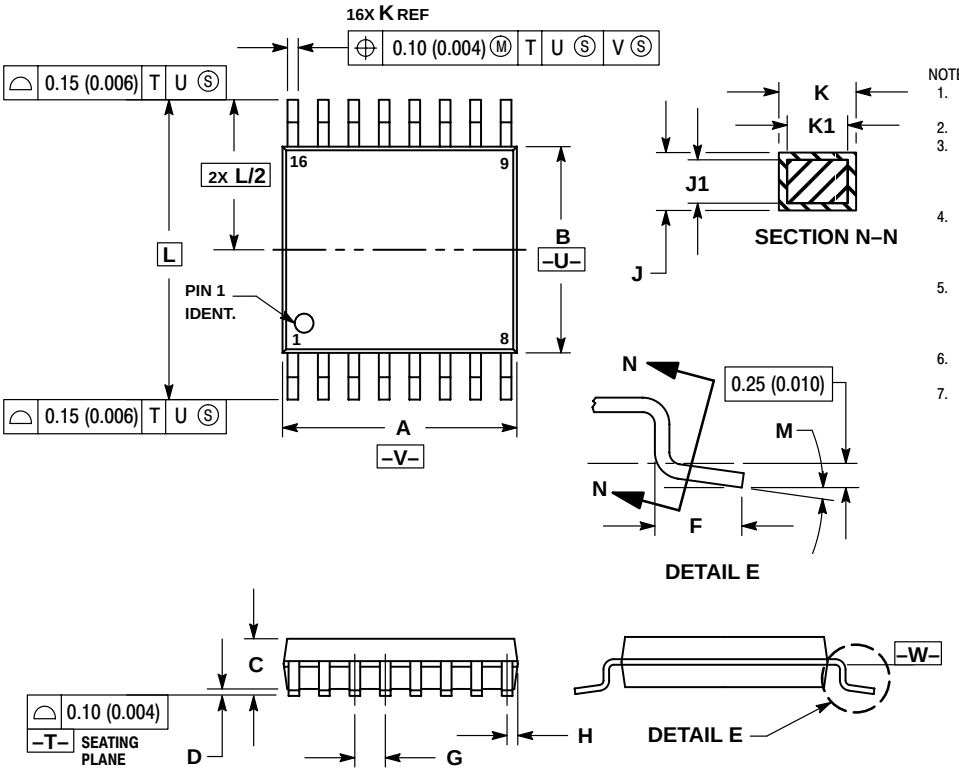
SOIC–16
D SUFFIX
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP–16
DT SUFFIX
CASE 948F–01
ISSUE O

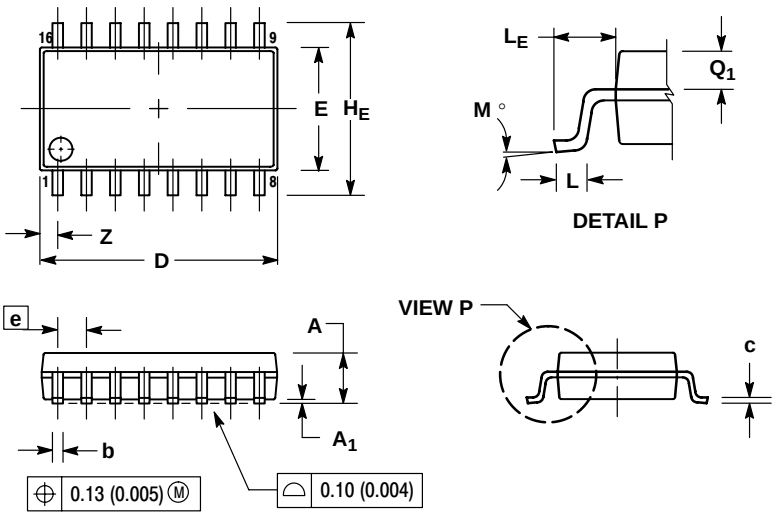


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

PACKAGE DIMENSIONS

SOIC EIAJ–16
M SUFFIX
CASE 966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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