

MC74LVX50

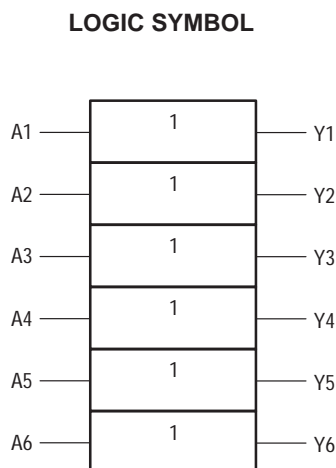
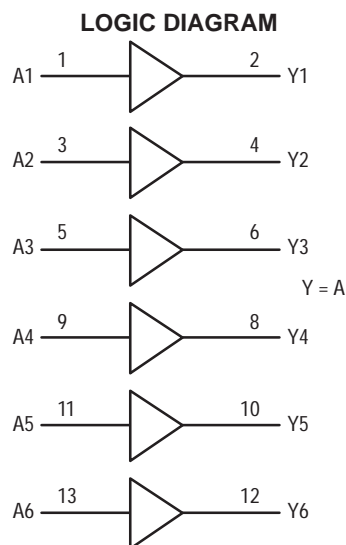
Product Preview

Hex Buffer

The MC74LVX50 is an advanced high speed CMOS buffer fabricated with silicon gate CMOS technology.

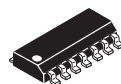
The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 5.0\text{ns}$ (Typ) at $V_{CC} = 3.3\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Low Noise: $V_{OLP} = 0.5\text{V}$ (Max)
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

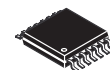


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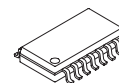
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**14-LEAD SOIC
D SUFFIX
CASE 751A**

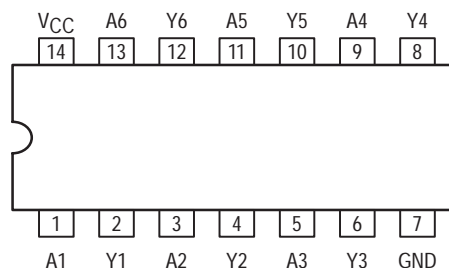


**14-LEAD TSSOP
DT SUFFIX
CASE 948G**



**14-LEAD SOIC EIAJ
M SUFFIX
CASE 965**

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX50D	SOIC	55 Units/Rail
MC74LVX50DT	TSSOP	96 Units/Rail
MC74LVX50M	SOIC EIAJ	50 Units/Rail

FUNCTION TABLE

A Input	Y Output
L	L
H	H

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MC74LVX50

MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN}	-0.5 to +7.0	V
DC Output Voltage $V_{CC} = 0$ High or Low State	V_{OUT}	-0.5 to 7.0 -0.5 to $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current ($V_{OUT} < GND$; $V_{OUT} > V_{CC}$)	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	P_D	500 450	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.0	3.6	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range	T_A	-55	+85	°C
Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$	t_r, t_f	0	100	ns/V

MC74LVX50

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 3.6	1.5 2.1 2.4			1.5 2.1 2.4		1.5 2.1 2.4		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.9 0.8		0.5 0.9 0.8		0.5 0.9 0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA I _{OH} = -50μA I _{OH} = -4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 4.5		1.9 2.9 2.48		1.9 2.9 2.34		V
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA I _{OL} = 50μA I _{OL} = 4mA	2.0 3.0 3.0		0.0 0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44		0.1 0.1 0.52	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Y	V _{CC} = 2.7V C _L = 15 pF C _L = 50 pF V _{CC} = 3.3 ± 0.3V C _L = 15 pF C _L = 50 pF		6.0 8.0	7.0 9.5		9.0 12.5		11.0 15.0	ns
C _{IN}	Maximum Input Capacitance			4	10		10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C, V _{CC} = 5.0V	pF
		18	

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.3	0.5	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.3	-0.5	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

MC74LVX50

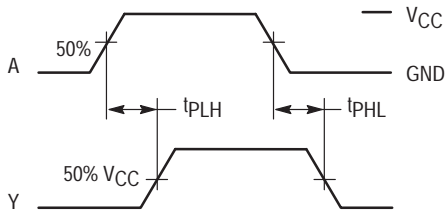
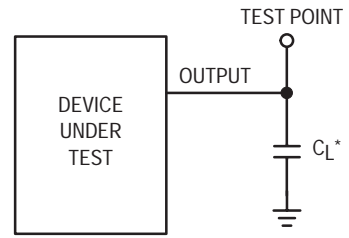


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

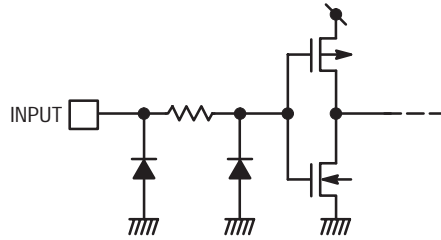
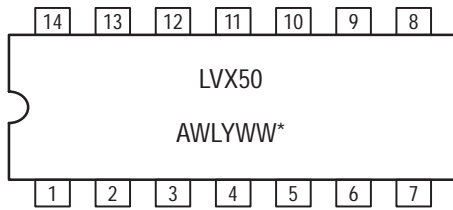
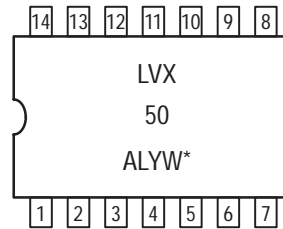


Figure 3. Input Equivalent Circuit

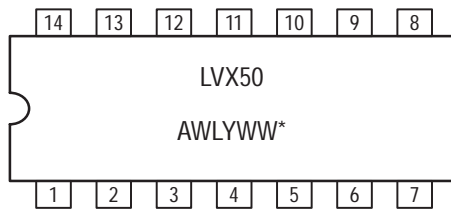
MARKING DIAGRAMS (Top View)



14-LEAD SOIC
D SUFFIX
CASE 751A



14-LEAD TSSOP
DT SUFFIX
CASE 948G



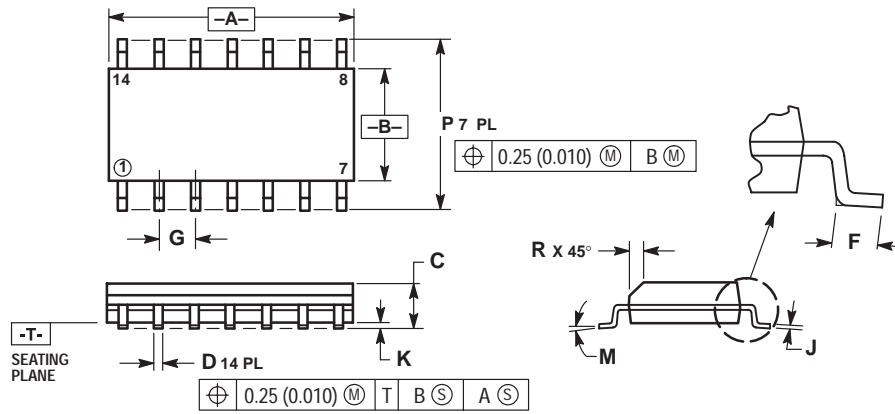
14-LEAD SOIC EIAJ
M SUFFIX
CASE 965

*See Applications Note #AND8004/D for date code and traceability information.

MC74LVX50

PACKAGE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



NOTES:

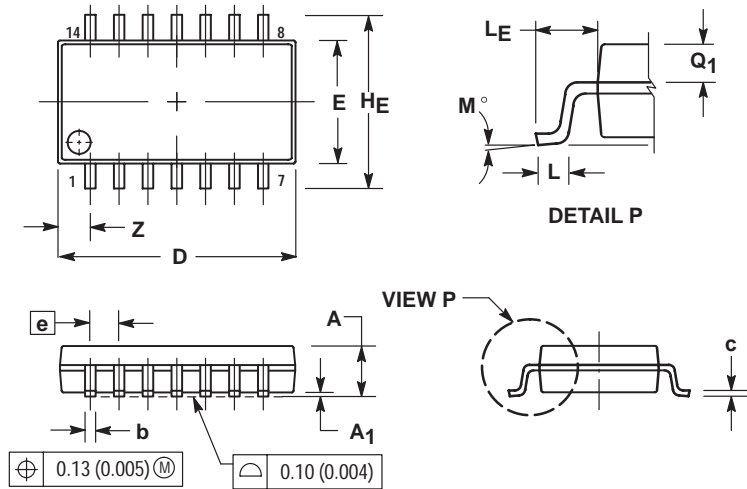
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

MC74LVX50

PACKAGE DIMENSIONS


M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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