Dual Supply Octal Translating Transceiver
with 3-State Outputs

The 74LVX4245 is a 24–pin dual–supply, octal translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment such as laptop computers using a 3.3V CPU and 5V LCD display. The A port interfaces with the 5V bus; the B port interfaces with the 3V bus.

The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow. Transmit (active–High) enables data from the A port to the B port. Receive (active–Low) enables data from the B port to the A port. The Output Enable ($\overline{OE}$) input, when High, disables both A and B ports by placing them in 3–State.

- Bi–directional Interface Between 5V and 3V Buses
- Control Inputs Compatible with TTL Level
- 5V Data Flow at A Port and 3V Data Flow at B Port
- Outputs Source/Sink 24mA at 5V Bus and 12mA at 3V Bus
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Available in SOIC and TSSOP Packages
- Functionally Compatible with the 74 Series 245

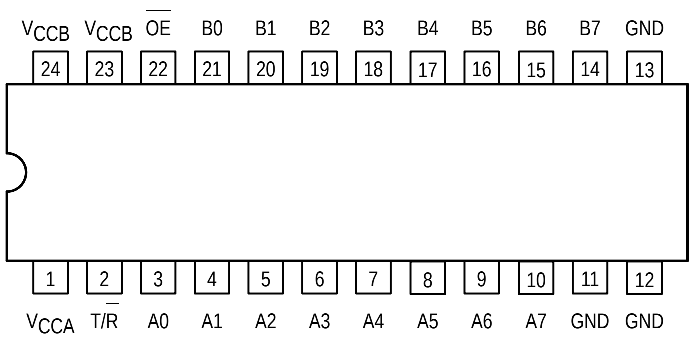
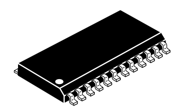


Figure 1. 24–Lead Pinout
(Top View)

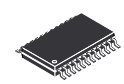
MC74LVX4245

LVX

LOW–VOLTAGE CMOS



DW SUFFIX
24–LEAD PLASTIC SOIC PACKAGE
CASE 751E–04



DT SUFFIX
24–LEAD PLASTIC TSSOP PACKAGE
CASE 948H–01

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

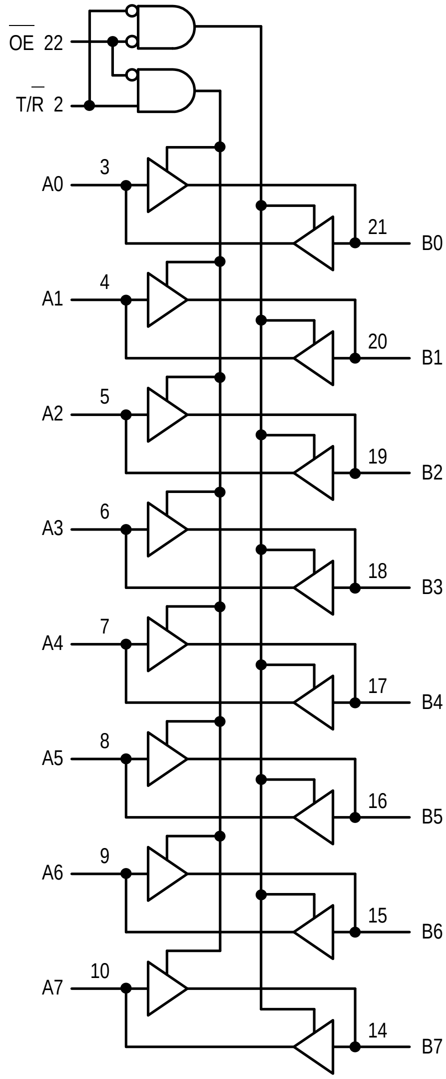


Figure 2. Logic Diagram

INPUTS		OPERATING MODE Non–Inverting
$\overline{OE}$	$T/\overline{R}$	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		–0.5 to +7.0		V
V_I	DC Input Voltage	$\overline{OE}$, $T/\overline{R}$	–0.5 to V_{CCA} +0.5		V
$V_{I/O}$	DC Input/Output Voltage	An	–0.5 to V_{CCA} +0.5		V
		Bn	–0.5 to V_{CCB} +0.5		V
I_{IK}	DC Input Diode Current	$\overline{OE}$, $T/\overline{R}$	±20	V_I < GND	mA
I_{OK}	DC Output Diode Current		±50	V_O < GND; V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}, I_{GND}	DC Supply Current	Per Output Pin Maximum Current at I_{CCA} Maximum Current at I_{CCB}	±50 ±200 ±100		mA
T_{STG}	Storage Temperature Range		–65 to +150		°C
Latchup	DC Latchup Source/Sink Current		±300		mA

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Supply Voltage	V_{CCA} V_{CCB}	4.5 2.7	5.5 3.6	V
V_I	Input Voltage	$\overline{OE}$, $T/\overline{R}$	0	V_{CCA}	V
$V_{I/O}$	Input/Output Voltage	An Bn	0 0	V_{CCA} V_{CCB}	V
T_A	Operating Free–Air Temperature		–40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate V_{IN} from 30% to 70% of V_{CC}; V_{CC} at 3.0V, 4.5V, 5.5V		0	8	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = –40 to +85°C Guaranteed Limits	Unit
V_{IHA}	Minimum HIGH Level Input Voltage	An,$\overline{OE}$ $T/\overline{R}$	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$	5.5 4.5	3.3 3.3		2.0 2.0	2.0 2.0	V
V_{IHB}		Bn		5.0 5.0	3.6 2.7		2.0 2.0	2.0 2.0	V
V_{ILA}	Maximum LOW Level Input Voltage	An,$\overline{OE}$ $T/\overline{R}$	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$	5.5 4.5	3.3 3.3		0.8 0.8	0.8 0.8	V
V_{ILB}		Bn		5.0 5.0	2.7 3.6		0.8 0.8	0.8 0.8	V
V_{OHA}	Minimum HIGH Level Output Voltage		I_{OUT} = –100µA I_{OH} = –24mA	4.5 4.5	3.0 3.0	4.50 4.25	4.40 3.86	4.40 3.76	V
V_{OHB}			I_{OUT} = –100µA I_{OH} = –12mA I_{OH} = –8mA	4.5 4.5 4.5	3.0 3.0 2.7	2.99 2.80 2.50	2.9 2.4 2.4	2.9 2.4 2.4	V
V_{OLA}	Maximum LOW Level Output Voltage		I_{OUT} = 100µA I_{OL} = 24mA	4.5 4.5	3.0 3.0	0.002 0.18	0.10 0.36	0.10 0.44	V
V_{OLB}			I_{OUT} = 100µA I_{OL} = 12mA I_{OL} = 8mA	4.5 4.5 4.5	3.0 3.0 2.7	0.002 0.1 0.1	0.10 0.31 0.31	0.10 0.40 0.40	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	$T_A = -40$ to $+85°C$ Guaranteed Limits	Unit
I_{IN}	Max Input Leakage Current	$\overline{OE}$, T/R	$V_I = V_{CCA}$, GND	5.5	3.6		±0.1	±1.0	µA
I_{OZA}	Max 3–State Output Leakage	An	$V_I = V_{IH}$, V_{IL} $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND	5.5	3.6		±0.5	±5.0	µA
I_{OZB}	Max 3–State Output Leakage	Bn	$V_I = V_{IH}$, V_{IL} $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND	5.5	3.6		±0.5	±5.0	µA
ΔI_{CC}	Maximum I_{CCT} per Input	An,$\overline{OE}$ T/R	$V_I = V_{CCA}-2.1V$	5.5	3.6	1.0	1.35	1.5	mA
		Bn	$V_I = V_{CCB}-0.6V$	5.5	3.6		0.35	0.5	mA
I_{CCA}	Quiescent V_{CCA} Supply Current		An=V_{CCA} or GND Bn=V_{CCB} or GND $\overline{OE}$=GND T/R=GND	5.5	3.6		8	80	µA
I_{CCB}	Quiescent V_{CCB} Supply Current		An=V_{CCA} or GND Bn=V_{CCB} or GND $\overline{OE}$=GND T/R=V_{CCA}	5.5	3.6		5	50	µA
V_{OLPA} V_{OLPB}	Quiet Output Max Dynamic V_{OL}		Notes 1., 2.	5.0 5.0	3.3 3.3		1.5 1.2		V
V_{OLVA} V_{OLVB}	Quiet Output Min Dynamic V_{OL}		Notes 1., 2.	5.0 5.0	3.3 3.3		–1.2 –0.8		V
V_{IHDA} V_{IHDB}	Min HIGH Level Dynamic Input Voltage		Notes 1., 3.	5.0 5.0	3.3 3.3		2.0 2.0		V
V_{ILDA} V_{ILDB}	Max LOW Level Dynamic Input Voltage		Notes 1., 3.	5.0 5.0	3.3 3.3		0.8 0.8		V

1. Worst case package.
2. Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.
3. Max number of data inputs (n) switching. (n–1) inputs switching 0V to V_{CC} level. Input under test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1MHz.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CCA} = 5.0V$; $V_{CCB} = 3.3V$	4.5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CCA} = 5.0V$; $V_{CCB} = 3.3V$	15	pF
C_{PD}	Power Dissipation Capacitance (Measured at 10MHz) B→A A→B	$V_{CCA} = 5.0V$ $V_{CCB} = 3.3V$	55 40	pF

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = –40 to +85°C C_L = 50pF V_{CCA} = 5V ±0.5V V_{CCB} = 3.3V ±0.3V Min	Typ (Note 4.)	Max	T_A = –40 to +85°C C_L = 50pF V_{CCA} = 5V ±0.5V V_{CCB} = 2.7V Min	Max	Unit
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	5.1 5.3	9.0 9.0	1.0 1.0	10.0 10.0	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	5.4 5.5	9.0 9.0	1.0 1.0	10.0 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	6.5 6.7	10.5 10.5	1.0 1.0	11.5 11.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	5.2 5.8	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	6.0 3.3	10.0 7.0	1.0 1.0	10.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0 1.0	3.9 2.9	7.5 7.0	1.0 1.0	7.5 7.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew, Data to Output (Note 5.)		1.0	1.5		1.5	ns

4. Typical values at V_{CCA} = 5.0V; V_{CCB} = 3.3V at 25°C.
5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

Dual Supply Octal Translating Transceiver

The 74LVX4245 is a is a dual–supply device well capable of bidirectional signal voltage translation. This level shifting ability provides an excellent interface between low voltage CPU local bus and a standard 5V I/O bus. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

The LVX4245 is ideal for mixed voltage applications such as notebook computers using a 3.3V CPU and 5V peripheral devices.

Applications:
Mixed Mode Dual Supply Interface Solutions

The LVX4245 is designed to solve 3V/5V interfaces when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of a 3V device is driven by a 5V device, the P–Channel transistor in the 3V device will conduct — causing current flow from the I/O bus to the 3V power supply. The result may be destruction of the 3V device through latchup effects. A current limiting resistor may be used to prevent destruction, but it causes speed degradation and needless power dissipation.

A better solution is provided in the LVX4245. It provides two different output levels that easily handle the dual voltage interface. The A port is a dedicated 5V port; the B port is a dedicated 3V port. Figure 4 on page 6 shows how the LVX4245 may fit into a mixed 3V/5V system.

Since the LVX4245 is a ‘245 transceiver, the user may either use it for bidirectional or unidirectional applications. The center 20 pins are configured to match a ‘245 pinout. This enables the user to easily replace this level shifter with a 3V ‘245 device without additional layout work or re–manufacture of the circuit board (when both buses are 3V).

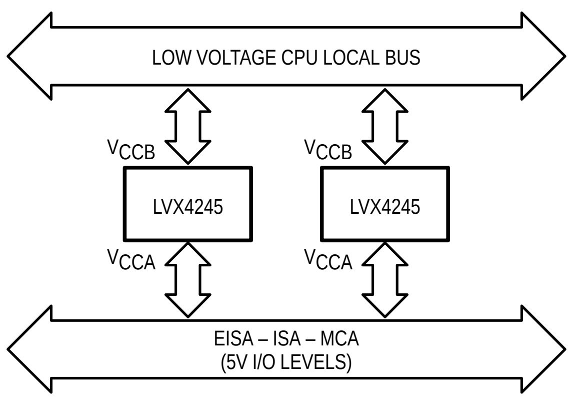


Figure 3. 3.3V/5V Interface Block Diagram

Powering Up the LVX4245

When powering up the LVX4245, please note that if the V_{CCB} pin is powered–up well in advance of the V_{CCA} pin, several milliamps of either I_{CCA} or I_{CCB} current will result. If the V_{CCA} pin is powered–up in advance of the V_{CCB} pin then only nanoamps of Icc current will result. In actuality the V_{CCB} can be powered “slightly” before the V_{CCA} without the current penalty, but this “setup time” is dependent on the power–up ramp rate of the V_{CC} pins. With a ramp rate of approximately 50mV/ns (50V/µs) a 25ns setup time was observed (V_{CCB}

before V_{CCA}). With a 7V/µs rate, the setup time was about 140ns. When all is said and done, the safest power–up strategy is to simply power V_{CCA} before V_{CCB}. One more note: if the V_{CCB} ramp rate is faster than the V_{CCA} ramp rate then power problems might still occur, even if the V_{CCA} power–up began prior to the V_{CCB} power–up.

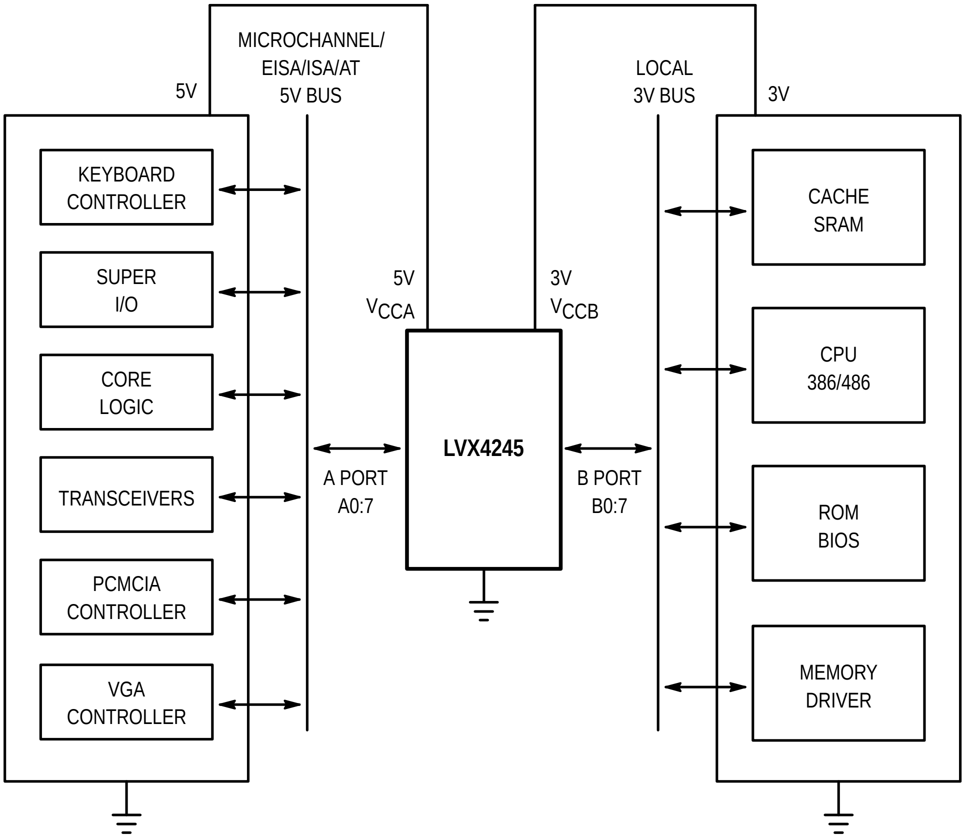


Figure 4. MC74LVX4245 Fits Into a System with 3V Subsystem and 5V Subsystem

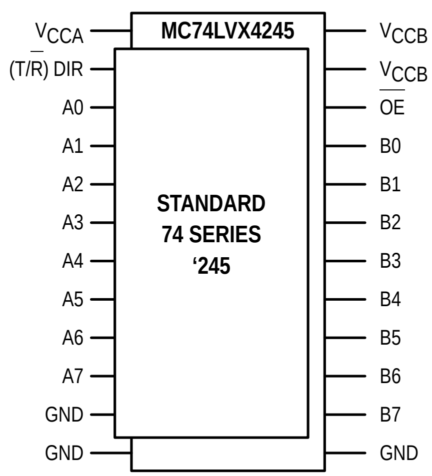
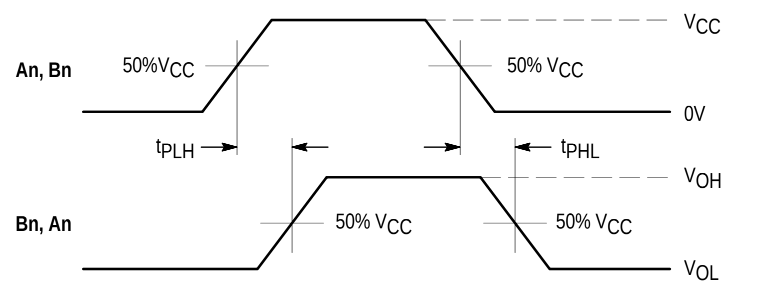
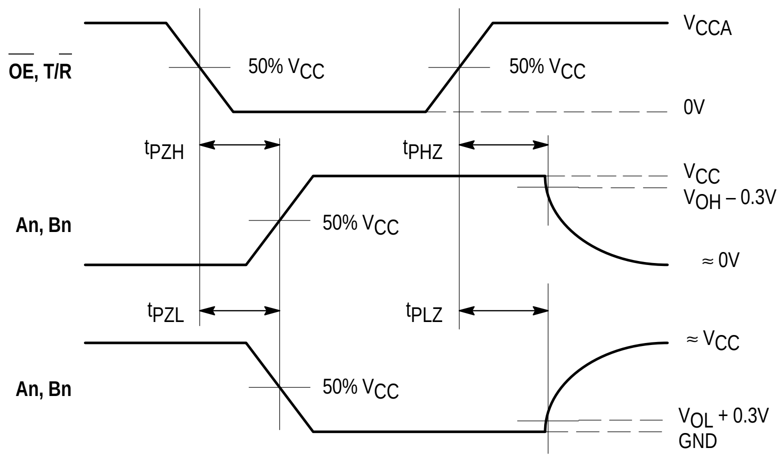


Figure 5. MC74LVX4245 Pin Arrangement Is Compatible to 20–Pin 74 Series ‘245s

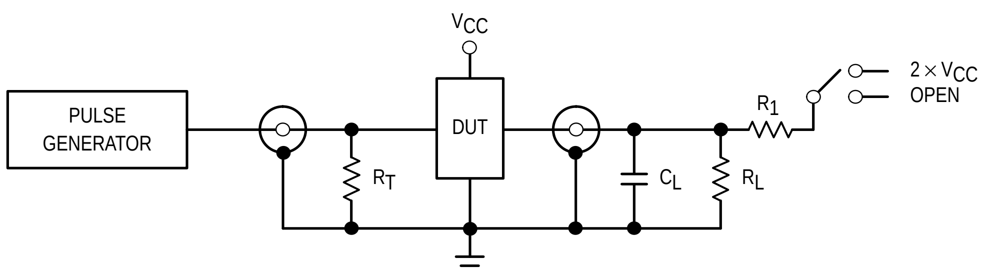


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 6. AC Waveforms



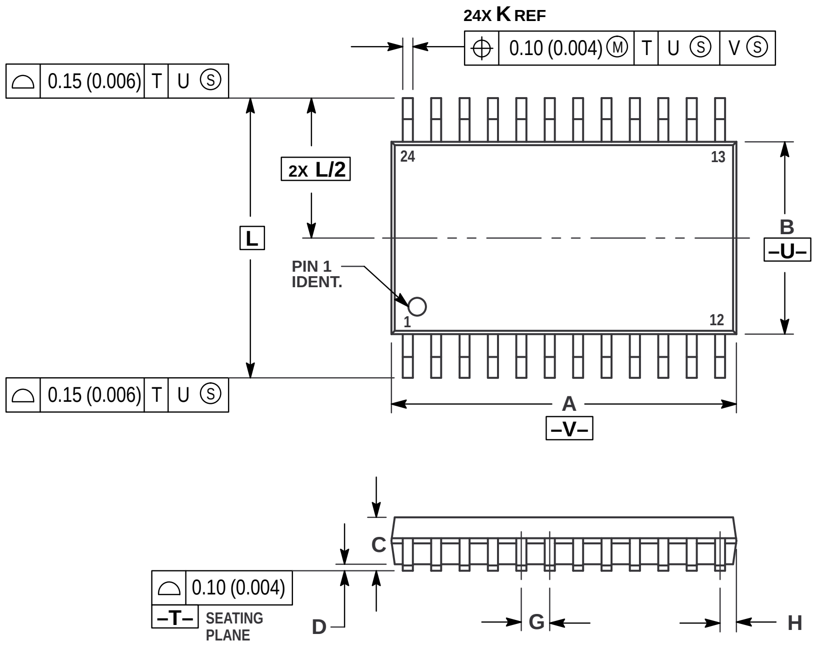
TEST	SWITCH
t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	$2 \times V_{CC}$

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7. Test Circuit

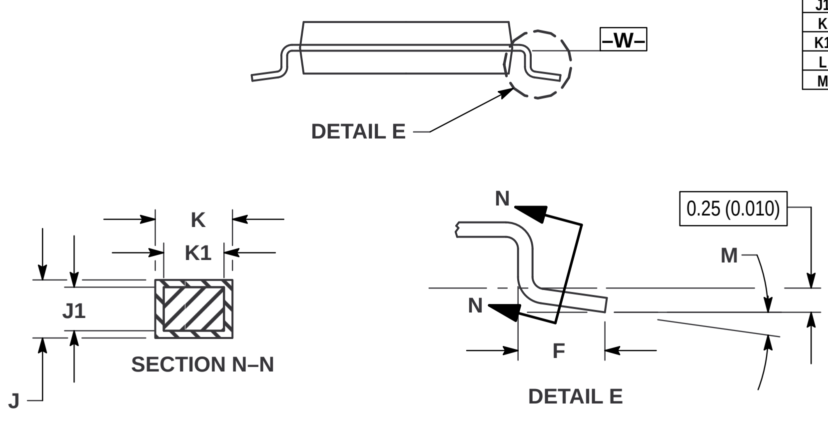
OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H–01
ISSUE O



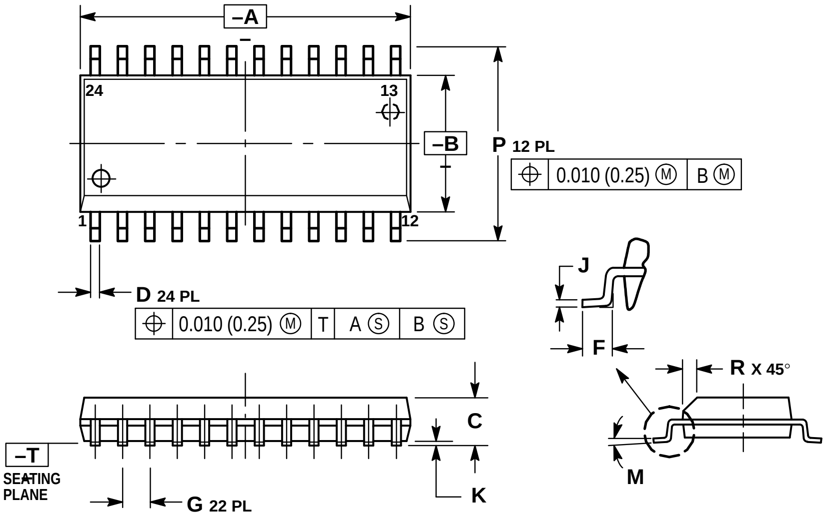
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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