Octal Bus Transceiver With 5V-Tolerant Inputs

The MC74LVX245 is an advanced high speed CMOS octal bus transceiver.

It is intended for two–way asynchronous communication between data buses. The direction of data transmission is determined by the level of the T/R input. The output enable pin (OE) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

- High Speed: tpD = 4.7ns (Typ) at VCC = 3.3V
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: Volp = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

APPLICATION NOTES

- 1. Do not force a signal on an I/O pin when it is an active output, damage may
- 2. All floating (high impedence) input or I/O pins must be fixed by means of pull up or pull down resistors or bus terminator ICs.
- 3. A parasitic diode is formed between the bus and V_{CC} terminals. Therefore, the LVX245 cannot be used to interface 5V to 3V systems directly.

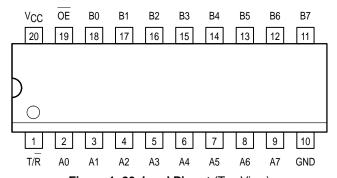


Figure 1. 20-Lead Pinout (Top View)

MC74LVX245



LOW-VOLTAGE CMOS



DW SUFFIX 20-LEAD SOIC PACKAGE CASE 751D-04



DT SUFFIX 20-LEAD TSSOP PACKAGE CASE 948E-02



M SUFFIX 20-LEAD SOIC EIAJ PACKAGE CASE 967-01

PIN NAMES

Pins	Function
O <u>E</u> T/R	Output Enable Input Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State
B0-B7	Outputs Side B 3–State Inputs or 3–State Outputs



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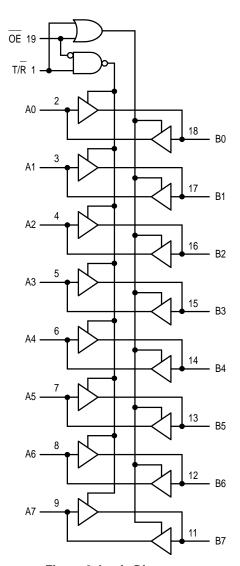


Figure 2. Logic Diagram

INPUTS		OPERATING MODE
OE	T/R	Non-Inverting
L	L	B Data to A Bus
L	Н	A Data to B Bus
Н	Х	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage	-0.5 to +7.0	V
V _{in}	DC Input Voltage (T/R, OE)	-0.5 to +7.0	V
V _{I/O}	DC Output Voltage	-0.5 to V _{CC} +0.5	V
ΙΙΚ	Input Diode Current	-20	mA
lok	Output Diode Current	±20	mA
l _{out}	DC Output Current, per Pin	±25	mA
ICC	DC Supply Current, V _{CC} and GND Pins	±75	mA
PD	Power Dissipation	180	mW
T _{stg}	Storage Temperature	-65 to +150	°C

^{*} Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute—maximum—rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCC	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage (T/R, OE)	0	5.5	V
V _{I/O}	DC Output Voltage	0	VCC	V
TA	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

			Vcc	T _A = 25°C			T _A = - 40	0 to 85°C	
Symbol	Parameter	Test Conditions	v	Min	Тур	Max	Min	Max	Unit
VIH	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
VIL	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
VOH	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = -50μA I _{OH} = -50μA I _{OH} = -4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage (Vin = V _{IH} or V _{IL})	I _{OL} = 50μA I _{OL} = 50μA I _{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{in}	Input Leakage Current	V _{in} = <u>5.5</u> V or GND (T/R, OE)	3.6			±0.1		±1.0	μА
loz	Maximum Three–State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	3.6			±0.25		±2.5	μА
ICC	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	μΑ

3

AC ELECTRICAL CHARACTERISTICS (Input $t_f = t_f = 3.0 \text{ns}$)

				T _A = 25°C			T _A = -40	0 to 85°C		
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit	
tPLH, tPHL	Propagation Delay Input to Output	V _{CC} = 2.7V	C _L = 15pF C _L = 50pF		6.1 8.6	10.7 14.2	1.0 1.0	13.5 17.0	ns	
		$V_{CC} = 3.3 \pm 0.3 V$	C _L = 15pF C _L = 50pF		4.7 7.2	6.6 10.1	1.0 1.0	8.0 11.5		
t _{PZL} , t _{PZH}	Output Enable Time to High and Low Level	$V_{CC} = 2.7V$ $R_L = 1k\Omega$	C _L = 15pF C _L = 50pF		9.0 11.5	16.9 20.4	1.0 1.0	20.5 24.0	ns	
		$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$	C _L = 15pF C _L = 50pF		7.1 9.6	11.0 14.5	1.0 1.0	13.0 16.5		
t _{PLZ} , t _{PHZ}	Output Disable Time From High and Low Level	$V_{CC} = 2.7V$ $R_L = 1k\Omega$	C _L = 50pF		11.5	18.0	1.0	21.0	ns	
		$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$	C _L = 50pF		9.6	12.8	1.0	14.5		
tOSHL tOSLH	Output-to-Output Skew (Note 1.)	V _{CC} = 2.7V V _{CC} = 3.3 ±0.3V	$C_L = 50pF$ $C_L = 50pF$			1.5 1.5		1.5 1.5	ns	

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (tOSHL) or LOW-to-HIGH (tOSLH); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

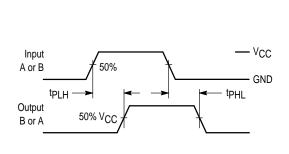
		T _A = 25°C		T _A = - 40 to 85°C			
Symbol	Parameter	Min	Тур	Max	Min	Max	Unit
C _{in}	Input Capacitance (T/R, OE)		4	10		10	pF
C _{I/O}	Maximum Three–State I/O Capacitance		8				pF
C _{PD}	Power Dissipation Capacitance (Note 2.)		21				pF

^{2.} CpD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per bit). C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input $t_{\Gamma} = t_{f} = 3.0$ ns, $C_{L} = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

		T _A = 25°C		
Symbol	Characteristic	Тур	Max	Unit
VOLP	Quiet Output Maximum Dynamic VOL	0.5	0.8	V
VOLV	Quiet Output Minimum Dynamic VOL	-0.5	-0.8	V
VIHD	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS



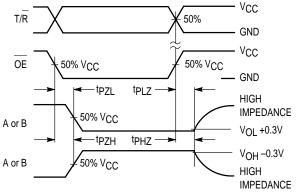
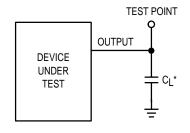


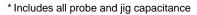
Figure 3.

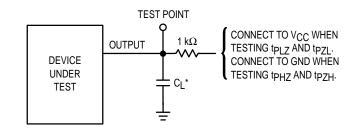
Figure 4.

TEST CIRCUITS

5





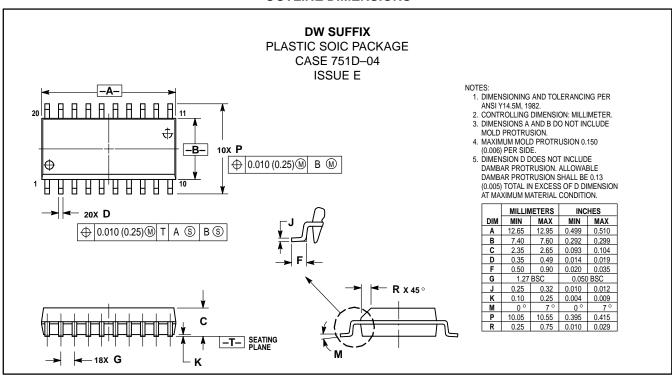


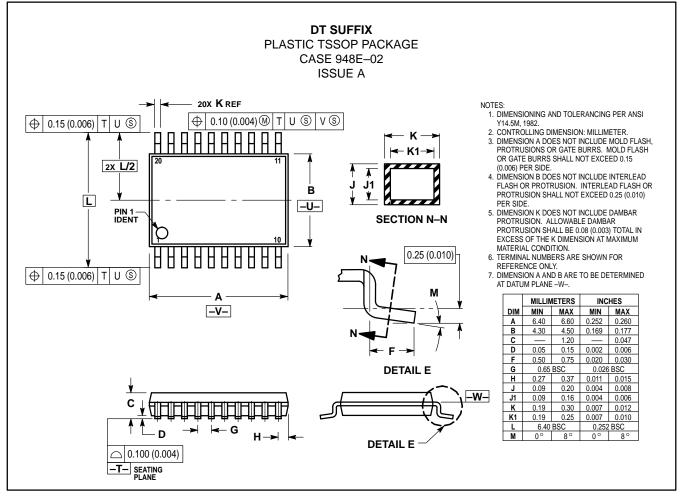
^{*} Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit

Figure 6. Three-State Test Circuit

OUTLINE DIMENSIONS

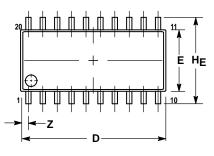


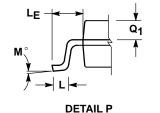


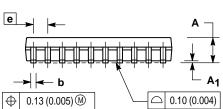
OUTLINE DIMENSIONS

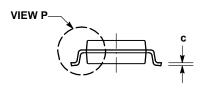
M SUFFIX

PLASTIC SOIC EIAJ PACKAGE CASE 967-01 ISSUE O









NOTES

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
- TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
 DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE
 BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
Α ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
Е	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050) BSC
±Ε	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LΕ	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z		0.81		0.032

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