MC74LVX126

Product Preview

Quad Bus Buffer
With 5V–Tolerant Inputs

The MC74LVX126 is an advanced high speed CMOS quad bus buffer. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

The MC74LVX126 requires the 3–state control input (OE) to be set Low to place the output into the high impedance state.

- High Speed: t_{PD} = 4.4ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

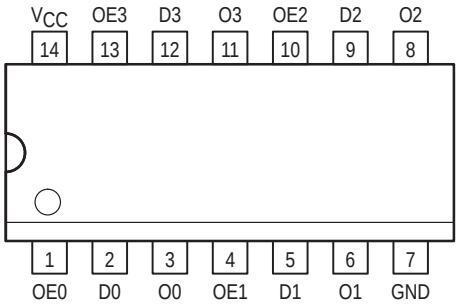

Figure 1. 14–Lead Pinout (Top View)

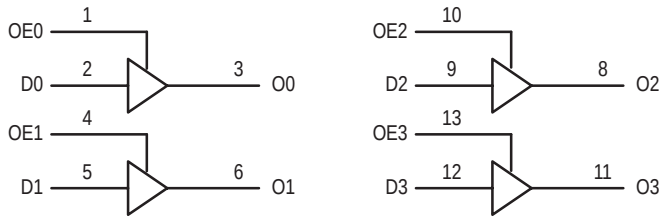

Figure 2. Logic Diagram

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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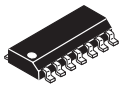
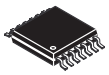
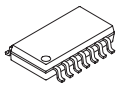


14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G



14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

PIN NAMES

Pins	Function
OEn	Output Enable Inputs
Dn	Data Inputs
On	3–State Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
OEn	Dn	On
H	L	L
H	H	H
L	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX126D	SOIC	55 Units/Rail
MC74LVX126DT	TSSOP	96 Units/Rail
MC74LVX126M	SOIC EIAJ	50 Units/Rail

DEVICE MARKING INFORMATION

For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+125	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = ≤ 85°C		T_A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50μA I_{OH} = –50μA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48			1.9 2.9 2.34	V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44		0.1 0.1 0.52	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0		±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5		±5.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40		40	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = \leq 85°C$ Min	$T_A = \leq 85°C$ Max	$T_A = \leq 125°C$ Min	$T_A = \leq 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	V_{CC} = 2.7V	C_L = 15pF		5.5	10.1	1.0	13.5	1.0	15.0	ns
			C_L = 50pF		7.5	13.6	1.0	17.0	1.0	19.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		3.9	6.2	1.0	8.5	1.0	11.0	
			C_L = 50pF		5.9	9.7	1.0	12.0	1.0	14.0	
t_{PZL}, t_{PZH}	Output Enable Time OE to O	V_{CC} = 2.7V R_L =1kΩ	C_L = 15pF		5.3	9.3	1.0	12.5	1.0	15.5	ns
			C_L = 50pF		7.8	12.8	1.0	16.0	1.0	18.5	
		V_{CC} = 3.3 ± 0.3V R_L =1kΩ	C_L = 15pF		4.0	5.6	1.0	7.5	1.0	9.5	
			C_L = 50pF		6.5	9.1	1.0	11.0	1.0	13.0	
t_{PLZ}, t_{PHZ}	Output Disable Time OE to O	V_{CC} = 2.7V R_L =1kΩ	C_L = 50pF		10.0	15.7	1.0	19.0	1.0	21.0	MHz
		V_{CC} = 3.3 ± 0.3V R_L =1kΩ	C_L = 50pF		8.3	11.2	1.0	13.0	1.0	15.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = \leq 85°C$ Min	$T_A = \leq 85°C$ Max	$T_A = \leq 125°C$ Min	$T_A = \leq 125°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10		10	pF
C_{out}	Maximum Three–State Output Capacitance		6						pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		14						pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

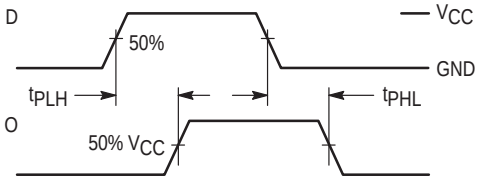


Figure 3.

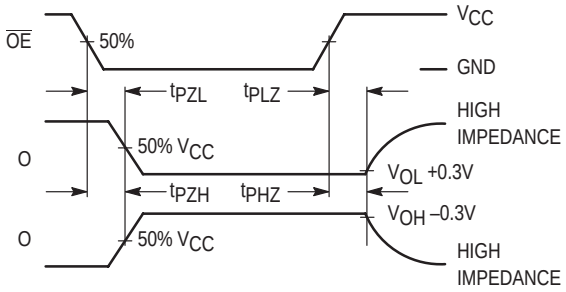
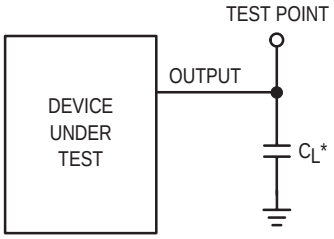


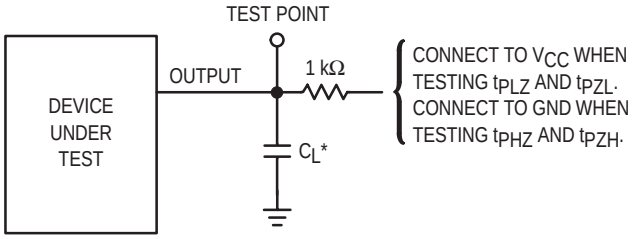
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit

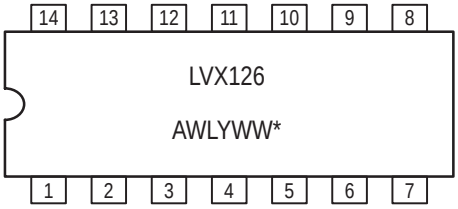


*Includes all probe and jig capacitance

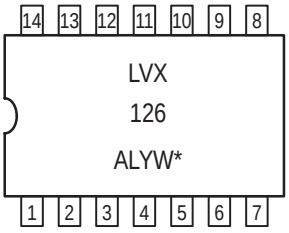
Figure 6. Three–State Test Circuit

MARKING DIAGRAMS

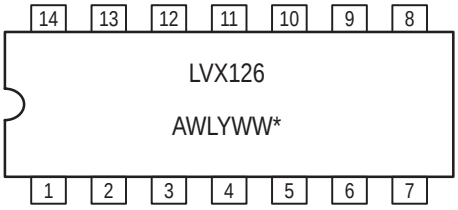
(Top View)



14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G

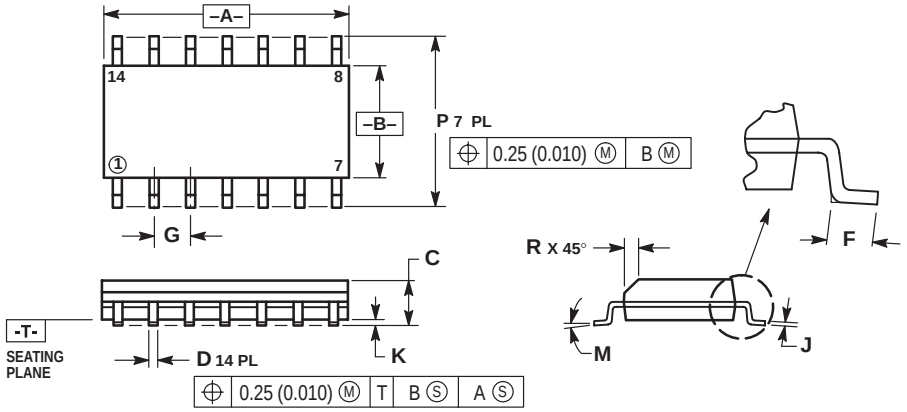


14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

*See Applications Note #AND8004/D for date code and traceability information.

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F

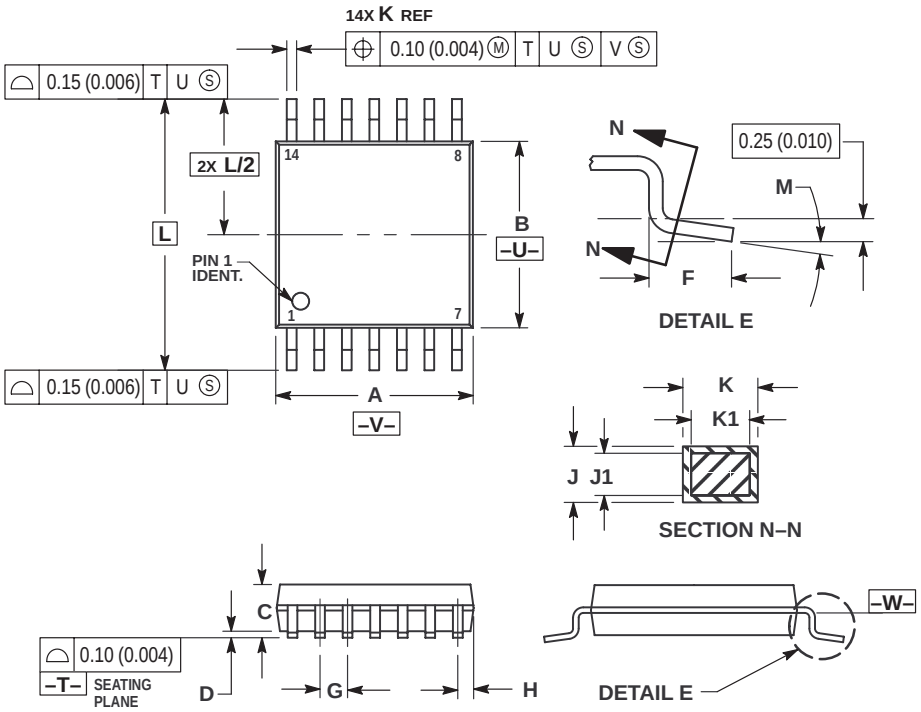


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

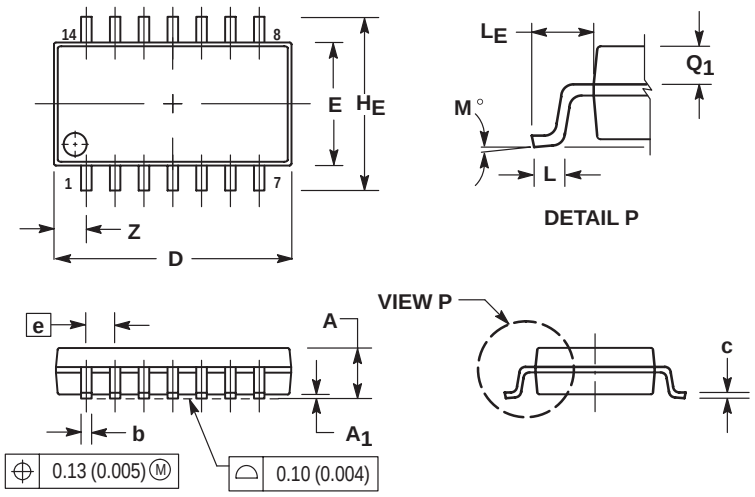


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_F	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

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