

## Low-Voltage CMOS 16-Bit Latching Transceiver

### With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16543A is a high performance, non-inverting 16-bit latching transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX16543A inputs to be safely driven from 5V devices. The MC74LCX16543A is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the  $\overline{\text{EAB}}$  LOW, the A-to-B Output Enable (OEAB) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With EAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal will latch the A latches, and the outputs no longer change with the A inputs. With EAB and OEAB both LOW, the 3-State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symmetric to that above, but uses the EBA, LEBA, and OEBA inputs.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation
- 5.2ns Maximum  $t_{pd}$
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

**MC74LCX16543A**

**LCX**

**LOW-VOLTAGE CMOS  
16-BIT LATCHING  
TRANSCEIVER**



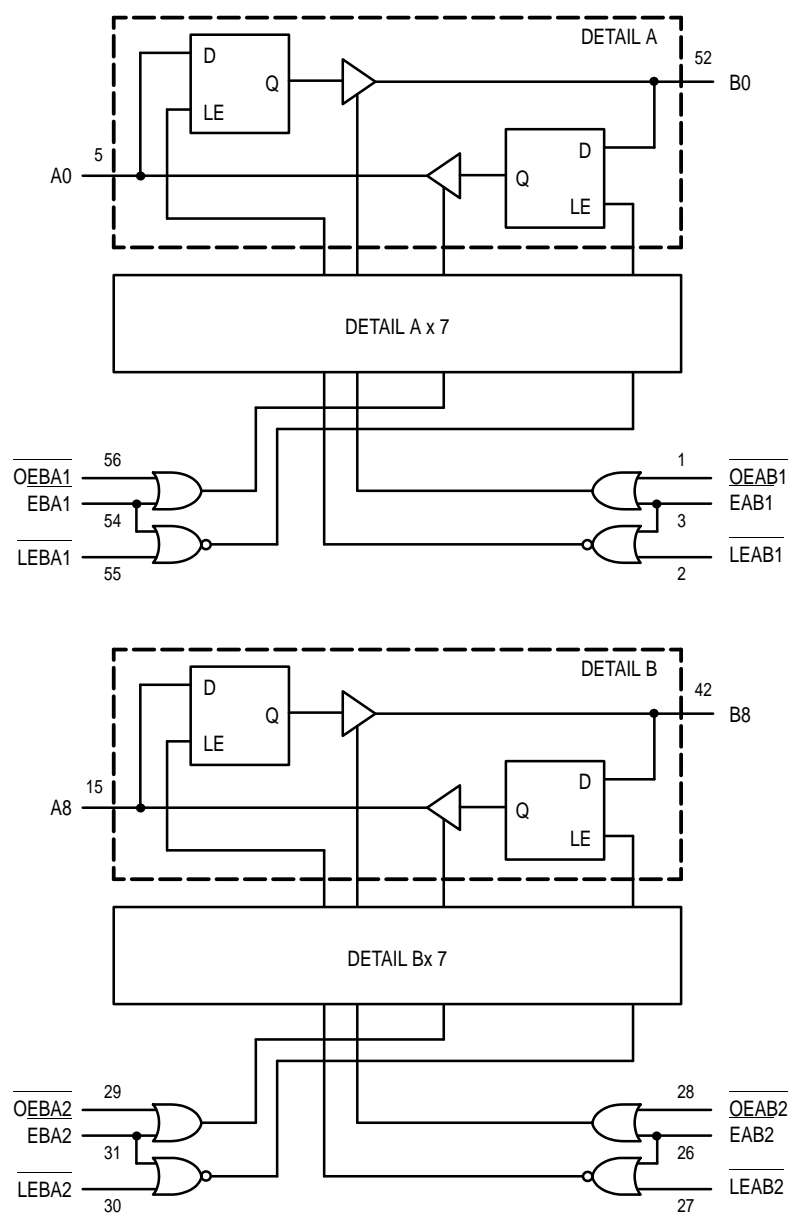
**DT SUFFIX**  
56-LEAD PLASTIC TSSOP PACKAGE  
CASE 1202-01

#### PIN NAMES

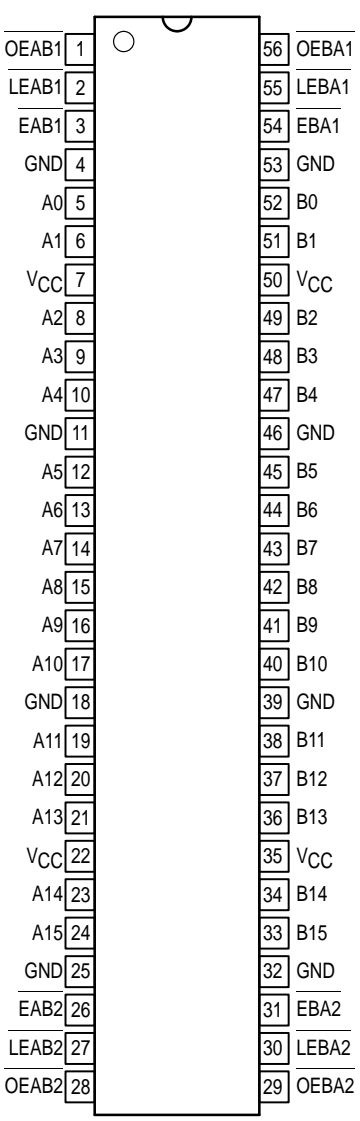
Pins	Function
$\overline{\text{OE}}_{xxn}$	Output Enable Inputs
$\overline{\text{E}}_{xxn}$	Enable Inputs
$\overline{\text{LE}}_{xxn}$	Latch Enable Inputs
A0–A15	3-State Inputs/Outputs
B0–B15	3-State Inputs/Outputs



LOGIC DIAGRAM



Pinout: 56-Lead TSSOP  
(Top View)



FUNCTION TABLE

Inputs						Data Ports		Operating Mode
OEABn	OEBA n	EABn	EBA n	LEABn	LEBA n	An	Bn	
H	H					Input	Input	
		X	X	X	X	X	X	Disable Outputs
		L	L	L	L	X	X	Transparent Data; Outputs Disabled
				H	H	l h	l h	Latch and Outputs Disabled
L	H					Input	Output	
		H	X*	L	X	l h	Z Z	Load and B Outputs Disabled
				H	X	X	Z	Hold; B Outputs Disabled
		L	X*	L	X	L H	L H	Transparent A to B
				H	X	l h	L H	Latch and Display B Outputs
H	L					Output	Input	
		X*	H	X	L	Z Z	l h	Load and A Outputs Disabled
				X	H	Z	X	Hold; A Outputs Disabled
		X*	L	X	L	L H	L H	Transparent B to A
				X	H	L H	l h	Latch and Display A Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; X = Don't Care; \* = The latches are not internally gated with the Output Enables. Therefore, data at the A or B ports may enter the latches at any time, provided that the LExx and Exx pins are set accordingly. For I<sub>CC</sub> reasons, Do Not Float Inputs.

## ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	−0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	−0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	−0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		−0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Note 1.	V
I <sub>IK</sub>	DC Input Diode Current	−50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	−50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	−65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I<sub>O</sub> absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
$V_I$	Input Voltage	0		5.5	V
$V_O$	Output Voltage (HIGH or LOW State) (3-State)	0 0		$V_{CC}$ 5.5	V
$I_{OH}$	HIGH Level Output Current, $V_{CC} = 3.0V - 3.6V$			-24	mA
$I_{OL}$	LOW Level Output Current, $V_{CC} = 3.0V - 3.6V$			24	mA
$I_{OH}$	HIGH Level Output Current, $V_{CC} = 2.7V - 3.0V$			-12	mA
$I_{OL}$	LOW Level Output Current, $V_{CC} = 2.7V - 3.0V$			12	mA
$T_A$	Operating Free-Air Temperature	-40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8V to 2.0V, $V_{CC} = 3.0V$	0		10	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
$V_{IH}$	HIGH Level Input Voltage (Note 2.)	$2.7V \leq V_{CC} \leq 3.6V$	2.0		V
$V_{IL}$	LOW Level Input Voltage (Note 2.)	$2.7V \leq V_{CC} \leq 3.6V$		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$ ; $I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7V$ ; $I_{OH} = -12\text{mA}$	2.2		
		$V_{CC} = 3.0V$ ; $I_{OH} = -18\text{mA}$	2.4		
		$V_{CC} = 3.0V$ ; $I_{OH} = -24\text{mA}$	2.2		
$V_{OL}$	LOW Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$ ; $I_{OL} = 100\mu\text{A}$		0.2	V
		$V_{CC} = 2.7V$ ; $I_{OL} = 12\text{mA}$		0.4	
		$V_{CC} = 3.0V$ ; $I_{OL} = 16\text{mA}$		0.4	
		$V_{CC} = 3.0V$ ; $I_{OL} = 24\text{mA}$		0.55	
$I_I$	Input Leakage Current	$2.7V \leq V_{CC} \leq 3.6V$ ; $0V \leq V_I \leq 5.5V$		$\pm 5.0$	$\mu\text{A}$
$I_{OZ}$	3-State Output Current	$2.7 \leq V_{CC} \leq 3.6V$ ; $0V \leq V_O \leq 5.5V$ ; $V_I = V_{IH}$ or $V_{IL}$		$\pm 5.0$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$V_{CC} = 0V$ ; $V_I$ or $V_O = 5.5V$		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$2.7 \leq V_{CC} \leq 3.6V$ ; $V_I = \text{GND}$ or $V_{CC}$		20	$\mu\text{A}$
		$2.7 \leq V_{CC} \leq 3.6V$ ; $3.6 \leq V_I$ or $V_O \leq 5.5V$		$\pm 20$	$\mu\text{A}$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$2.7 \leq V_{CC} \leq 3.6V$ ; $V_{IH} = V_{CC} - 0.6V$		500	$\mu\text{A}$

2. These values of  $V_I$  are used to test DC electrical characteristics only.

**AC CHARACTERISTICS** ( $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits				Unit
			T <sub>A</sub> = −40°C to +85°C				
			V <sub>CC</sub> = 3.0V to 3.6V		V <sub>CC</sub> = 2.7V		
			Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay An to Bn or Bn to An	1	1.5 1.5	5.4 5.4	1.5 1.5	6.0 6.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBAn to An or LEABn to Bn	4	1.5 1.5	7.0 7.0	1.5 1.5	8.2 8.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA <sub>n</sub> to An or OEAB <sub>n</sub> to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA <sub>n</sub> to An or OEAB <sub>n</sub> to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time EBA <sub>n</sub> to An or EAB <sub>n</sub> to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time EBA <sub>n</sub> to An or EAB <sub>n</sub> to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t <sub>s</sub>	Setup Time, HIGH to LOW Data to LExxn	4	2.5		2.5		ns
t <sub>h</sub>	Hold Time, HIGH to LOW Data to LExxn	4	1.5		1.5		ns
t <sub>s</sub>	Setup Time, HIGH to LOW Data to Exxn	4	2.5		2.5		ns
t <sub>h</sub>	Hold Time, HIGH to LOW Data to Exxn	4	1.5		1.5		ns
t <sub>w</sub>	Latch Enable or Enable Pulse Width, LOW	4	3.0		3.0		ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 3.)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

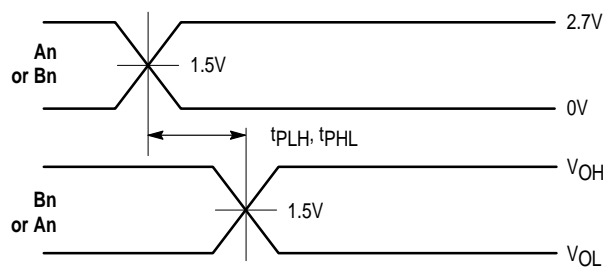
**DYNAMIC SWITCHING CHARACTERISTICS**

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 4.)	$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$ , $V_{IH} = 3.3\text{V}$ , $V_{IL} = 0\text{V}$		0.8		V
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 4.)	$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$ , $V_{IH} = 3.3\text{V}$ , $V_{IL} = 0\text{V}$		0.8		V

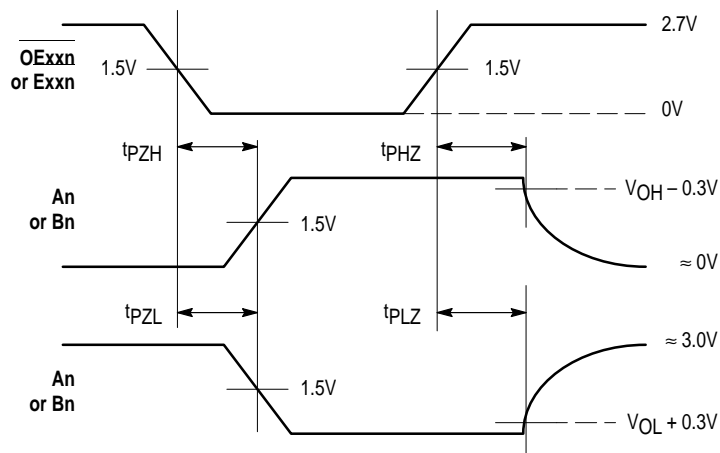
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	20	pF

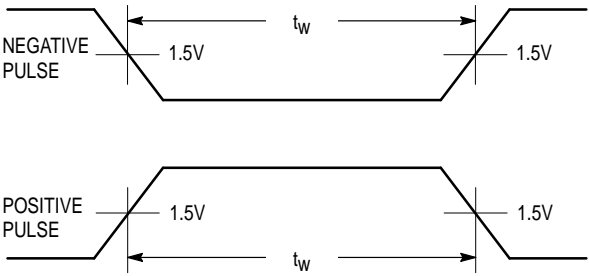


**WAVEFORM 1 – A/B to B/A PROPAGATION DELAYS**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

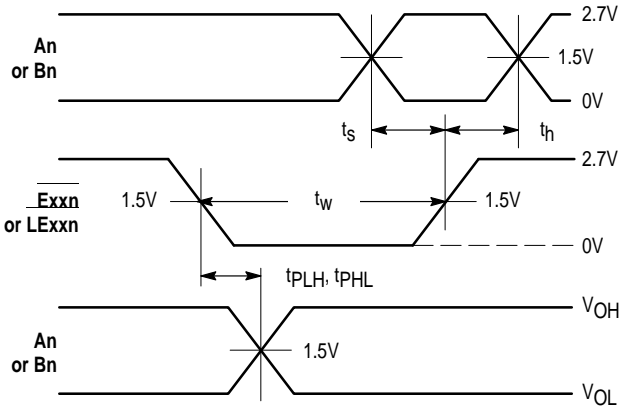


**WAVEFORM 2 – OExx/Exx to A or B OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 1. AC Waveforms**

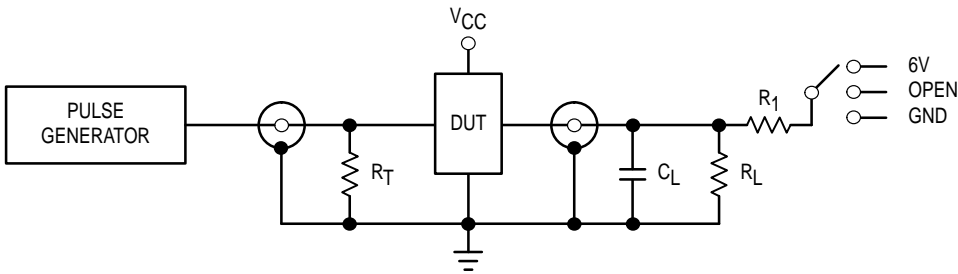


**WAVEFORM 3 – INPUT PULSE DEFINITION**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90% of 0V to 2.7V



**WAVEFORM 4 – Enable to A or B PROPAGATION DELAYS, Enable MINIMUM PULSE WIDTH, A or B to Enable SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$  except when noted

**Figure 2. AC Waveforms** (continued)



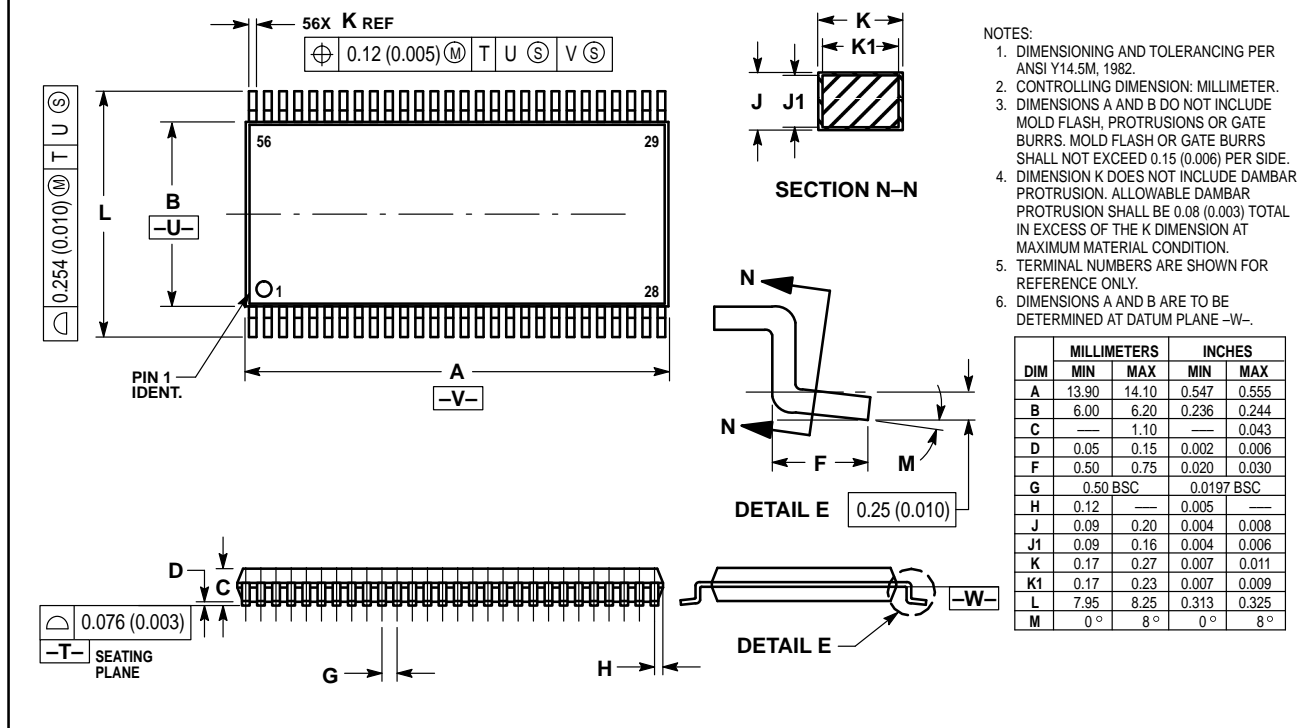
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND


$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 3. Test Circuit**

## OUTLINE DIMENSIONS

DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 1202-01  
ISSUE A



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