MC74LCX14

Product Preview

Low Voltage CMOS Hex Schmitt Inverter

With 5 V–Tolerant Inputs

The MC74LCX14 is a high performance hex inverter with Schmitt–Trigger inputs operating from a 2.7 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers, while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX14 inputs to be safely driven from 5 V devices.

Pin configuration and function are the same as the MC74LCX04, but the inputs have hysteresis and, with its Schmitt trigger function, the LCX14 can be used as a line receiver which will receive slow input signals.

- Designed for 2.3 V to 3.6 V V_{CC} Operation
- 5 V Tolerant Inputs – Interface Capability With 5 F TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μA) Substantially Reduces System Power Requirements
- Latch Performance Exceeds 500 mA
- Current Drive Capability is 24 mA at the Outputs
- Pin and Function Compatible with Other Standard Logic Families
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 60 FETs or 15 Equivalent Gates

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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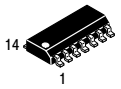
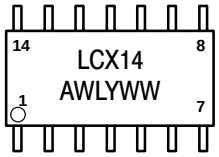
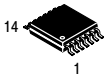
MARKING DIAGRAMS

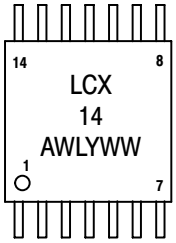


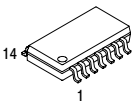
SOIC–14
D SUFFIX
CASE 751A



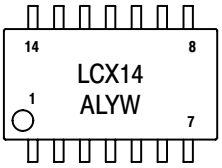


TSSOP–14
DT SUFFIX
CASE 948G





SOIC EIAJ–14
M SUFFIX
CASE 965

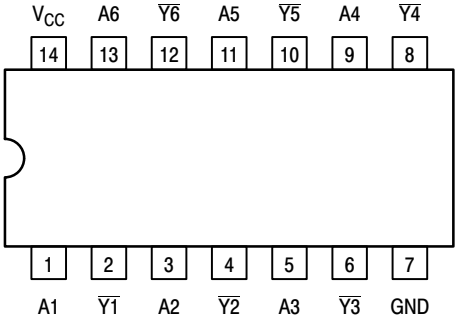


A =Assembly Location
WL or L = Wafer Lot
Y = Year
WW or W = Work Week

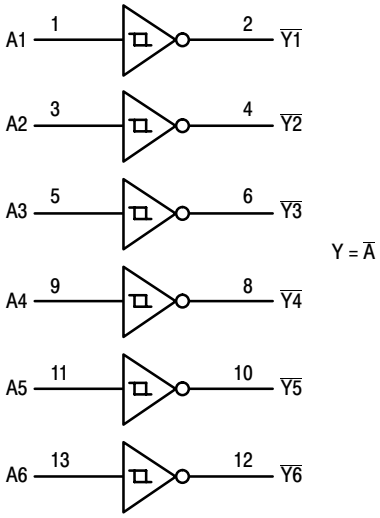
ORDERING INFORMATION

Device	Package	Shipping
MC74LCX14D	SOIC–14	55 Units/Rail
MC74LCX14DR2	SOIC–14	2500 Units/Reel
MC74LCX14DT	TSSOP–14	96 Untis/Rail
MC74LCX14DTR2	TSSOP–14	2500 Units/Reel
MC74LCX14M	SOIC EIAJ–14	50 Units/Rail
MC74LCX14MEL	SOIC EIAJ–14	2000 Units/Reel

Pinout: 14–Lead Packages (Top View)



LOGIC DIAGRAM



PIN NAMES

Pins	Function
An	Data Inputs
$\overline{Yn}$	Outputs

FUNCTION TABLE

Inputs	Outputs
A	**$\overline{Y}$**
L	H
H	L

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$–0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$–0.5 \le V_O \le V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	2.3 to 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0		V_{CC}	V
I_{OH}	HIGH Level Output Current	V_{CC}= 3.0V–3.6V V_{CC}= 2.7V–3.0V V_{CC}= 2.3V–2.7V			–24 –12 –8	mA
I_{OL}	LOW Level Output Current	V_{CC}= 3.0V–3.6V V_{CC}= 2.7V–3.0V V_{CC}= 2.3V–2.7V			+24 +12 +8	mA
T_A	Operating Free–Air Temperature		–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = – 40 to 85°C			Unit
			Min	Typ	Max	
V_{T+}	Positive Input Threshold Voltage (Figure 3.)	2.3V ≤ V_{CC} < 2.7V 2.7V ≤ V_{CC} < 3.0V 3.0V ≤ V_{CC} < 3.6V	0.9 TBD 1.2	TBD TBD TBD	1.7 TBD 2.2	V
$V_{T–}$	Negative Input Threshold Voltage (Figure 3.)	2.3V ≤ V_{CC} < 2.7V 2.7V ≤ V_{CC} < 3.0V 3.0V ≤ V_{CC} < 3.6V	0.4 TBD 0.6	TBD TBD TBD	1.1 TBD 1.5	V
V_H	Input Hysteresis Voltage (Figure 3.)	2.3V ≤ V_{CC} < 2.7V 2.7V ≤ V_{CC} < 3.0V 3.0V ≤ V_{CC} < 3.6V	0.3 TBD 0.4	TBD TBD TBD	1.0 TBD 1.2	V
V_{OH}	Minimum HIGH–Level Output Voltage	2.3V ≤ V_{CC} ≤ 3.6V, I_{OH}= 100μA V_{CC}= 2.3V, I_{OH}= 8**m**A V_{CC}= 2.7V, I_{OH}= 12**m**A V_{CC}= 3.0V, I_{OH}= 18**m**A V_{CC}= 3.0V, I_{OH}= 24**m**A	V_{CC} – 0.2 1.7 2.2 2.4 2.2			V
V_{OL}	Maximum LOW–Level Output Voltage	2.3V ≤ V_{CC} ≤ 3.6V, I_{OL}= 100μA V_{CC}= 2.3V, I_{OL}= 8**m**A V_{CC}= 2.7V, I_{OL}= 12**m**A V_{CC}= 3.0V, I_{OL}= 18**m**A V_{CC}= 3.0V, I_{OL}= 24**m**A			0.2 0.7 0.4 0.4 0.55	V
I_I	Maximum Input Leakage Current	2.3V ≤ V_{CC} ≤ 3.6V, 0V ≤ V_I ≤ 5.5V			±5.0	μA
I_{CC}	Maximum Quiescent Supply Current	2.3V ≤ V_{CC} ≤ 3.6V, V_I= V_{CC} or GND 2.3V ≤ V_{CC} ≤ 3.6V, 3.6V ≤ V_I ≤ 5.5V			10 ±10.0	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.3V ≤ V_{CC} ≤ 3.6V, One Input at V_{IH}= V_{CC}–0.6			500	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Limits						Unit
		T_A= –40°C to +85°C						
		V_{CC}= 3.0V to 3.6V		V_{CC}= 2.7V		V_{CC}= 2.3V to 2.7V		
		C_L= 50pF		C_L= 50pF		C_L= 30pF		
		Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to Y	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	1.5 1.5	7.8 7.8	ns
t_{OSHL}, t_{OSLH}	Output–to–Output Skew		1.0 1.0					ns

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 1.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V V_{CC} = 2.5V, C_L = 30pF, V_{IH} =2.5V, V_{IL} = 0V		0.9 0.7		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 1.)	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V V_{CC} = 2.5V, C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V		–0.8 –0.6		V

1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF

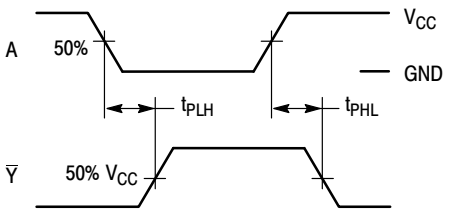
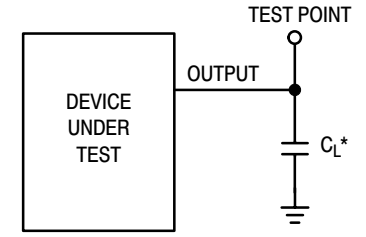


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

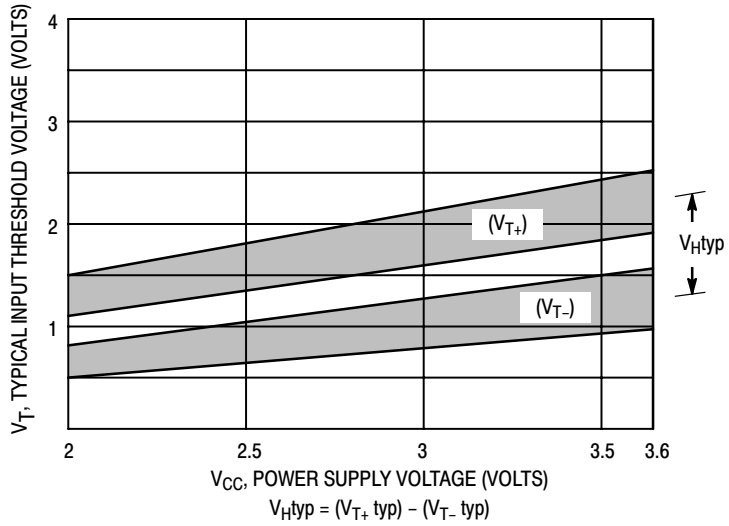


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

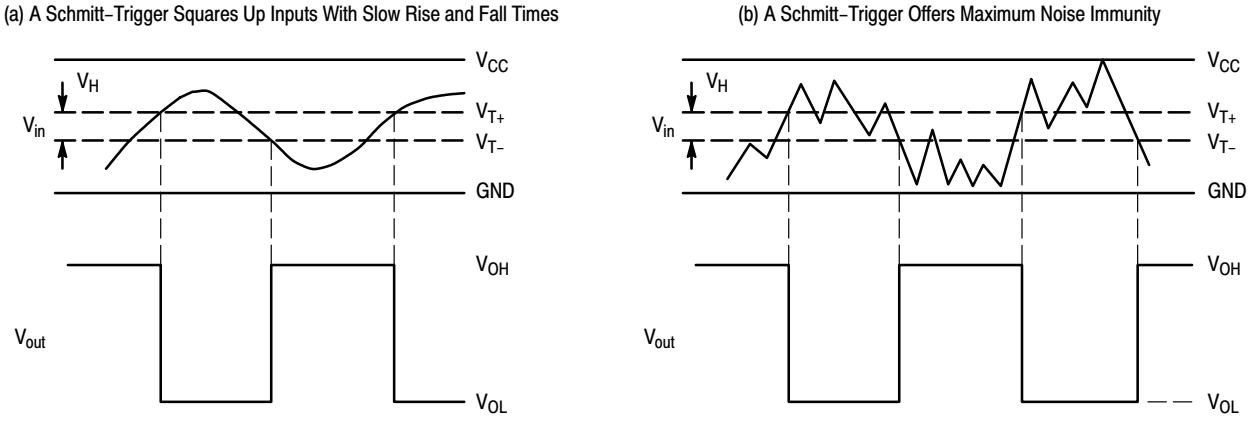


Figure 4. Typical Schmitt–Trigger Applications

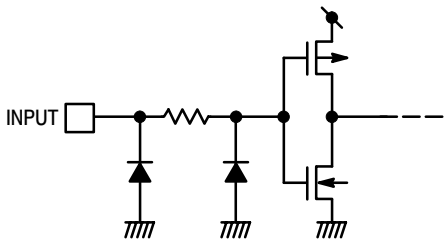
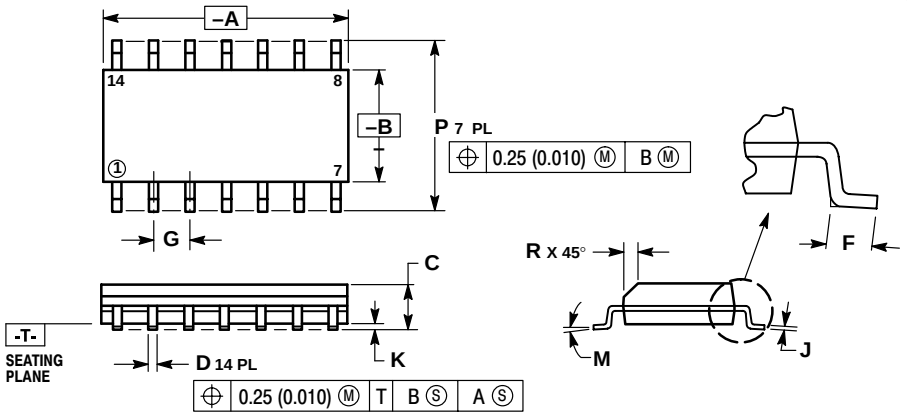


Figure 5. Input Equivalent Circuit

PACKAGE DIMENSIONS

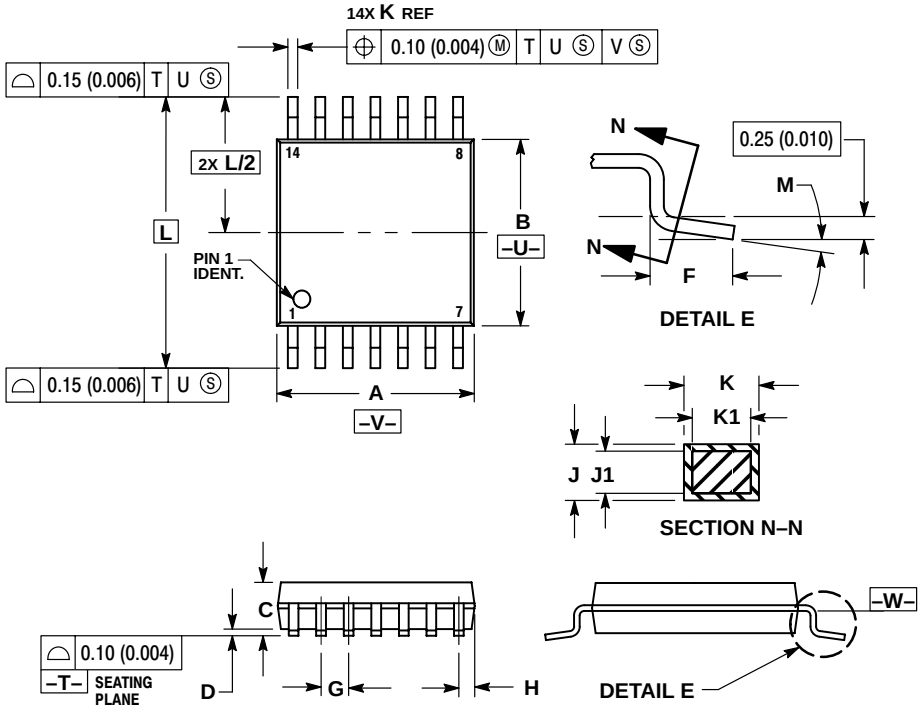
SOIC–14
D SUFFIX
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP–14
DT SUFFIX
CASE 948G–01
ISSUE O

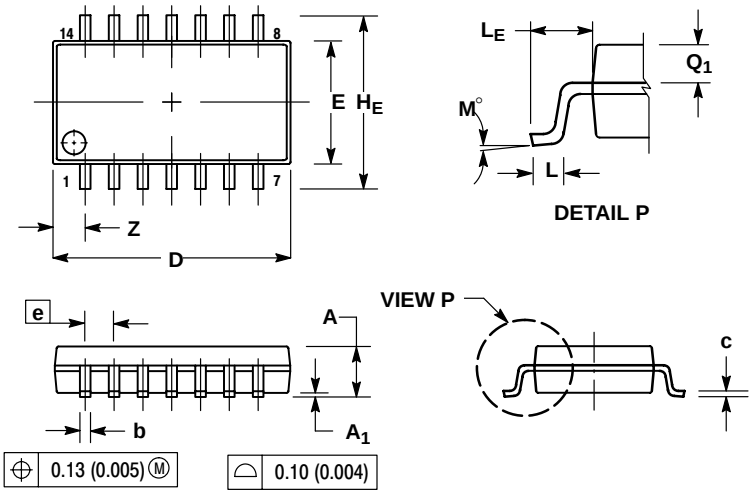


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOIC EIAJ–14
M SUFFIX
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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