# Hex Unbuffered Inverter
High–Performance Silicon–Gate CMOS

The MC74HCU04A is identical in pinout to the LS04 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single–stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high–input impedance amplifier. For digital applications, the HC04A is recommended.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V; 2.5 to 6 V in Oscillator Configurations
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 12 FETs or 3 Equivalent Gates
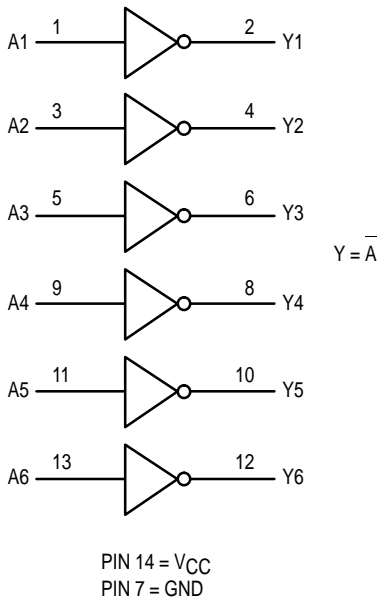
MC74HCU04A
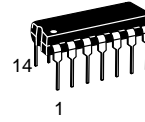
N SUFFIX
PLASTIC PACKAGE
CASE 646–06
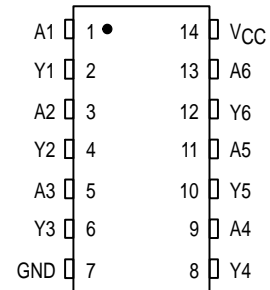
14
1

D SUFFIX
SOIC PACKAGE
CASE 751A–03

14
1

DT SUFFIX
TSSOP PACKAGE
CASE 948G–01

14
1

ORDERING INFORMATION

MC74HCUXXAN	Plastic
MC74HCUXXAD	SOIC
MC74HCUXXADT	TSSOP

LOGIC DIAGRAM

A1 —1—▷○—2— Y1

A2 —3—▷○—4— Y2

A3 —5—▷○—6— Y3

A4 —9—▷○—8— Y4

A5 —11—▷○—10— Y5

A6 —13—▷○—12— Y6

$Y = \overline{A}$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1 ●	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

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MC74HCU04A

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		− 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)		− 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)		− 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 50	mA
P_D	Power Dissipation in Still Air	Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature		− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from case for 10 Seconds Plastic DIP, SOIC or TSSOP Package		260	°C

> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
>
> Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.
  Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: –10mW/°C from 65° to 125°C
             SOIC Package: –7mW/°C from 65° to 125°C
             TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	− 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions		V_{CC} V	Guaranteed Limit			Unit
					− 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.5 V* $|I_{out}|$ ≤ 20 µA		2.0 3.0 4.5 6.0	1.7 2.5 3.6 4.8	1.7 2.5 3.6 4.8	I.7 2.5 3.6 4.8	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = V_{CC} − 0.5 V* $|I_{out}|$ ≤ 20 µA		2.0 3.0 4.5 6.0	0.3 0.5 0.8 1.1	0.3 0.5 0.8 1.1	0.3 0.5 0.8 1.1	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = GND $|I_{out}|$ ≤ 20 µA		2.0 4.5 6.0	1.8 4.0 5.5	1.8 4.0 5.5	1.8 4.0 5.5	V
		V_{in} = GND	$|I_{out}|$ ≤ 2.4 mA $|I_{out}|$ ≤ 4.0 mA $|I_{out}|$ ≤ 5.2 mA	3.0 4.5 6.0	2.36 3.86 5.36	2.26 3.76 5.26	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{CC} $|I_{out}|$ ≤ 20 µA		2.0 4.5 6.0	0.2 0.5 0.5	0.2 0.5 0.5	0.2 0.5 0.5	V
		V_{in} = V_{CC}	$|I_{out}|$ ≤ 2.4 mA $|I_{out}|$ ≤ 4.0 mA $|I_{out}|$ ≤ 5.2 mA	3.0 4.5 6.0	0.32 0.32 0.32	0.32 0.37 0.37	0.32 0.40 0.40	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				− 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 µA	6.0	1	10	40	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
* For V_{CC} = 2.0 V, V_{out} = 0.2 V or V_{CC} − 0.2 V.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	70 40 14 12	90 45 18 15	105 50 21 18	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
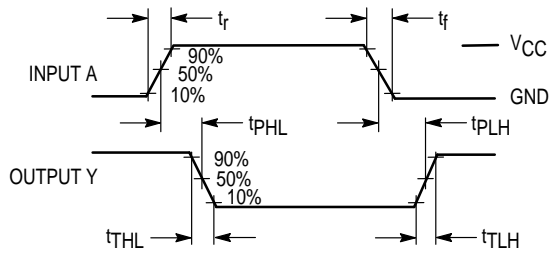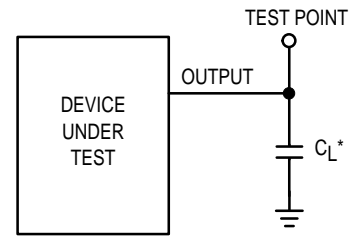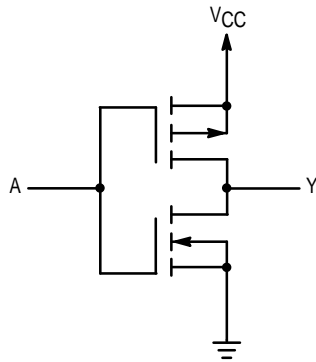
MC74HCU04A

Figure 1. Switching Waveforms

* Includes all probe and jig capacitance
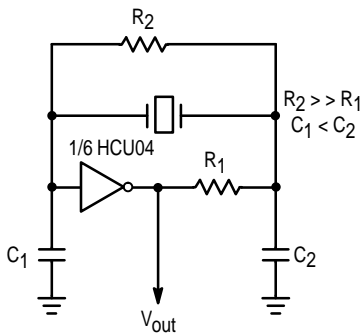
Figure 2. Test Circuit

LOGIC DETAIL
(1/6 of Device Shown)
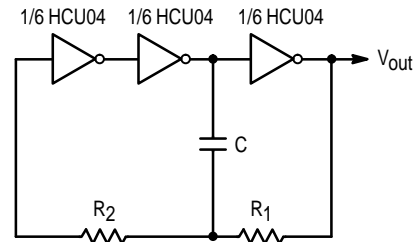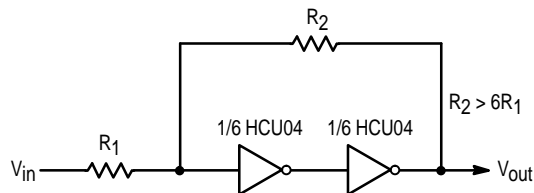
TYPICAL APPLICATIONS

Crystal Oscillator

$R_2 >> R_1$
$C_1 < C_2$

R2

1/6 HCU04   R1

C1   C2

V_{out}

Stable RC Oscillator

1/6 HCU04   1/6 HCU04   1/6 HCU04

V_{out}

C

R2   R1

Schmitt Trigger

R2

$R_2 > 6R_1$

V_{in} R1   1/6 HCU04   1/6 HCU04 V_{out}

**High Input Impedance Single–Stage Amplifier
with a 2 to 6 V Supply Range**

V_{CC}

1 M   1/6 HCU04

INPUT   OUTPUT

1 M

Multi–Stage Amplifier

V_{CC}

1/6 HCU04   1/6 HCU04   1/6 HCU04

INPUT   OUTPUT

LED Driver

+V

1/6 HCU04
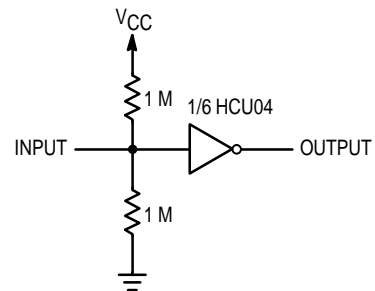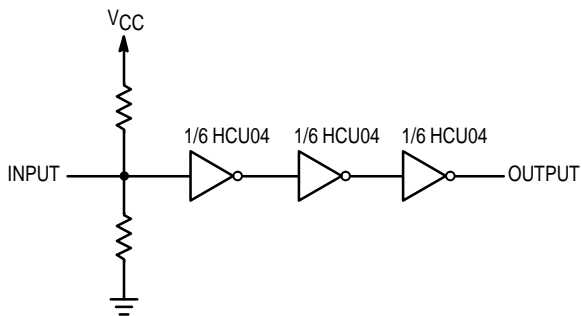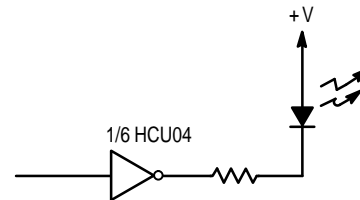
For reduced power supply current, use high–efficiency LEDs
such as the Hewlett–Packard HLMP series or equivalent.

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L
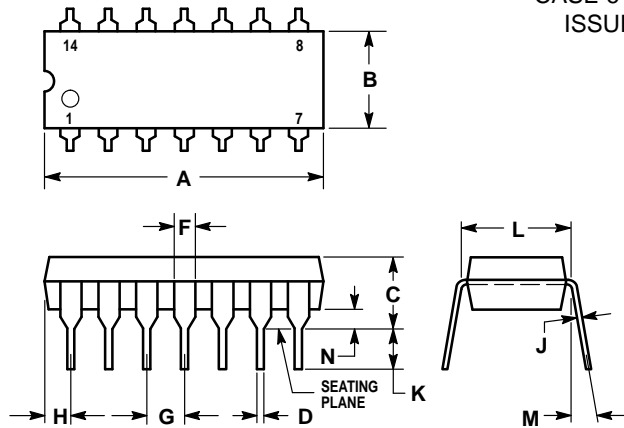
NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F
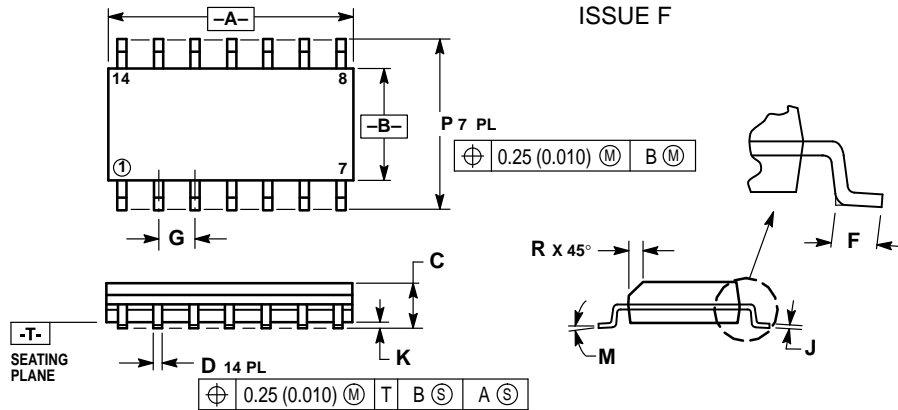
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O
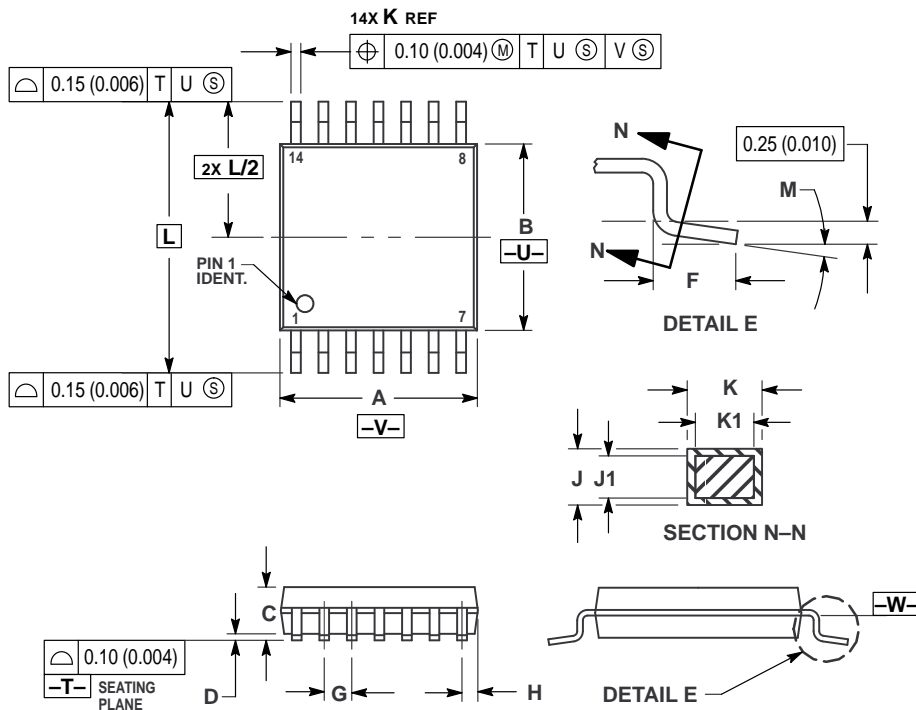
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

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