MC74HC174A

Hex D Flip-Flop with Common Clock and Reset

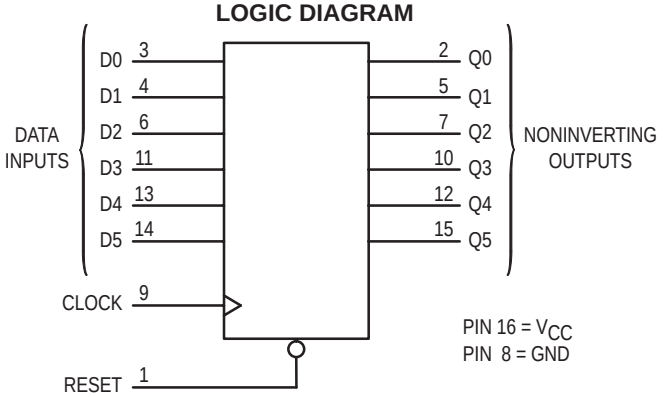
High–Performance Silicon–Gate CMOS

The MC74HC174A is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip–flops with common Clock and Reset inputs. Each flip–flop is loaded with a low–to–high transition of the Clock input. Reset is asynchronous and active–low.

- Output Drive Capability: 10 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change
H	↓	X	No Change

Design Criteria	Value	Units
Internal Gate Count*	40.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two–input NAND gate.

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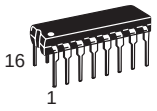
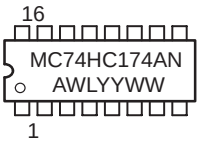
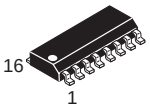
MARKING DIAGRAMS

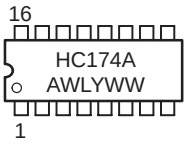


PDIP–16
N SUFFIX
CASE 648



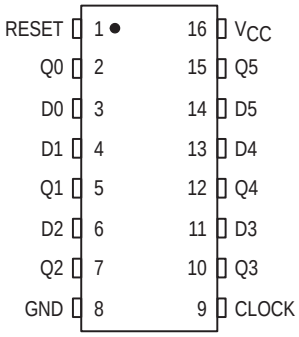


SO–16
D SUFFIX
CASE 751B



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC174AN	PDIP–16	2000 / Box
MC74HC174AD	SOIC–16	48 / Rail
MC74HC174ADR2	SOIC–16	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTES:
1. Information on typical parametric values along with high frequency or heavy load considerations, can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Total Supply Current = $I_{CC} + S\Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	110 21 19	140 28 24	160 32 27	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

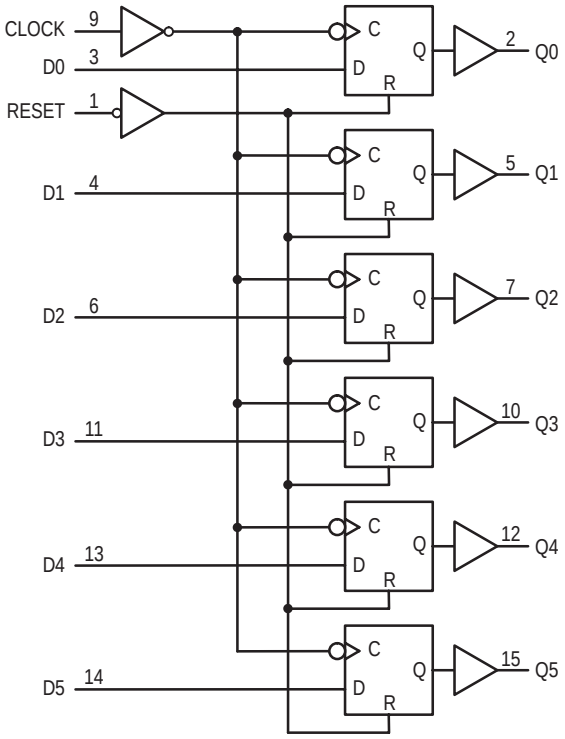
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	62	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	V_{CC} V	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	2.0 4.5 6.0	50 10 9.0		65 13 11		75 15 13		ns
t_h	Minimum Hold Time, Clock to Data	3	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock	2	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	1	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_w	Minimum Pulse Width, Reset	2	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

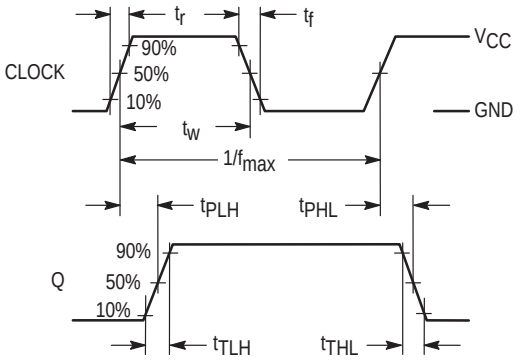


Figure 1.

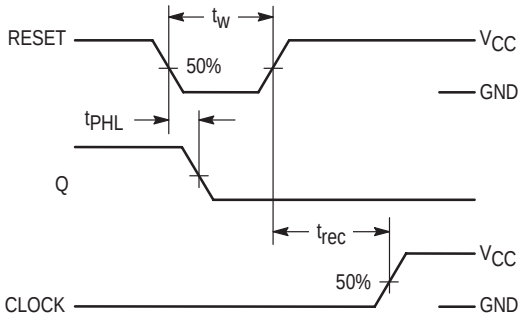


Figure 2.

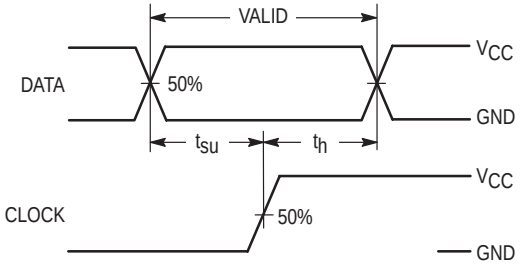
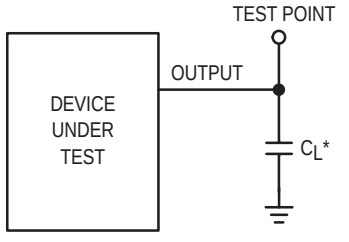


Figure 3.

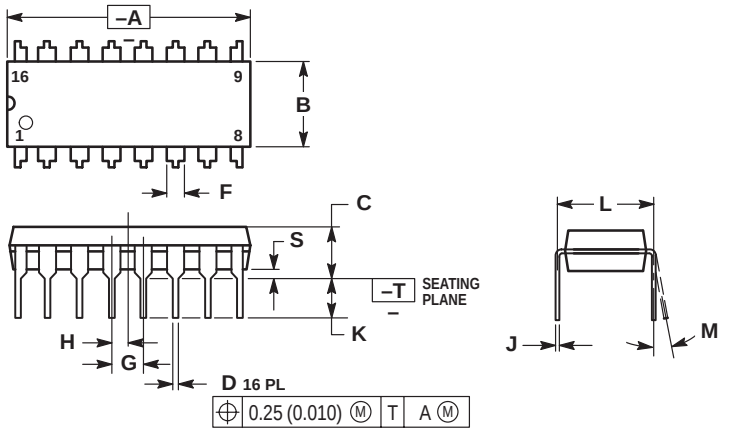


*Includes all probe and jig capacitance

Figure 4. Test Circuit

PACKAGE DIMENSIONS

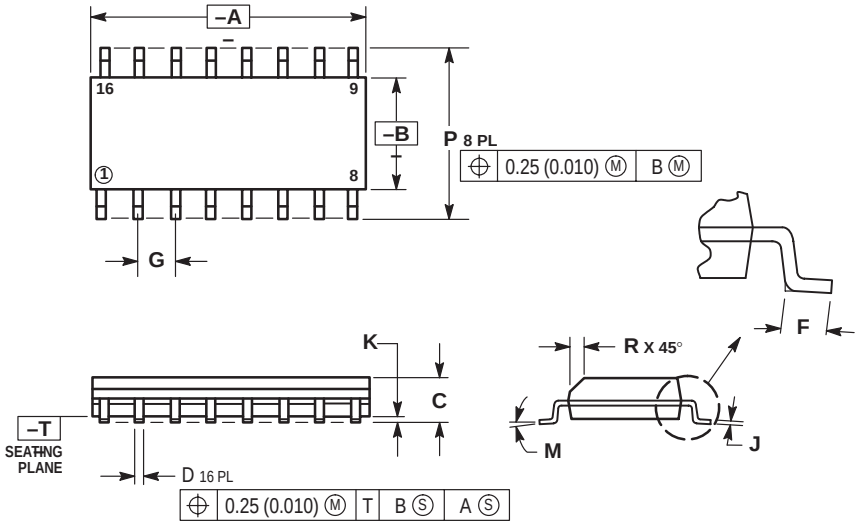
PDIP–16
N SUFFIX
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC–16
D SUFFIX
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Notes

Notes

PUBLICATION ORDERING INFORMATION

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