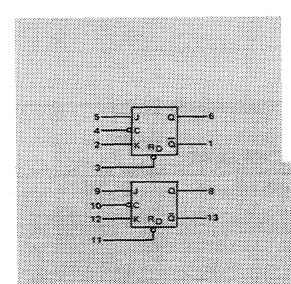
MC663 MC12663

ISSUE A



The MC663 and the MC12663 consist of two J-K flip-flops having direct reset inputs in addition to clocked inputs. The 15 volt V_{CC} device (MC663) and the extended 12-15 volt V_{CC} device (MC12663), are schematically indentical. The MC12663 meets the MC663 specifications in addition to the 12 volt specifications. Both are available in the 14 pin dual-in-line plastic package (suffix P) and the 14 pin dual-in-line ceramic package (suffix L). A full temperature version of the MC663 dual-in-line ceramic is also available (suffix tL). This device meets the -30 to +75 standard specifications at -55 to +125 respectively

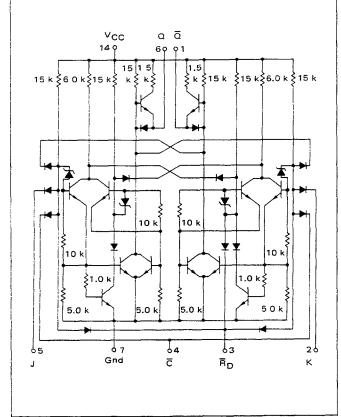
Input Loading Factor

Rig Input # 2
C Input # 15
COMM Input # 1

Output Loading Factor # 9
Ing # 3.0 MHz typ

Total Power Dissipation # 200 mW typ

CIRCUIT SCHEMATIC (1/2 OF CIRCUIT SHOWN)



See General Information section for packaging

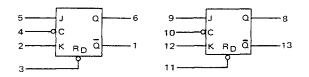
TRUTH TABLE

		1	n		t _{n+1}									
	Jn	Кn	Ĉ _n	Ŕ _D	J _{n+1}	K _{n+1}	$\overline{C_{n+1}}$	Ŕ _D	Q _{n+1}					
See	0	0	Х	1	Х	×	Х	1	a _n					
Note	1	0	1	1	1	0	0	1	1					
	0	1	1	1	0	1	0	1	0					
е	1	1	1	1	1	1	0	1	ān					
See	×	×	0	1	×	×	0	1	σ'n					
Note	1	×	1	1	0	Kn	1	1	1					
NOTE	×	1	1	1	Jn	0	1	1	0					
	1	1	1	1	0	0	1	1	<u>o</u> u					
See Note g	х	×	×	1	×	×	×	0	0					

- a t_n refers to the time period immediately prior to an input transition. t_{n+1} applies to the time period after the transition.
- b. J_n , K_n , etc., denotes the state of the input during the time period t_n ; J_{n+1} , K_{n+1} , etc., denotes the state of the input during the time period t_{n+1} .
- c. Q_{n+1} denotes the state achieved by the output during the time period t_{n+1} .
- d A "0" at an input terminal denotes low state (-1.0 V to 6.5 V), "1" denotes high state (8.5 V to 18 V). An "X" means that either a "0" or "1" may be applied.
- e. This portion of the truth table refers to synchronous (clocked) operation. Note that a "1" to "0" transition of the J or K input should not occur while the clock input $(\bar{\mathbb{C}})$ is high.
- f This portion of the truth table refers to dynamic J-K operation. Note that the clock input (\bar{C}) must remain high for this mode of operation.
- g. This portion of the truth table refers to asynchronous operation. Note that a low level on $\overline{\bf R}_D$ overrides all other inputs.
- Rise (or fall) time of inputs should be less than 200 nanoseconds measured between 6.5 and 8.5 volts.
- j. Inputs which are not used should be returned through a resistor (2 k Ω -20 k Ω) to V_{CC}.

ELECTRICAL CHARACTERISTICS

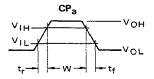
Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.

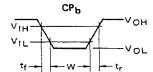


	nΑ	Volts												
OL	IOH	VIL	VIH.	VE	VR	VCCL	Vccн							
10.8	-0.027	6.50	8.50	1.5	16.0	14.0	16.0							

Characteristic Sy						MC663 T	est Limits					TEST CUI	REENT/V	OL TAGE	APPLIE)			ł	į
		Pin Under	-30°C		+25°C		+75°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										1
	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	1OL	ЮН	VIL	VtH	٧۴	VR	I VCCL	Vccн	CP ₃	CPb	Gnd
	VOL	1 6	-	1.5 1.5	-	1.5 1.5	-	1.5 1.5	Vdc Vdc	6	_	2 5	3.5 2,3	-	_	14	-	4	-	7
	VOH	1 1 6	-	-	12 5 12 5 12.5	-	12 5 12 5 12.5	-	Vdc Vdc Vdc	-	1 1 6	2,3 5 2	5 23 3.5	-	-	14 14 14	-	4 4 4		7 7 7
Short Circuit	isc	1	-		-6.5	-15	-6.5	-15	mAdc		-	3,4	-	-	-	, _	14		 -	1,7
Reverse Current	1R	2	-			2.0		20	μAdc		-	_	-	Γ-	2	14			-	3,4,5,7
	318	3	-		_	6.0	_	6.0	μAdc	-	-		-	T -	3	2.4,5.14	-			7
	21 R	4			-	4.0	-	4.0	μAdc	-			-	-	4	14	-		-	2.3.5.7
	1R	5	_	-	-	2.0	_	2.0	μAdc	-	-	-	-	-	5_	. 14	-			2,3.4,7
Forward Current	۱۶	2				-1.20	-	-1.20	mAdc	-	-	-	-	2	-	-	14		4	7
	21 F	3	_		-	-2.40		-2.40	mAdc	-	_	-	_	3	i -		14		-	2,4,5
	151F	4		-	-	-1.80	-	-1.80	mAdc	-	-	-	-	4		-	2.5,14			7
iF	i,F	5	-	_		-1.20	-	-1.20	mAdc	-	-	-	-	5		-	14	-	4	7
Power Drain Current Both Flip-Floos)	CCL	14	-	-	-	16 7	~	-	mAdc	-	-	-	-	-	-	-	14	-	-	2,3,4,5 7,9 10,11,12
	¹ CCH	14			-	16 7		_	mAdc			-	-		_	-	14	-	-	7

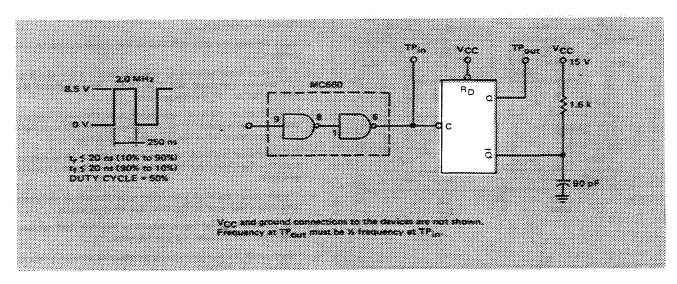
Pins not listed are left open



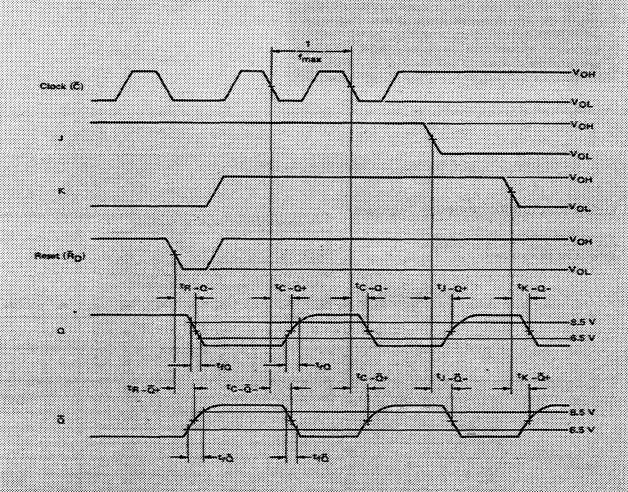


 $t_r \le 200 \text{ ns}$ $t_f \le 200 \text{ ns}$ $W \ge 200 \text{ ns}$

TOGGLE MODE TEST CIRCUIT



SWITCHING CHARACTERISTICS



		-30°E	25°C	+75°C	
Characteristic	Symbol	Typ	Men Typ	Typ Unit	•
Propagation Delay	98-Q-	55	- 60	66 es	
	₩-Ö+	150	- 180	210 ns	
	*C-Q+,*U-Q+	150	- 180	210 %	
	*c-äti-ä-	56	- 60	65 ns	
	tc-01x-0-	88	- 60	665 ns	
	10+0+1K+0+	150	- 180	210 ns	
Rise Time	40.4ä	35	- 36	40 rs	
Fall Time	110-110	5.0	- 5.0	4.0 ns	
Operating Frequency	\$max	4.0	20 40	3.0 484	

MC12663 - EXTENDED 12:15 VOLT SUPPLY **VOLTAGE OPERATION**

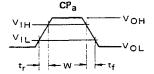
Most MC663 devices are operable at a V_{CC} as low as 12 volts, there are times when it is necessary to guarantee the 12 volt VCC Operation as well as certain maximum and minimum electrical characteristics. The MC12663 is guaranteed to meet both the standard MC563 electrical specifications and the 12 volt electrical characteristics.

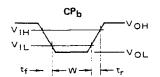
ELECTRICAL CHARACTERISTICS - MC12663

Unless otherwise noted, tests are shown for

only one flip-flop	mA				Vo	its			ļ						
ested in the same m						IOL	ІОН	VIL	VIH	٧F	VR	Vcc			
							-0.016	6.50	8.50	1.5	12	12			
		Pin	Test Limits -30 ≤T _A ≤+75°C 1			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:									
		Under			Unit		T	VIL	VIH	Ve	1-5	Vcc	CP _a	CPh	Gnd
Characteristic	Symbol	Test	Min	Max	Ome	lOL	юн	VIL	VIH	V F	V _R	1 000	O a	CPB	
Output Voltage	VOL	1 6	_	1 8 1 8	Vdc Vdc	1 6	-	2 5	3 5 2 3	<u>-</u>	- -	14 14	4		7 7
	Voн	1 1 6	11 0 11 0 11 0	- - -	Vdc Vdc Vdc	- - -	1 1 6	23 5 2	5 23 23	-	- - -	14 14 14	4 4 4	- -	7 7 7
Short Circuit Current	¹cs	1	-4 5	-12	mAdc		-	3 4	-	-	-	14	-	-	1 7
Reverse Current	I _R	2	-	20	μAdc	-	-	-	-	-	2	14	-	-	3 4 5 7
	31 _R	3	-	6.0	μAdc	-	-	-	-	-	3	24514	-	-	7
	21 _R	4	-	40	μAdc	-	-	-		-	4	14			2357
	^I R	5	-	20	μAdc	-	-	_	-	-	5	14	-	-	2347
Forward Current	1F	2	-0 55	-10	mAdc	-	-		-	2	-	14		4	7
	21 _F	3	-1 10	-20	mAdc	-	-	-	-	3	-	14	-	-	2 4 5
	151 _F	4	-0 80	-1 5	mAdc	~	-	_	-	4	-	2514	-	-	7
	ıF	5	-0 55	-10	mAdc	-	-	-	-	5	-	14	-	4	7
Power Drain Current	1CCL	14	-	12 5	mAdc	-	-	-		-	-	14	-	-	2345,79101112
Both Flip Flopsi	1ccH	14	-	12 5	mAdc	-	-	-	-		-	14	~	-	7

TEST CURRENT/VOLTAGE VALUES (All Temperatures)





 $t_r \le 200 \text{ ns}$ $t_{\rm f} \leq$ 200 ns W ≥ 200 ns

pins not listed are left open
Best results obtained if TA limited to 0°C to 75°C

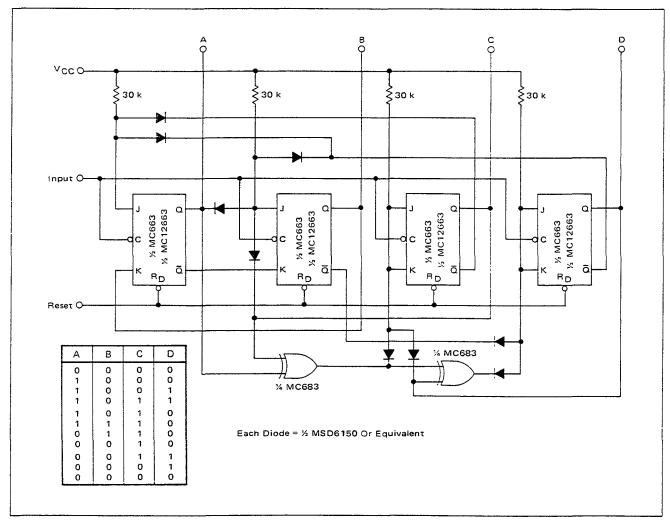
APPLICATIONS INFORMATION

The fact that the MC663/12663 may be used as either a synchronous (clocked) flip-flop or in the dynamic J-K mode lends a great deal of versatility to the device. Typical applications — as well as a description of operating principles — may be found in Application Note AN-414

The high degree of noise immunity inherent in MHTL allows the use of diode "AND" gating if desired with very little loss in performance A discrete 30 k Ω pull-up resistor

is recommended to charge the capacitance associated with the input and insure "one" state noise immunity. (The resistor adds 0.4 loads to the input loading factor.) The Gray-Code counter circuit below illustrates this technique. The discrete components in this counter may be replaced by three 2-input NAND gates, one 3-input NAND gate, and four inverters if desired

DECIMAL GRAY CODE COUNTER

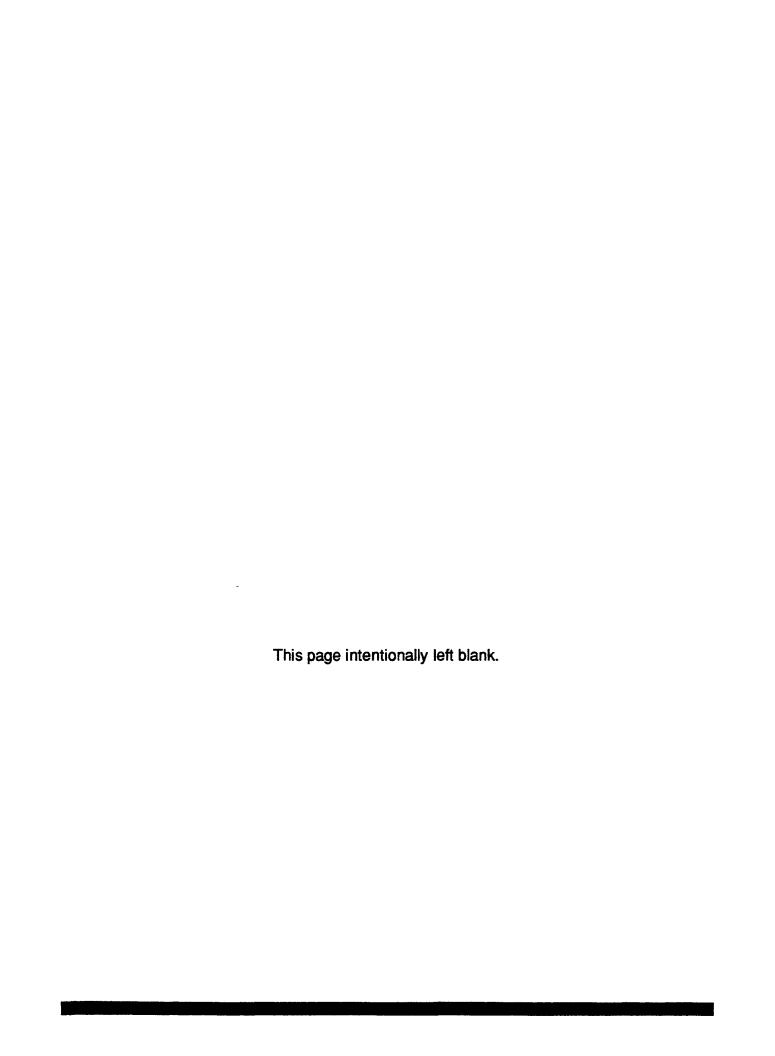


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