MC663
MC12663

ISSUE A
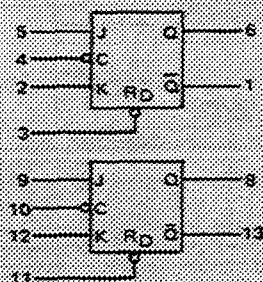

The MC663 and the MC12663 consist of two J-K flip-flops having direct reset inputs in addition to clocked inputs. The 15 volt V_{CC} device (MC663) and the extended 12-15 volt V_{CC} device (MC12663), are schematically indentical The MC12663 meets the MC663 specifications in addition to the 12 volt specifications. Both are available in the 14 pin dual-in-line plastic package (suffix P) and the 14 pin dual-in-line ceramic package (suffix L) A full temperature version of the MC663 dual-in-line ceramic is also available (suffix tL). This device meets the –30 to +75 standard specifications at –55 to +125 respectively

Input Loading Factor:
$\overline{R}_D$ input = 2
C input = 1.5
Other inputs = 1
Output Loading Factor = 9
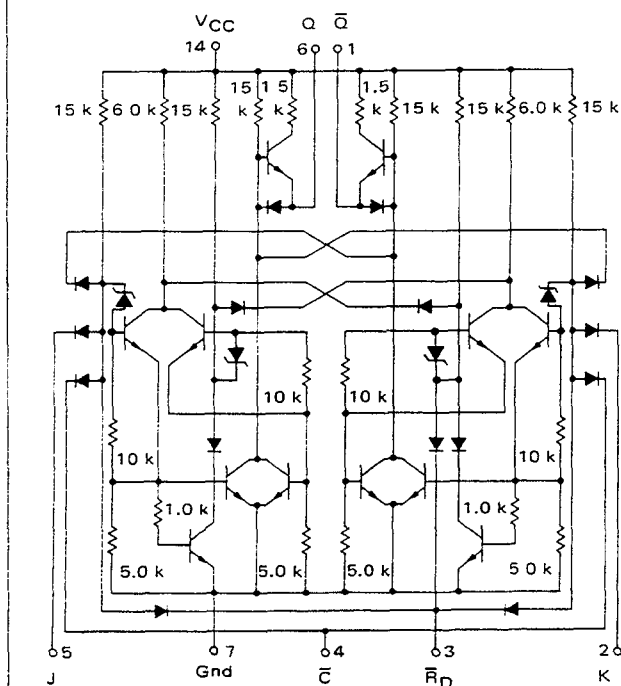f_{Tog} = 3.0 MHz typ
Total Power Dissipation = 200 mW typ

CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)

See General Information section for packaging

TRUTH TABLE

	t_n				t_{n+1}				
	J_n	K_n	$\overline{C}_n$	$\overline{R}_D$	J_{n+1}	K_{n+1}	$\overline{C_{n+1}}$	$\overline{R}_D$	Q_{n+1}
See Note e	0	0	X	1	X	X	X	1	Q_n
	1	0	1	1	1	0	0	1	1
	0	1	1	1	0	1	0	1	0
	1	1	1	1	1	1	0	1	$\overline{Q}_n$
See Note f	X	X	0	1	X	X	0	1	Q_n
	1	X	1	1	0	K_n	1	1	1
	X	1	1	1	J_n	0	1	1	0
	1	1	1	1	0	0	1	1	$\overline{Q}_n$
See Note g	X	X	X	1	X	X	X	0	0

a t_n refers to the time period immediately prior to an input transition. t_{n+1} applies to the time period after the transition.

b. J_n, K_n, etc., denotes the state of the input during the time period t_n; J_{n+1}, K_{n+1}, etc., denotes the state of the input during the time period t_{n+1}.

c. Q_{n+1} denotes the state achieved by the output during the time period t_{n+1}.

d A "0" at an input terminal denotes low state (–1.0 V to 6.5 V), "1" denotes high state (8.5 V to 18 V). An "X" means that either a "0" or "1" may be applied.

e. This portion of the truth table refers to synchronous (clocked) operation. Note that a "1" to "0" transition of the J or K input should not occur while the clock input ($\overline{C}$) is high.

f This portion of the truth table refers to dynamic J-K operation. Note that the clock input ($\overline{C}$) must remain high for this mode of operation.

g. This portion of the truth table refers to asynchronous operation. Note that a low level on $\overline{R}_D$ overrides all other inputs.

h. Rise (or fall) time of inputs should be less than 200 nanoseconds measured between 6.5 and 8.5 volts.

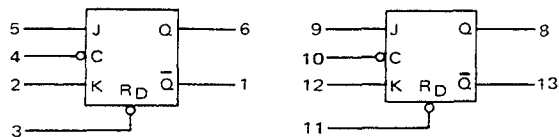j. Inputs which are not used should be returned through a resistor (2 kΩ-20 kΩ) to V_{CC}.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for
only one flip-flop. The other flip-flop is
tested in the same manner.

					TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
					mA		Volts									
					I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}				
					10.8	-0.027	6.50	8.50	1.5	16.0	14.0	16.0				

| | | Pin Under Test | MC663 Test Limits | | | | | | | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: | | | | | | | | | |
| | | | -30°C | | +25°C | | +75°C | | | | | | | | | | | | |
Characteristic	Symbol		Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}	CP_a	CP_b	Gnd
Output Voltage	V_{OL}	1	–	1.5	–	1.5	–	1.5	Vdc	1	–	2	3.5	–	–	14	–	4	–	7
		6	–	1.5	–	1.5	–	1.5	Vdc	6	–	5	2.3	–	–	14	–	4	–	7
	V_{OH}	1	–	–	12.5	–	12.5	–	Vdc	–	1	2,3	5	–	–	14	–	4	–	7
		1	–	–	12.5	–	12.5	–	Vdc	–	1	5	2.3	–	–	14	–	4	–	7
		6	–	–	12.5	–	12.5	–	Vdc	–	6	2	3.5	–	–	14	–	4	–	7
Short Circuit	I_{SC}	1	–	–	-6.5	-15	-6.5	-15	mAdc	–	–	3,4	–	–	–	–	14	–	–	1,7
Reverse Current	I_R	2	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	2	14	–	–	–	3,4,5,7
	$3I_R$	3	–	–	–	6.0	–	6.0	μAdc	–	–	–	–	–	3	2,4,5,14	–	–	–	7
	$2I_R$	4	–	–	–	4.0	–	4.0	μAdc	–	–	–	–	–	4	14	–	–	–	2,3,5,7
	I_R	5	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	5	14	–	–	–	2,3,4,7
Forward Current	I_F	2	–	–	–	-1.20	–	-1.20	mAdc	–	–	–	–	2	–	–	14	–	4	7
	$2I_F$	3	–	–	–	-2.40	–	-2.40	mAdc	–	–	–	–	3	–	–	14	–	–	2,4,5
	$1.5I_F$	4	–	–	–	-1.80	–	-1.80	mAdc	–	–	–	–	4	–	–	2,5,14	–	–	7
	I_F	5	–	–	–	-1.20	–	-1.20	mAdc	–	–	–	–	5	–	–	14	–	4	7
Power Drain Current (Both Flip-Flops)	I_{CCL}	14	–	–	–	16.7	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	2,3,4,5,7,9,10,11,12
	I_{CCH}	14	–	–	–	16.7	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	7

Pins not listed are left open
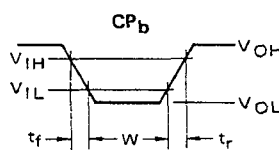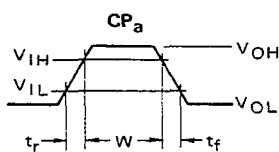
$t_r \leq 200$ ns
$t_f \leq 200$ ns
$W \geq 200$ ns

TOGGLE MODE TEST CIRCUIT
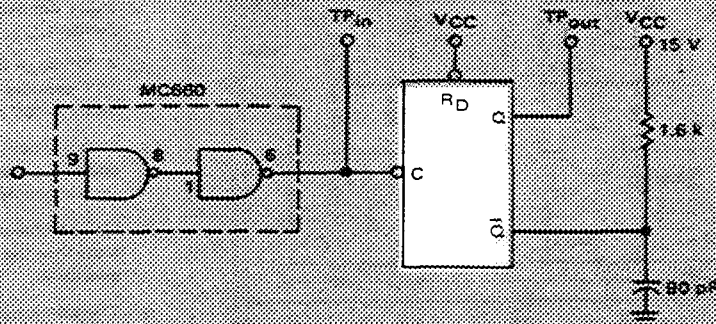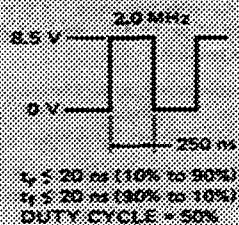
V_{CC} and ground connections to the devices are not shown.
Frequency at TF_{out} must be ½ frequency at TF_{in}.

SWITCHING CHARACTERISTICS
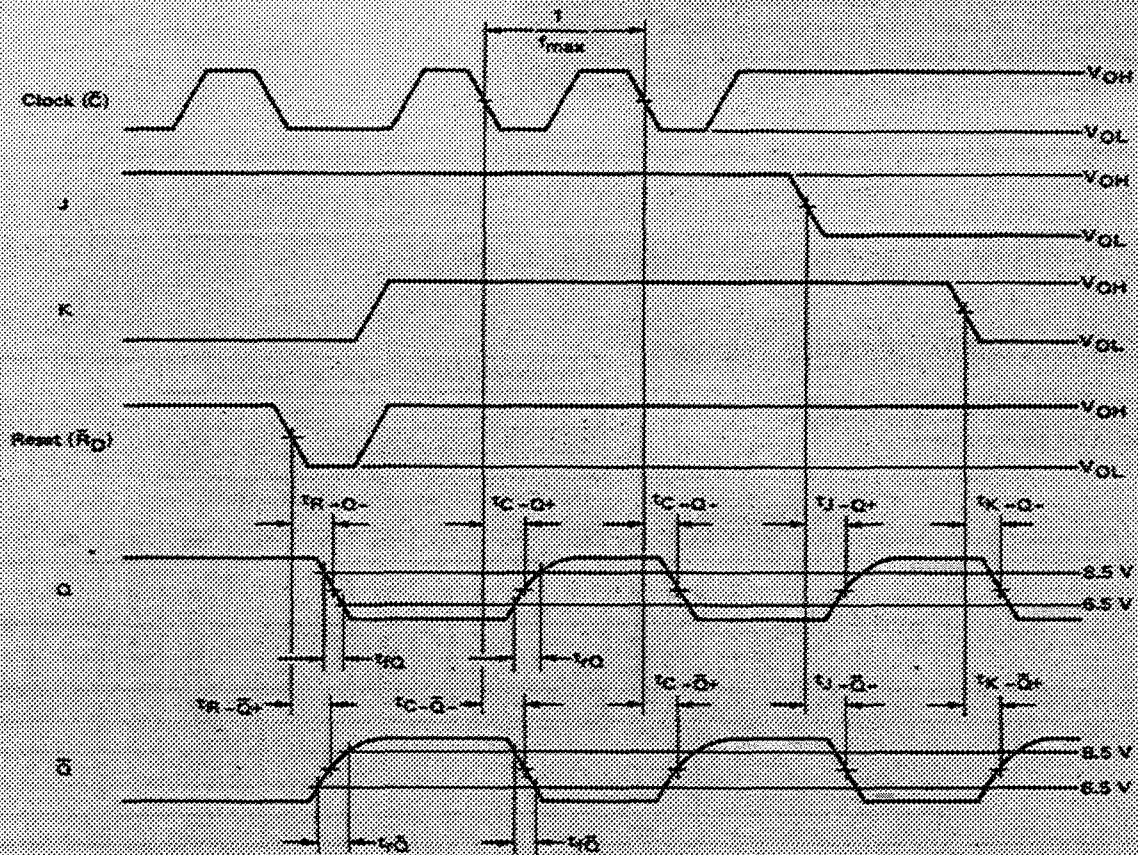
Characteristic	Symbol	-30°C	25°C		+75°C	Units
		Typ	Min	Typ	Typ	
Propagation Delay	t_{R-Q-}	55	—	60	65	ns
	$t_{R-\bar{Q}+}$	150	—	180	210	ns
	$t_{C-Q+},\ t_{J-Q+}$	150	—	180	210	ns
	$t_{C-\bar{Q}-},\ t_{J-\bar{Q}-}$	55	—	60	65	ns
	$t_{C-Q-},\ t_{K-Q-}$	55	—	60	65	ns
	$t_{C-\bar{Q}+},\ t_{K-\bar{Q}+}$	150	—	180	210	ns
Rise Time	$t_rQ,\ t_r\bar{Q}$	35	—	36	40	ns
Fall Time	$t_fQ,\ t_f\bar{Q}$	5.0	—	5.0	4.0	ns
Operating Frequency	f_{max}	4.0	2.0	4.0	3.0	MHz

ELECTRICAL CHARACTERISTICS – MC12663

Unless otherwise noted, tests are shown for only one flip-flop   The other flip-flop is tested in the same manner.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)						
mA			Volts			
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}
8.0	-0.016	6.50	8.50	1.5	12	12

Characteristic	Symbol	Pin Under Test	Test Limits $-30 \leq T_A \leq +75°C$ [1] Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	CP_a	CP_b	Gnd
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:									
Output Voltage	V_{OL}	1	–	18	Vdc	1	–	2	35	–	–	14	4	–	7
		6	–	18	Vdc	6	–	5	23	–	–	14	4	–	7
	V_{OH}	1	110	–	Vdc	–	1	23	5	–	–	14	4	–	7
		1	110	–	Vdc	–	1	5	23	–	–	14	4	–	7
		6	110	–	Vdc	–	6	2	23	–	–	14	4	–	7
Short Circuit Current	I_{CS}	1	-45	-12	mAdc	–	–	34	–	–	–	14	–	–	17
Reverse Current	I_R	2	–	20	μAdc	–	–	–	–	–	2	14	–	–	3 4 5 7
	$3I_R$	3	–	60	μAdc	–	–	–	–	–	3	2 4 5 14	–	–	7
	$2I_R$	4	–	40	μAdc	–	–	–	–	–	4	14			2 3 5 7
	I_R	5	–	20	μAdc	–	–	–	–	–	5	14	–	–	2 3 4 7
Forward Current	I_F	2	-055	-10	mAdc	–	–	–	–	2	–	14	–	4	7
	$2I_F$	3	-110	-20	mAdc	–	–	–	–	3	–	14	–	–	2 4 5
	$15I_F$	4	-080	-15	mAdc	–	–	–	–	4	–	2 5 14	–	–	7
	I_F	5	-055	-10	mAdc	–	–	–	–	5	–	14	–	4	7
Power Drain Current	I_{CCL}	14	–	125	mAdc	–	–	–	–	–	–	14	–	–	2 3 4 5,7 9 10 11 12
(Both Flip Flops)	I_{CCH}	14	–	125	mAdc	–	–	–	–	–	–	14	–	–	7

Pins not listed are left open
[1] Best results obtained if T_A limited to 0°C to 75°C
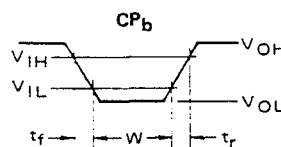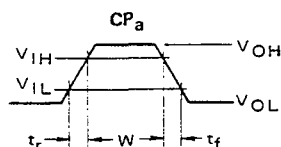
$t_r \leq 200$ ns
$t_f \leq 200$ ns
$W \geq 200$ ns

The fact that the MC663/12663 may be used as either a synchronous (clocked) flip-flop or in the dynamic J-K mode lends a great deal of versatility to the device. Typical applications — as well as a description of operating principles — may be found in Application Note AN-414

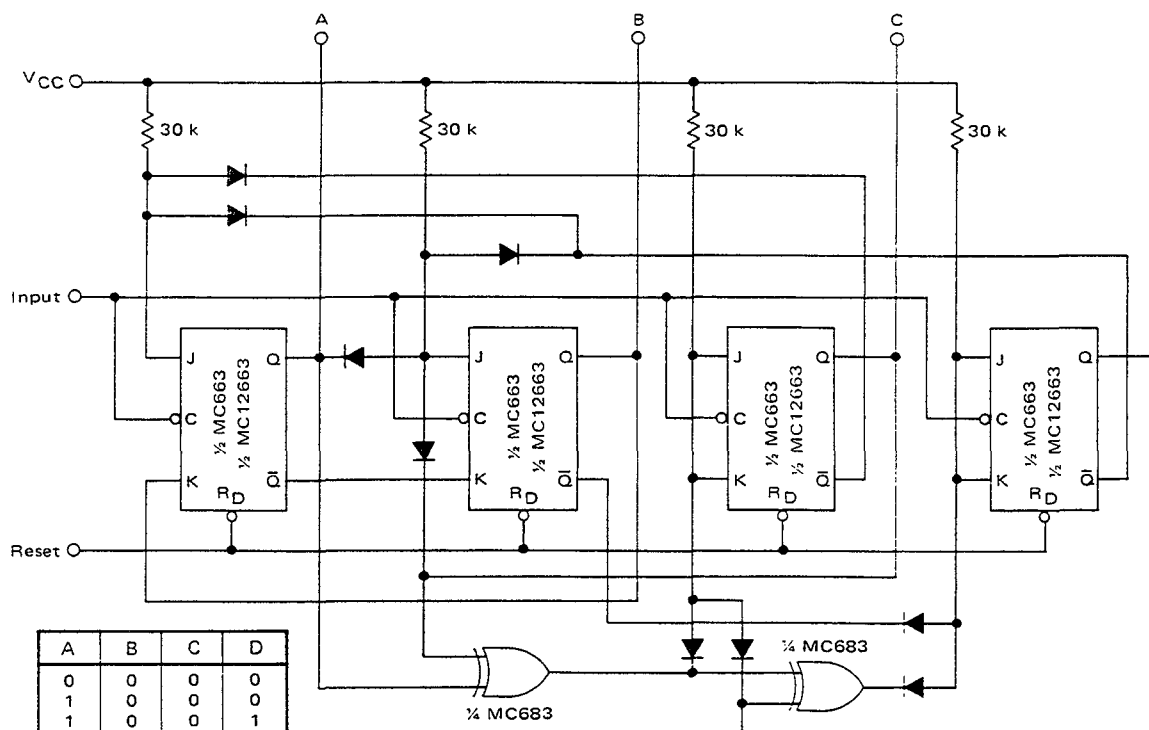The high degree of noise immunity inherent in MHTL allows the use of diode "AND" gating if desired with very little loss in performance   A discrete 30 kΩ pull-up resistor is recommended to charge the capacitance associated with the input and insure "one" state noise immunity. (The resistor adds 0.4 loads to the input loading factor.)   The Gray-Code counter circuit below illustrates this technique. The discrete components in this counter may be replaced by three 2-input NAND gates, one 3-input NAND gate, and four inverters if desired

DECIMAL GRAY CODE COUNTER

A	B	C	D
0	0	0	0
1	0	0	0
1	0	0	1
1	0	1	1
1	0	1	0
1	1	1	0
0	1	1	0
0	0	1	0
0	0	1	1
0	0	0	1
0	0	0	0

Each Diode = ½ MSD6150 Or Equivalent

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MC663/D