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SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC6108

Advance Information

8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

The MC6108 is a microprocessor compatible, 8-bit, high speed analog-to-digital converter. Included are a precision reference, DAC, comparator, SAR, matched scale resistors, 3-state output buffers, and control logic. Conversion can be completed in under 2.0 μs and input voltage ranges of 0 to +10 V, 0 to +5.0 V, and −5.0 to +5.0 V can be converted without additional external components. With appropriate external resistors, the converter can accommodate other input voltage ranges. 8-bit linearity and monotonic operation with no missing codes are guaranteed over temperature. Bus compatibility is provided for by the 3-state outputs (latches not required).

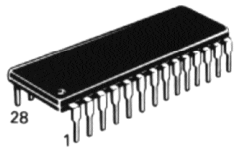
The MC6108 conversion time is short enough to allow most microprocessors to accept the data immediately after requesting a conversion. Applications include process control systems, servo control systems, waveform storage, signal processing, and others.

This device is functionally and pin compatible with the AM6108.

- 1.8 μs Conversion Time (Guaranteed)
- Microprocessor Compatible — Connect Directly to Data Bus
- Trimmed Internal Voltage Reference
- 0.1% Nonlinearity (Typ)
- Low Operating Voltage (+5.0 V, −5.2 V)
- Internal Matched Gain, Reference, and Offset Resistors
- Pin Programmable Natural Binary or Two's Complement
- Conversion Complete Available as Interrupt or on Data Bus
- Max Power Dissipation — 415 mW

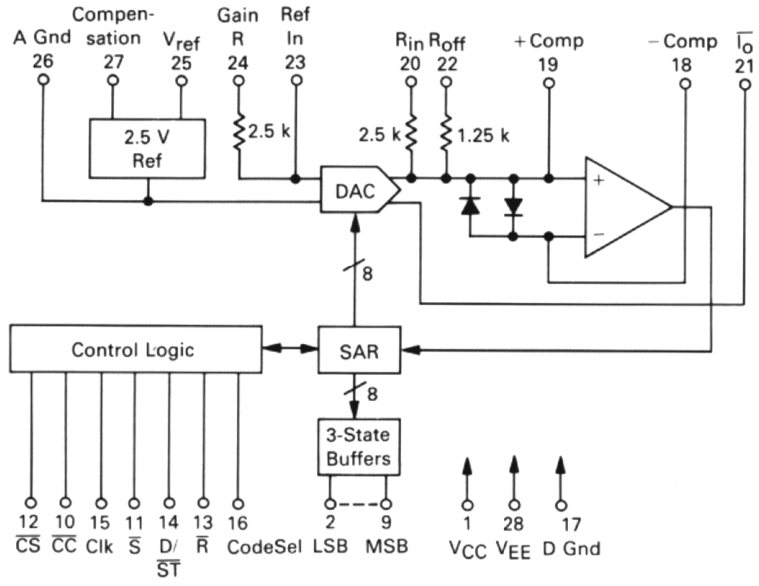
8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

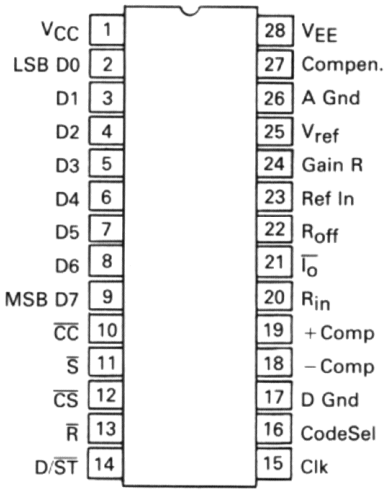


P SUFFIX
PLASTIC PACKAGE
CASE 710-02

BLOCK DIAGRAM



PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI1328
(Replacing NP175)

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to D. Gnd except where noted)

Parameter	Value	Units
V_{CC} (Pin 1)	−0.3, +7.0	V
V_{EE} (Pin 28)	+0.3, −7.0	V
Max Differential ($V_{CC} - V_{EE}$)	12	V
Digital Inputs (Pins 11–16)	−0.5, +6.0	V
A. Gnd (Pin 26)	±1.0	V
Input Current @ Ref In, Gain R	3.0	mA
Voltage @ Gain R	V_{CC}, V_{EE}	V
Voltage @ R_{in}, R_{off}	±12	V
Voltage @ +Comp, −Comp, $\overline{I_O}$	−2.5, +12	V
Voltage @ D0–D7 (in 3-state mode)	−0.5, +6.0	V
Junction Temperature	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

(Voltages referred to D. Gnd except where noted)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{EE}	−5.46	−5.2	−4.94	V
Analog Ground	AGnd	−0.1	0	0.1	V
V_{ref} Current	I_{Vref}	0	—	5.0	mA
Voltage @ Gain R	—	1.25	2.5	5.0	V
Ref In Current	I_{ref}	0.5	1.0	2.0	mA
Voltage @ R_{in}	V_{in}	−8.0	—	10	V
Voltage @ R_{off}	V_{off}	−8.0	—	10	V
Clock Frequency	f_{clk}	0	—	5.0	MHz
Voltage @ −Comp	—	0	0	4.0	V
Voltage @ $\overline{I_O}$	—	−1.0	0	+5.0	V
Digital Input Voltage	—	0	—	5.25	V
Ambient Temperature	T_A	0	—	+70	°C

TRANSFER CHARACTERISTICS (V_{CC} = +5.0 V, ±5.0%, V_{EE} = −5.2 V, ±5.0%, 0 < T_A < 70°C, Clk = 5.0 MHz, V_{ref} connected to Gain R, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units
Resolution	Res	8.0	—	8.0	Bits
Monotonicity	Mon	GUARANTEED			
Differential Non-Linearity	DNL	—	±1/4	±3/4	LSB
Integral Non-Linearity (Unipolar)	INLU	—	±1/4	±1/2	LSB
Integral Non-Linearity (Bipolar)	INLB	—	±1/4	±3/4	LSB
Unipolar Gain Error (V_{in} = 0 to +5.0 V @ Pin 22)	UGER	—	—	±2-1/2	LSB
Unipolar Gain Error (V_{in} = 0 to +10 V @ Pin 20)	UGER	—	—	±2-1/2	LSB
Unipolar Offset Error (D7–D0 = 00_H to 01_H)	UOFF	—	—	±1.0	LSB
Bipolar Gain Error (V_{in} = −5.0 to +5.0 V @ Pin 20)	BGER	—	—	±2-1/2	LSB
Bipolar Zero Error (D7–D0 = $7F_H$ to 80_H)	BZER	—	—	±1-1/2	LSB
Bipolar Offset Error (D7–D0 = 00_H to 01_H)	BOFF	—	—	±2-1/2	LSB

TRANSFER CHARACTERISTICS (continued)

Parameter	Symbol	Min	Typ	Max	Units
I_o Full Scale Current (D7–D0 = FF_H, T_A = 25°C) (See Text "DAC")	I_{FS}	3.1	3.992	4.9	mA
$\overline{I_o}$ Zero Scale Current (D7–D0 = FF_H, T_A = 25°C) (See Text "DAC")	$\overline{I_{ZS}}$	−5.0	—	+5.0	μA
I_o Zero Scale Current (D7–D0 = 00_H, T_A = 25°C) (See Text "DAC")	I_{ZS}	3.0	7.8	13	μA
$\overline{I_o}$ Full Scale Current (D7–D0 = 00_H, T_A = 25°C) (See Text "DAC")	$\overline{I_{FS}}$	3.1	3.984	4.9	mA
DAC Current Gain (See Text "DAC")	G_{DAC}	3.92	4.0	4.08	—
Gain Sensitivity to V_{CC} Variations ($4.75 < V_{CC} < 5.25$ V, V_{EE} = −5.2 V)	$PSSV_{CC}$	—	±0.01	±0.2	%FS
Gain Sensitivity to V_{EE} Variations ($-5.46 < V_{EE} < -4.94$ V, V_{CC} = +5.0 V)	$PSSV_{EE}$	—	±0.02	±0.2	%FS

INTERNAL REFERENCE SUPPLY

Pin 25 Voltage ($I_{ref} \approx -1.0$ mA, V_{CC} = +5.0, V_{EE} = −5.2)	V_{ref}	2.475	2.5	2.525	V
Temperature Coefficient	T_C	—	±20	—	ppm/°C
Load Regulation (-1.0 mA $< I_{ref} < -5.0$ mA)	Reg_{load}	—	±0.05	±0.2	$\%V_{ref}$
Line Regulation ($4.75 < V_{CC} < 5.25$ V)	Reg_{line}	—	±0.02	±0.2	$\%V_{ref}$
Noise (f_n = 10 kHz to 1.0 MHz, T_A = 25°C)	—	—	20	—	μV_{rms}
Short Circuit Current (T_A = 25°C)	IRSC	−30	−20	−5	mA
POWER SUPPLIES					
V_{CC} Current (Outputs unloaded)	I_{CC}	5.0	20	27	mA
V_{EE} Current (Outputs unloaded)	I_{EE}	−50	−38	−5	mA
Power Dissipation (Outputs unloaded)	P_D	—	300	415	mW
ANALOG INPUTS (T_A = 25°C)					
Input Resistance @ Gain R (Pin 24)	R_{GR}	—	2.5	—	kΩ
Input Resistance @ R_{in} (Pin 20)	R_{RI}	1.75	2.5	3.25	kΩ
Input Resistance @ R_{off} (Pin 22)	R_{RO}	—	1.25	—	kΩ
Reference Input Offset Voltage (Pin 23–26)	Ref_{off}	−10	—	+10	mV
Comparator Input Clamp Voltage (4.0 mA through the back-to-back diodes)	V_{clamp}	±0.4	±0.8	±1.3	V
Input Capacitance @ +Comp (Pin 19)	C_C	—	20	—	pF
Input Capacitance @ $\overline{I_o}$ (Pin 21)	C_I	—	10	—	pF
Input Capacitance @ R_{in}, R_{off}, Ref In, Gain R, −Comp.	—	—	2.0	—	pF
DIGITAL INPUTS					
Input Voltage — High (Pins 11–16)	V_{IH}	2.0	—	5.25	V
Input Voltage — Low (Pins 11–16)	V_{IL}	0	—	0.8	V
Input Current @ 4.0 V (Pins 11–16)	I_{IH}	—	—	10	μA
Input Current @ 0 V (Pins 11–16)	I_{IL}	—	—	10	μA
DIGITAL OUTPUTS					
Output Voltage — High (I_{OH} = −400 μA, Pins 2–10)	V_{OH}	2.4	3.2	—	V
Output Voltage — Low (I_{OL} = 8.0 mA, Pins 2–10)	V_{OL}	—	0.15	0.4	V
Short Circuit Current* (Pins 2–10, T_A = 25°C)	I_{SC}	−50	−25	—	mA
Three-State Leakage (V_O = 2.4 V, Pins 2–9) (V_O = 0.4 V, Pins 2–9)	I_{HLK} I_{LLK}	−20 −20	— —	+20 +20	μA
Capacitance (3-State Mode, Pins 2–9)	C_O	—	7.0	—	pF

*Short circuits should be limited to 1.0 second max, 1 output at a time.
Note: Currents into a pin designated as +, currents out of a pin designated as −.

TIMING CHARACTERISTICS (T_A = 25°C, See System Timing Diagram)

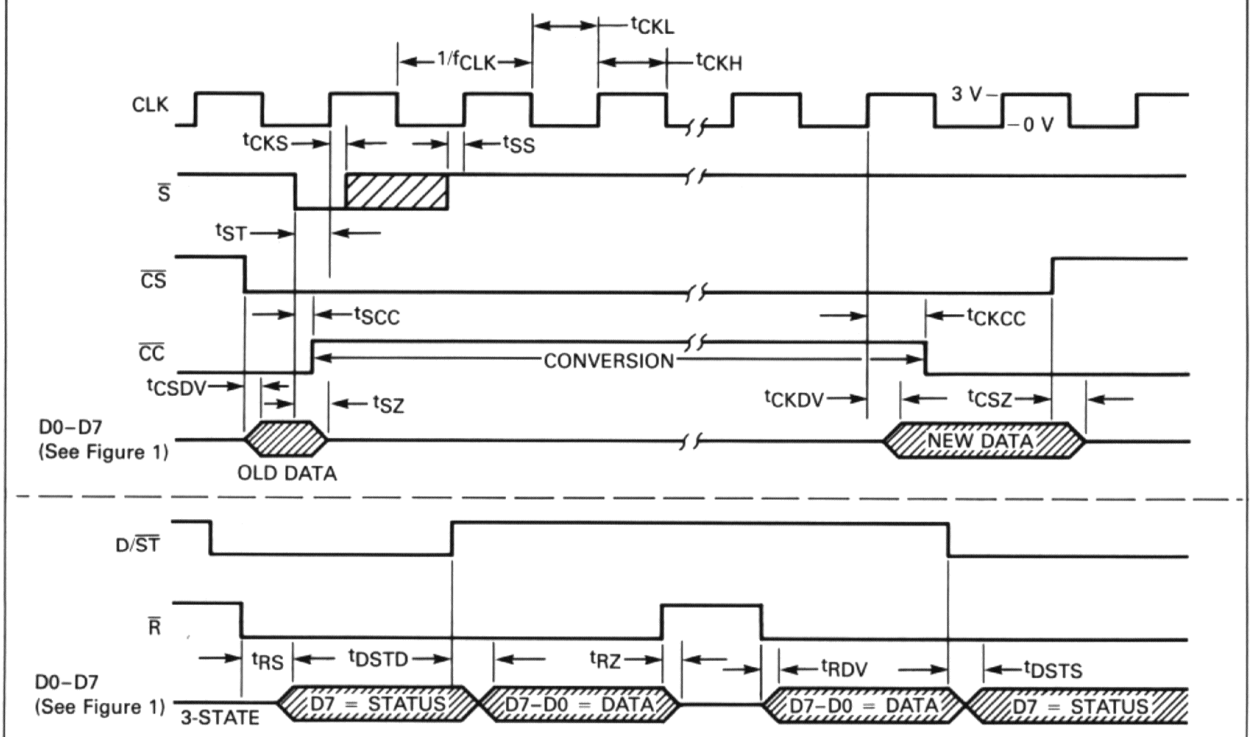
Parameter	Symbol	Min	Typ	Max	Units
INPUTS					
$\overline{S}$ High After CLK High*	t_{CKS}	0	—	—	ns
$\overline{S}$ High Before CLK High*	t_{SS}	25	—	—	ns
CLK Low Time	t_{CKL}	50	—	—	ns
CLK High Time	t_{CKH}	50	—	—	ns
CLK Rise, Fall Time	t_r, t_f	—	—	100	ns
$\overline{CS}$, CLK, $\overline{S}$ Concurrent Low Time*	t_{ST}	50	—	—	ns
Clock Frequency	f_{CLK}	—	—	5.0	MHz

*See text (Sequence of Operation)

OUTPUTS					
$\overline{CC}$ High from $\overline{S}$, $\overline{CS}$, or CLK Low	t_{SCC}	—	25	55	ns
Data to 3-State from $\overline{S}$, and CLK Low**	t_{SZ}	—	25	55	ns
$\overline{CC}$ Low from CLK High	t_{CKCC}	—	15	40	ns
Data Valid from CLK High**	t_{CKDV}	—	25	50	ns
Data Valid from $\overline{CS}$ Low**	t_{CSDV}	—	25	40	ns
Data to 3-State from $\overline{CS}$ High**	t_{CSZ}	—	20	40	ns
Data Valid from $\overline{R}$ Low**	t_{RDV}	—	20	40	ns
Data to 3-State from $\overline{R}$ High**	t_{RZ}	—	20	40	ns
D7 to Status from D/$\overline{ST}$ Low**	t_{DSTS}	—	20	40	ns
D7 to Data from D/$\overline{ST}$ High**	t_{DSTD}	—	20	40	ns
D7 to Status from $\overline{R}$ Low**	t_{RS}	—	20	40	ns

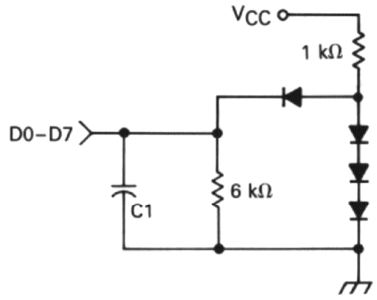
**See Figure 1 for output conditions

SYSTEM TIMING DIAGRAM

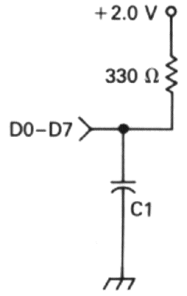


NOTE: D0–D7 timing measured at 2.0 and 0.8 volts when testing active outputs, and at 0.35 volts below V_{OH} and 0.35 volts above V_{OL} when entering 3-state mode.

FIGURE 1 — DATA OUTPUT LOAD TEST CIRCUIT



Active Outputs



Outputs To 3-State From Active

Diodes = 1N914 or equivalent
C1 = 125 pF (total)

TEMPERATURE SPECIFICATIONS ($0° < T_A < 70°$ C)

Function	Pin	Typical Change	Units
V_{ref}	25	±20	ppm/°C
DAC Current Gain	—	±8.0	ppm/°C
$\overline{I_O}$ Dynamic Impedance	21	+1.1	%/°C
Reference Input Offset	23–26	±20	μV/°C
Resistance @ R_{in}, R_{off}, Gain R	20,22,24	+0.1	%/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
V_{CC}	1	To be connected to a 5.0 volts (±5.0%) supply.
D0–D7	2–9	TTL level data outputs capable of three-state mode. Pin 2 is the LSB, Pin 9 is the MSB. Pin 9 can also indicate conversion status.
$\overline{CC}$	10	Conversion Complete. TTL level output. High indicates conversion in progress, low indicates conversion complete and valid data at the outputs. This output does not have three-state capability.
$\overline{S}$	11	Start conversion — TTL Input. Taking $\overline{S}$ low (with Clock and Chip Select low) resets the SAR. Taking $\overline{S}$ high allows the conversion to start.
$\overline{CS}$	12	Chip Select — TTL Input. When low, a conversion may be initiated or data read at the outputs. When high, data outputs are in the three-state mode, and other digital inputs are ignored.
$\overline{R}$	13	Read — TTL Input. When low, data may be read at D0–D7. When high, D0–D7 are in three-state condition.
D/$\overline{ST}$	14	Data/$\overline{Status}$ — TTL Input. When high, D0–D7 provide normal data. When low, D7 indicates "Conversion Complete" status, while D0–D6 are in three-state mode.
CLK	15	Clock — TTL Input. 0–5.0 MHz.
CodeSel	16	Code Select — TTL Input. When low, output data is in 2's complement format. When high, output data is straight binary (offset binary when used in the bipolar mode).
D. Gnd	17	Digital Ground. Connect to ground associated with digital side of the circuitry.
−Comp	18	Negative input of the comparator. Normally grounded, a voltage on this pin will provide an offset of the input voltage range.
+Comp	19	Positive input of the comparator. Normally open, this pin may be used for input voltage ranges other than 0–10 volts, or ±5.0 volts.
R_{in}	20	The voltage to be converted to a digital equivalent is normally applied to this pin. A nominal 2.5 kΩ resistor is internally connected from this pin to the comparator/DAC output node.
$\overline{I_O}$	21	Current flows into this pin, complementary in value to the DAC's normal current output (I_O). Normally grounded, it may be connected to a resistor to ground or a positive voltage source in order to provide an analog output.

PIN DESCRIPTIONS — continued

Symbol	Pin	Description
R_{off}	22	An input for the bipolar offset function. This input can also serve as an alternate voltage input with half the range at R_{in}. A nominal 1.25 kΩ resistor is internally connected from this pin to the comparator/DAC output node. When not used this pin should be grounded.
Ref In	23	DAC's reference input. Reference current may be supplied to the DAC through this pin rather than through Pin 24. The DAC's full scale current is 4x the reference current. Source impedance should be less than 10 kΩ.
Gain R	24	Normally 2.5 volts (from pin 25) is applied to this pin to supply the 1.0 mA reference current to the DAC. An internal 2.5 kΩ resistor connects this pin to the DAC's reference input.
V_{ref}	25	Output of the internal precision 2.5 volt reference supply, it can supply up to 5.0 mA. Normally used to supply the DAC's reference current and the bipolar offset current.
A. Gnd	26	Analog Ground. Connect to ground associated with the analog side of the circuitry.
Compen	27	Compensation for the reference supply regulator. Typically, a 0.01 μF capacitor is connected from this pin to A. Gnd or to V_{EE}.
V_{EE}	28	To be connected to a −5.2 volts (±5.0%) supply.

DESIGN GUIDELINES

ANALOG SECTION

DAC (Refer to Figures 2 and 3)

The DAC generates an output current (I_o) which is proportional to both the reference current and the digital input presented to it by the Successive Approximation Register (SAR), according to the following formula:

$$I_o = \frac{I_{ref} \times 4 \times A}{256} + I_{zs} \qquad (1)$$

where A is the binary digital code (0–255), and I_{zs} is the zero scale current. I_o flows ***into*** the DAC, never out. The 4x (±2.0%) factor is a current gain built into the DAC. For a nominal I_{ref} of 1.0 mA, the maximum I_o (@A = 255) is 3.992 mA (which includes an I_{zs} of 7.8 μA). I_{zs} is built in so the first transition occurs when the signal voltage (V_{in}) is 1/2 LSB above its minimum value. In normal operation, I_o is supplied from the signal voltage that is being converted to a digital code. Therefore, the signal source must be capable of supplying up to 4.0 mA in the unipolar mode. I_{ref} is the reference current flowing in through either pin 23 or 24. See Figure 2 for the basic unipolar configuration.

In the bipolar mode, an offset current of 2.0 mA is supplied to the I_o node (normally through R_{off}) in order that V_{in} may be symmetrical about zero volts. The signal source must be capable of sinking 2.0 mA when at the negative extreme, and sourcing 2.0 mA when at the positive extreme. See Figure 3 for the basic bipolar configuration.

+Comp (Pin 19) is maintained close to a virtual ground after a conversion as long as −Comp (Pin 18) is at ground. The voltage at +Comp varies (nominally ±0.8 volts) during a conversion as the DAC forces different current values at I_o and will end up close to zero at the end of a conversion. Because of the varying voltage at +Comp, the current from the signal source and the offset source (if used) will vary with each step of the successive approximation sequence, necessitating that the signal source have a dynamic impedance less than

$$\frac{V_1 \times R_X}{1.6\ V} \qquad (2)$$

where V_1 = 1/2 LSB of the signal voltage, and
R_X = Resistance between the signal source and Pin 19
(2.5 kΩ if using R_{in}, 1.25 kΩ if using R_{off}).

Normally Pin 19 is left open, although it may be used as a path for the offset current, or the signal current (to be digitized), with appropriate external resistors. See the Applications Information for more details.

I_{ref} flows ***into*** the DAC, never out, and should be between 0.5 mA and 2.0 mA to preserve linearity and accuracy. Linearity specified in the Electrical Characteristics is tested @ I_{ref} of ≈1.0 mA. The reference input stage is depicted in Figure 4. Normally I_{ref} is supplied by the MC6108's internal 2.5 volt reference (Pin 25) through Gain R (Pin 24). If a separate voltage source is used for the reference current, it must be free of noise, spikes, and ripple since the accuracy of a conversion is directly related to the quality and stability of the reference.

SIGNAL VOLTAGE

The input signal voltage (to be digitized) is applied to either R_{in}, R_{off}, or through an appropriate external resistor to +Comp, such that current from the signal source flows into the DAC's I_o port. The preset ranges, with V_{ref} connected to Gain R are as follows:

Input Range	Connect R_{in} to	Connect R_{off} to
0 to +10 V	V_{in}	A. Gnd
0 to +5.0 V	A. Gnd	V_{in}
−5.0 to +5.0 V	V_{in}	V_{ref}

FIGURE 2 — BASIC UNIPOLAR CONFIGURATION

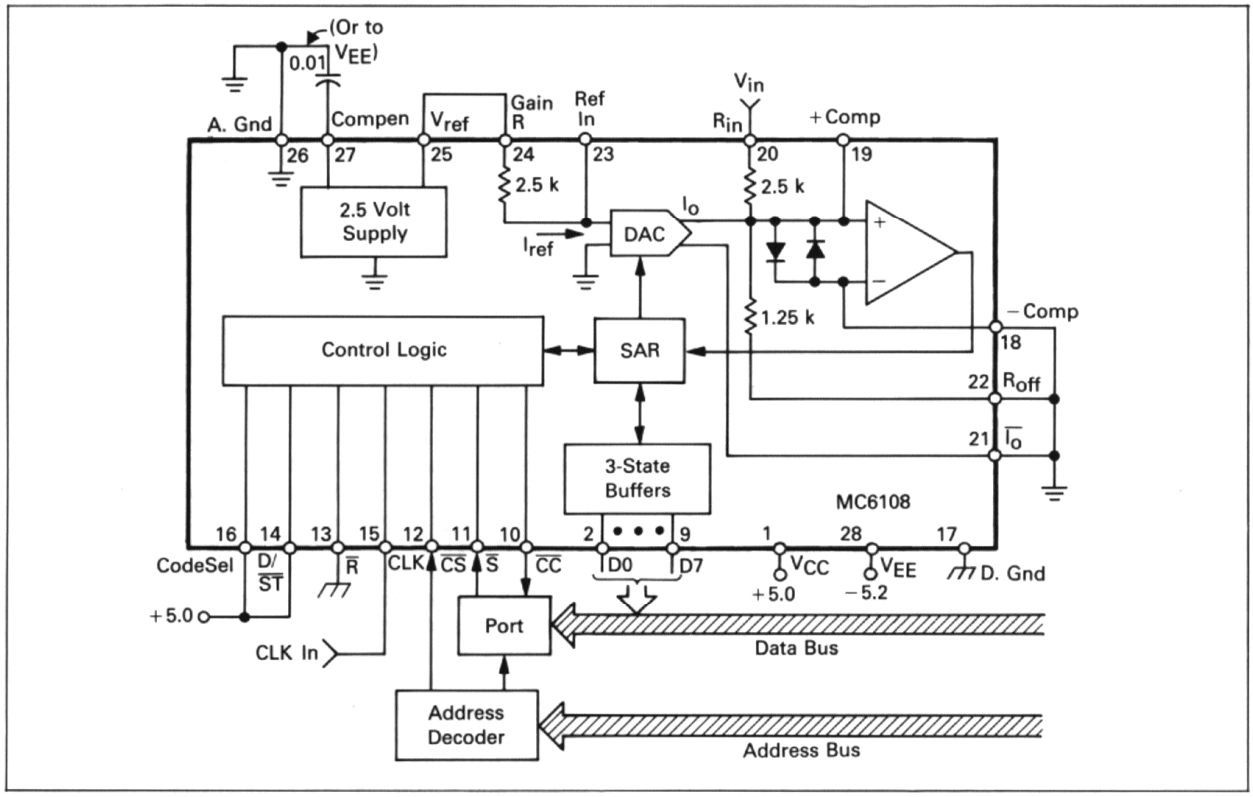


FIGURE 3 — BASIC BIPOLAR CONFIGURATION

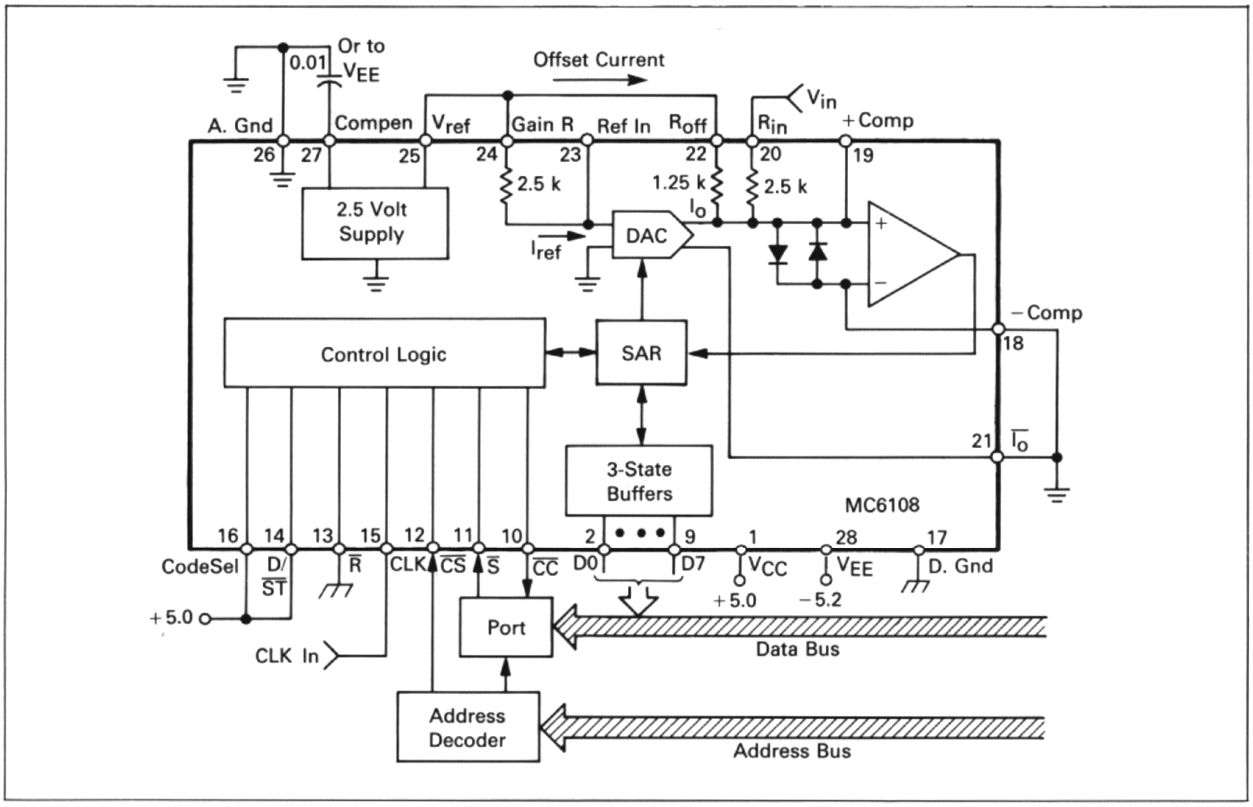
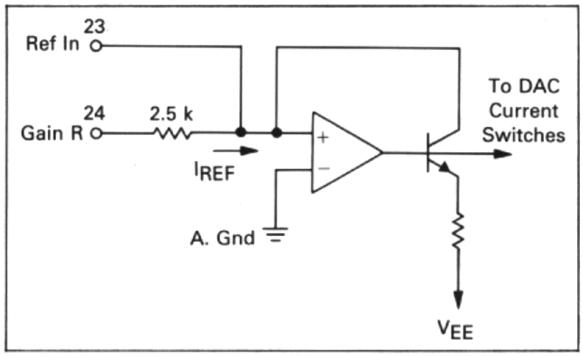


FIGURE 4 — REFERENCE AMPLIFIER



Although the tolerance on the absolute values of the resistors at Gain R, R_{in}, and R_{off} is $\approx \pm 30\%$, the ***ratio*** of their values is accurately controlled. Due to this fact, when the MC6108 is connected for any of the above mentioned ranges, the conversion accuracy is assured.

The voltage being digitized must be steady to within $\pm 1/2$ LSB during a conversion cycle in order to get an accurate representation of that voltage. The maximum slew rate during the conversion is defined by:

$$\frac{V_{range}}{2 \times 256 \times t_{CONV}} = \frac{V_{range} \times f_{CLK}}{2 \times 256 \times 9} = \frac{V_{range} \times f_{CLK}}{4608} \quad (3)$$

where Vrange = range of the input voltage;
t_{CONV} = conversion time (min. 9 clock cycles); and
f_{CLK} = clock frequency.

For a typical input range of 10 volts, and a clock frequency of 5.0 MHz, the maximum input slew rate is 0.0108 V/μs. The maximum sine-wave frequency which can be digitized without using a sample-and-hold is:

$$\frac{f_{CLK}}{4608 \times \pi} \quad (4)$$

The above equation assumes the signal's peak-to-peak voltage is equal to the input range of the MC6108. If the input signal will change more than 1/2 LSB during a conversion, a sample-and-hold is then needed at the input. With the use of a sample-and-hold, the maximum frequency which can be accurately digitized is 1/2 the conversion frequency, (277.78 kHz with an f_{CLK} of 5.0 MHz).

The dynamic impedance requirements of the signal source are discussed in the DAC section.

– COMP

Pin 18 is normally grounded, resulting in + COMP (Pin 19) being close to a virtual ground at the end of a conversion. However, this pin may be used as an alternate means of offsetting the input range. Applying a positive voltage to – COMP shifts the input voltage range in a positive direction.

The amount of the input's shift depends not only on the voltage applied to – COMP, but also on the impedances between the I_o node and the input source and ground. For example, if the signal voltage applied to R_{in}, and R_{off} is at ground (+ COMP open), the input range shifts 3 volts for each volt applied to – COMP.

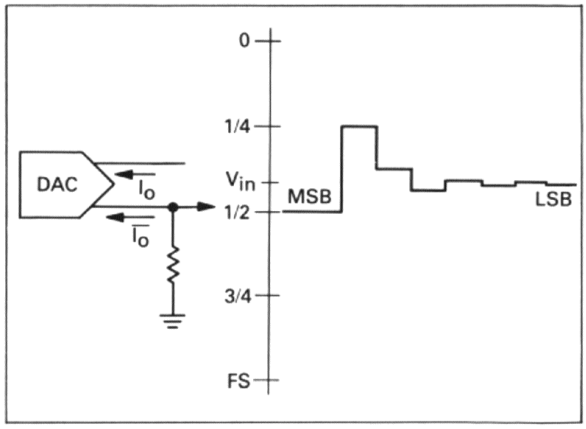
Since a portion of the DAC's I_o current will be drawn from the voltage at – COMP, that voltage source must be capable of supplying ± 2.0 mA, and must have a low dynamic impedance. The voltage at – COMP, R_{in}, and R_{off} must be kept within the limits listed in the Recommended Operating Conditions.

$\overline{I_o}$

$\overline{I_o}$ (Pin 21) is the DAC's complementary current output. The current at this pin changes opposite to that at I_o such that their sum is a constant value [4 x I_{ref}]. Current flow is ***into*** the pin.

In most applications, this pin is grounded. However, connecting this pin to a resistor to ground permits monitoring the steps of the SAR(see figure 5), or obtaining an analog output representative of the input voltage. The steps in Figure 5 indicate how the circuit finds the value of $\overline{I_o}$, representative of V_{in}, by successively trying each bit, and leaving each bit on or off (a conversion always starts with the MSB on). The voltage at $\overline{I_o}$ will swing negative, and is limited to – 1.0 volt (max resistor value is 250 Ω). To get a wider voltage swing, a larger resistor may be connected to a pull-up voltage (+ 5.0 volts max). For example, using a 1.25 kΩ resistor pulled up to + 5.0 volts results in this pin swinging between ground and + 5.0 volts. The output dynamic impedance of the $\overline{I_o}$ current source (when $\overline{I_o}$ is maximum) is $\approx$ 2.0 MΩ for applied voltages of – 1.0 to + 4.0 V, and is $\approx$50 kΩ for applied voltages > + 4.0 V, and tends to increase as the nominal value of $\overline{I_o}$ decreases.

FIGURE 5 — SUCCESSIVE APPROXIMATION STEPS AT $\overline{I_o}$



At the end of a conversion, $\overline{I_o}$ produces a spike approximately 40 ns wide which starts with the falling edge of $\overline{CC}$. The spike's amplitude varies from $\approx$1.0 mA (@ V_{in} = 0) to 0 mA (@ V_{in} = max). After the spike, $\overline{I_o}$ remains at the final current value until the start of the next conversion. The current value, once established, is independent of the inputs at $\overline{R}$, D/$\overline{ST}$, CodeSel, and $\overline{CS}$.

REFERENCE SUPPLY

The internal bandgap reference produces an output of +2.500 volts, ±25 mV (@ V_{ref}, pin 25), and is primarily intended to supply the reference current and the bipolar offset current. The output impedance is typically <0.5 Ω for load currents up to 5.0 mA, and increases rapidly at higher currents. Variations in V_{ref} are typically < 0.5 mV as V_{CC} is varied from +4.75 to +5.25 volts, and V_{ref} is independent of V_{EE} variations. The output is designed to source, not sink current.

A 0.001 μF capacitor from V_{ref} to A. Gnd is recommended to reduce noise on this output produced by the digital section. A 0.01 μF capacitor from the Compensation pin (Pin 27) to A. Gnd, or to V_{EE}, is necessary to stabilize the regulator.

POWER SUPPLIES

The power supplies are to be +5.0 volts, ±5.0% at V_{CC} (Pin 1), and −5.2 volts, ±5.0% at V_{EE} (Pin 28). For proper operation, bypassing is required for both supplies ***at the IC.*** 10 μF tantalum in parallel with 0.01 μF ceramic is recommended for each supply.

I_{CC} varies with the chip's different operating conditions, and is a maximum (typically 20 mA) during a conversion ($\overline{R}=0$, $D/\overline{ST}=1$, $\overline{CS}=0$) with the signal voltage at its minimum value. Minimum I_{CC} (typically 12 mA) occurs during a conversion with the signal voltage at its maximum value. I_{CC} is typically 16 mA when the MC6108 is deselected ($\overline{CS}=1$), and under all conditions, I_{CC} is independent of clock frequency.

I_{EE} is typically 38 mA, and varies <2.0 mA over different operating conditions. I_{EE} is independent of clock frequency.

DIGITAL SECTION

SEQUENCE OF OPERATION

A conversion is initiated when the $\overline{S}$ (Start), $\overline{CS}$ (Chip select), and CLK (Clock) inputs are simultaneously low for a minimum of 50 ns. The three inputs may be taken low in any sequence, including simultaneously. After all three have been brought low, $\overline{CC}$ (Conversion Complete) will change to a high state ≈25 ns later, indicating the SAR has been reset. A clock low-to-high transition must then occur before or with $\overline{S}$ switching high, and the conversion begins with the next CLK rising edge ($\overline{S}$ must precede that one by >25 ns). The conversion then requires seven complete clock cycles. At the end of the conversion, $\overline{CC}$ will switch low indicating the end of the conversion, and that valid data is available. See Figure 6 for the basic timing sequence.

If the $\overline{S}$, $\overline{CS}$, and CLK inputs appear simultaneously low ***during*** a conversion, the conversion sequence will be re-initiated at that point.

The following truth table describes the relationship of the six digital inputs (Pins 11–16):

Logic Inputs						Function
CLK	$\overline{CS}$	$\overline{S}$	$\overline{R}$	$D/\overline{ST}$	CodeSel	
X	1	X	X	X	X	Chip de-selected, D0–D7 @ Hi-Z
0	0	0	X	X	X	Reset SAR
↑ ↓	X	1	X	X	X	Conversion process (after SAR is reset)
X	0	X	1	X	X	D0–D7 @ Hi-Z
X	0	1	0	1	1	Read binary or offset binary data at D0–D7 after conversion
X	0	1	0	1	0	Read 2's complement data at D0–D7 after conversion
X	0	1	0	0	X	Read $\overline{CC}$ status at D7 (D0–D6 @ Hi-Z)

X = Don't care

Figure 7 depicts the input configurations in order to read the various output formats. Any digital input left open is equivalent to a Logic "0" — however, good design practice dictates that inputs should never be left open.

FIGURE 6 — CONVERSION TIMING DIAGRAM

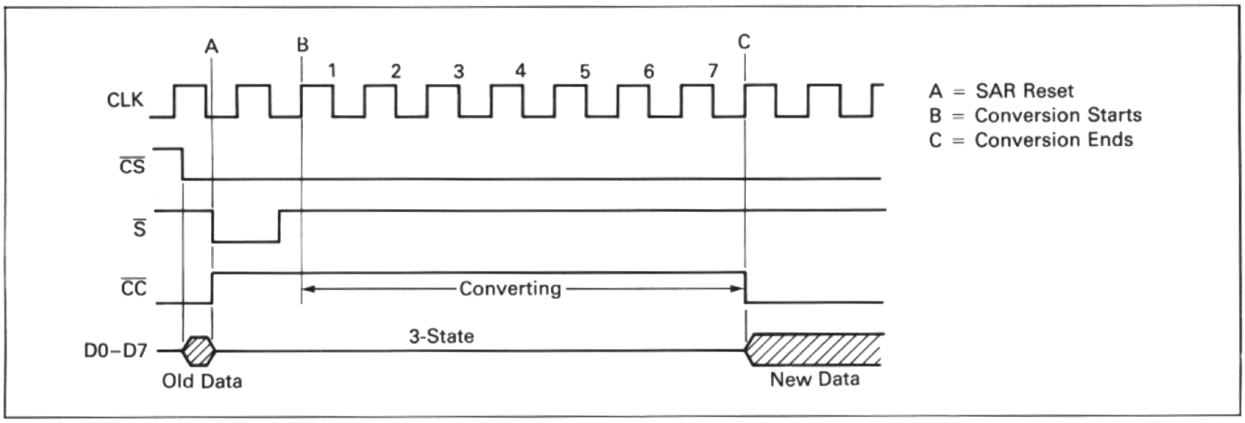
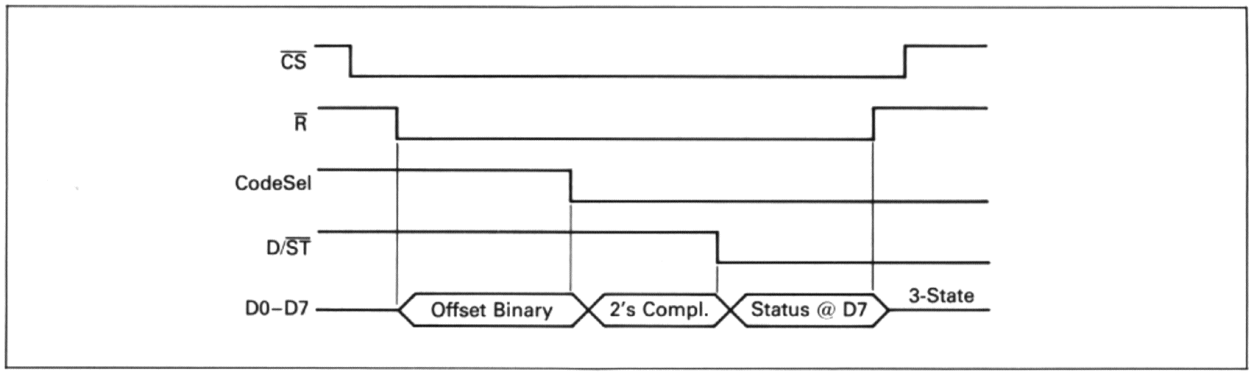


FIGURE 7 — OUTPUT DATA CONTROL



CLOCK

The clock input (Pin 15) is a TTL level input which steps the SAR through the successive approximation conversion process. There is no minimum required frequency, and the maximum operating frequency is listed in the timing characteristics. The clock duty cycle does not have to be 50%, but the minimum low and high times must be observed. The clock is needed only for the conversion, and may be removed or left applied to the MC6108 between conversions. The operation of $\overline{CS}$, D/$\overline{ST}$, $\overline{R}$, and CodeSel are not affected by the presence or absence of the clock.

CHIP SELECT

Chip Select (Pin 12) is a TTL level input which is normally used by a microprocessor's address decoding to select and de-select the device. A Logic "0" selects (enables) the MC6108, while a Logic "1" disables it. $\overline{CS}$ must be low for a conversion to start, and to read data at D0–D7 or status at D7 (see D/$\overline{ST}$ description). $\overline{CS}$ may be taken high during a conversion, as long as the minimum low time for $\overline{CS}$, $\overline{S}$, and CLK is adhered to, and then taken low in order to read the data after $\overline{CC}$ goes low. Alternately $\overline{CS}$ may be left low during the entire conversion.

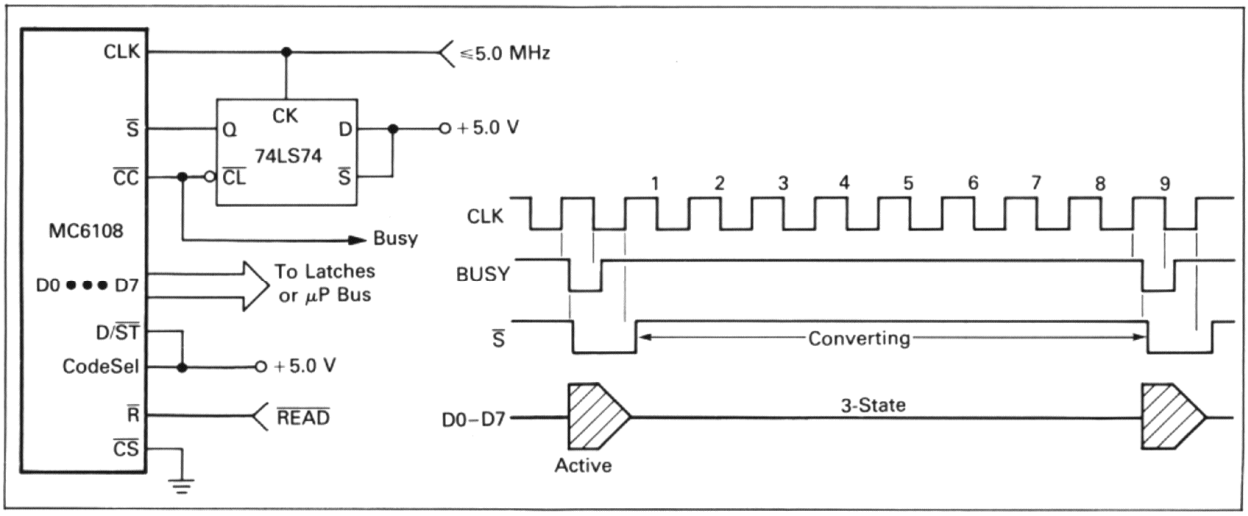
Whenever the MC6108 is de-selected, a conversion cannot be initiated, and D0–D7 are in the high-impedance condition, regardless of the other digital inputs.

START

$\overline{S}$ (Pin 11) is a TTL level input used to reset the SAR, and initiate a conversion. The SAR is reset when this pin is low simultaneous with the Clock and $\overline{CS}$ inputs for a minimum of 50 ns. $\overline{CC}$ output will then change to a high state. A clock rising edge must occur while $\overline{S}$ is low, or no later than coincident with its rising edge. There is no maximum time limit for $\overline{S}$ to stay low, but the conversion will not begin until the next rising edge of the Clock input ***after*** $\overline{S}$ goes high. Seven complete clock cycles are then needed to complete the conversion.

If the $\overline{S}$ input is connected to the $\overline{CC}$ output through a flip-flop (see Figure 8), the MC6108 will operate at the maximum possible conversion repetition rate, i.e. one conversion each 9 clock cycles.

FIGURE 8 — CONFIGURATION FOR MAXIMUM CONVERSION RATE



READ

Read (Pin 13) is a TTL level input which controls the state of the outputs (D0–D7) between conversions as long as the MC6108 is enabled ($\overline{CS}$ = 0). A Logic "1" forces the 8 outputs to a high impedance condition regardless of the other digital inputs. A Logic "0" permits reading the data at D0–D7 after the conversion is complete, or the $\overline{CC}$ status at D7 (depending on the D/$\overline{ST}$ input). During a conversion, $\overline{R}$ is ineffective, except for controlling D7 if D/$\overline{ST}$ is low.

The Read input differs from the $\overline{CS}$ input in that taking Read high does not prevent a conversion from being initiated in response to the $\overline{CS}$, CLK, and $\overline{S}$ inputs (described elsewhere). If desired, the Read input may be kept low at all times in a simple application.

CONVERSION COMPLETE

$\overline{CC}$ (Pin 10) is a TTL level output which indicates the status of the conversion. After $\overline{CS}$, CLK, and $\overline{S}$ are taken low to initiate a conversion, $\overline{CC}$ will go high ≈25 ns later. $\overline{CC}$ will stay high during the conversion, and then go low ≈15 ns after the rising edge of the clock corresponding to the end of the conversion. See Figure 6 and the System Timing Diagram.

The $\overline{CC}$ pin does not have a high impedance capability, and is therefore always active. The $\overline{CC}$ status is typically monitored through a port, or an interrupt pin.

DATA/STATUS

D/$\overline{ST}$ (Pin 14) is a TTL level input which controls the information presented at D0–D7. When at a Logic "1", D0–D7 will provide the digital equivalent of the analog input at the end of the conversion (D0–D7 are in a high impedance mode during the conversion). When at a Logic "0", D0–D6 are maintained in a high impedance mode, while D7 provides the Conversion Complete status both during and after the conversion (D7 does not go into a high impedance mode). The rising and falling edges of D7, when providing status, follow those of $\overline{CC}$ (Pin 10) within ≈ 10 ns.

D/$\overline{ST}$ may be used by the microprocessor as a means of reading the Status ***and*** the Data on the bus rather than using a separate port for the $\overline{CC}$ output (Pin 10). However, since D7 is active during the conversion, the microprocessor cannot be busy with other functions during this time. If the microprocessor is to be busy during the conversion, the status may be checked by periodically switching the D/$\overline{ST}$ pin, or the $\overline{CS}$ pin, or by reading the $\overline{CC}$ pin (Pin 10) through a separate port or interrupt pin. $\overline{R}$ (Pin 13) must be low to read data or status.

CODE SELECT

CodeSel (Pin 16) is a TTL level input which controls the format of the binary data presented at D0–D7 at the end of a conversion. When at a Logic "1", the data is presented as natural binary or offset binary, depending on whether the analog input is unipolar or bipolar, respectively. When at a Logic "0", the output code is in 2's complement form (applicable to bipolar operation only). This pin has no effect on D7 when the D/$\overline{ST}$ input is low (see section on Data/Status). The following tables illustrate examples of the different codes:

UNIPOLAR

Input	+10 V Range	+5.0 V Range	Natural Binary
FS — 1LSB	9.961 V	4.980 V	1111 1111
3/4 FS	7.500 V	3.750 V	1100 0000
1/2 FS	5.000 V	2.500 V	1000 0000
1/4 FS	2.500 V	1.250 V	0100 0000
0	0.000 V	0.000 V	0000 0000

BIPOLAR

Input	±5.0 V Range	Offset Binary	2's Complement
+FS — 1LSB	4.961 V	1111 1111	0111 1111
+1/2 FS	2.500 V	1100 0000	0100 0000
MidScale	0.000 V	1000 0000	0000 0000
−1/2 FS	−2.500 V	0100 0000	1100 0000
−FS + 1LSB	−4.961 V	0000 0001	1000 0001
−FS	−5.000 V	0000 0000	1000 0000

If an input voltage range other than those listed above is used, and CodeSel is at a Logic "1" (binary format), the code 0000 0000 will correspond to the most negative input voltage, while the code 1111 1111 corresponds to the most positive input voltage (−1 LSB). The 2's complement code is the same as the binary with the MSB (D7) inverted.

DATA OUTPUTS

The data outputs (Pins 2–9) are TTL level outputs with high impedance capability. Pin 2 is the LSB (D0), while Pin 9 is the MSB (D7). The 8 outputs are in the high impedance mode during a conversion ($\overline{CC}$ = high), or if $\overline{CS}$ or $\overline{R}$ are high. D0–D6 are in the high impedance mode, and D7 is active, anytime that D/$\overline{ST}$ is low ($\overline{CS}$ = $\overline{R}$ = 0).

During normal operation, the 8 outputs change from valid data to high impedance within 55 ns after the SAR has been reset ($\overline{CS}$ = CLK = $\overline{S}$ = 0) at the beginning of a conversion, and back to valid data within 50 ns after the rising edge of the CLK at the end of a conversion.

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The P.C. board layout, the quality of the power supplies and the ground system ***at the IC*** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC6108 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground ***at the IC*** (within 1" max) with a 10 μF tantalum and a 0.01 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors (<10 Ω, metal film) or inductors between the supplies and the IC.

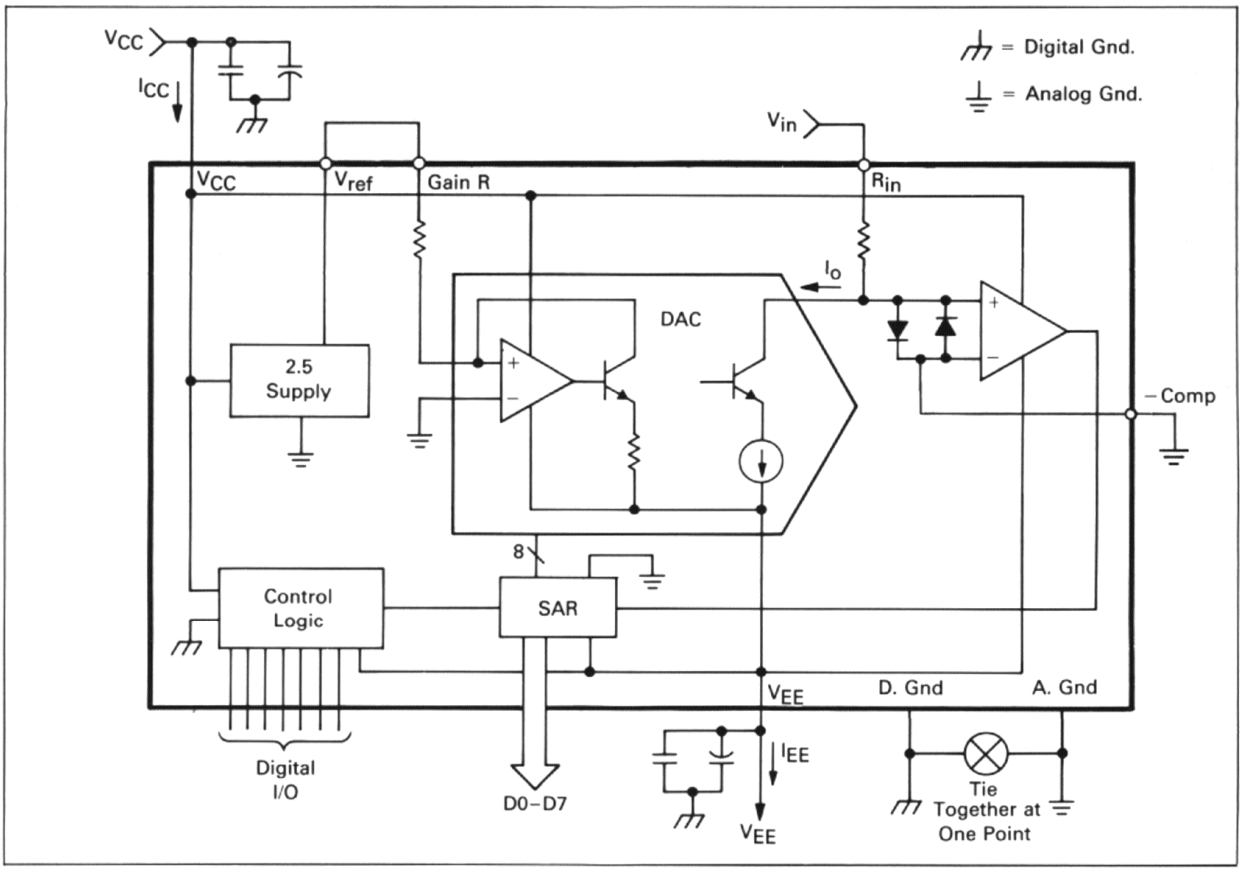
If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50 – 200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC6108.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The P.C. board tracks supplying V_{CC} and V_{EE} to the MC6108 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC6108 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC6108.

The MC6108 has two ground pins — A. Gnd (Pin 26), and D. Gnd. (Pin 17). V_{CC} and V_{EE} should be referenced to D. Gnd. A. Gnd is mainly a signal ground, and is the return path for the internal 2.5 volt reference, and the DAC's reference amplifier. A. Gnd must be connected to D. Gnd, preferably at one point, and in a manner so as to not pick up noise. The dc voltage between A. Gnd and D. Gnd must be <100 mV. Long PC tracks between them should be avoided as the inductance (at 5.0 MHz) can create stability problems. See Figure 9 for a depiction of the major current paths.

FIGURE 9 — MAJOR CURRENT PATHS



FULL SCALE, ZERO ADJUSTMENTS

The unadjusted full scale accuracy (at max. V_{in}) of the MC6108, when the internal resistors are used (Figures 2 and 3), is guaranteed to be within 2-1/2 LSBs. The offset error (at min. V_{in}) is guaranteed to be less than 1LSB for the unipolar configuration, and 2-1/2 LSBs for the bipolar configuration. If the application requires greater accuracy at the end points, then adjustments are needed, as shown in Figures 10 and 11. The potentiometers should be 20-turn type, with low T.C. The 50 Ω resistor is added to the R_{in} pin to ensure that the potentiometers can provide adjustment over the full plus and minus error range.

FIGURE 10 — UNIPOLAR ADJUSTMENTS

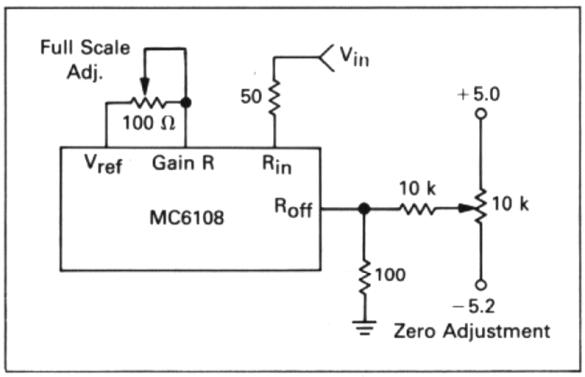
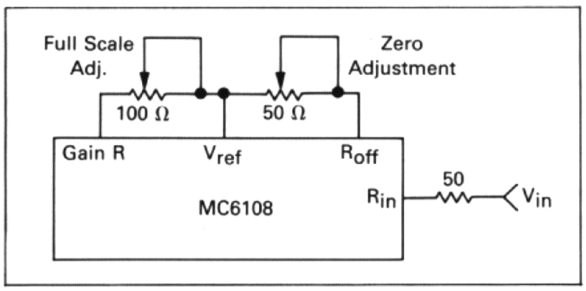


FIGURE 11 — BIPOLAR ADJUSTMENTS

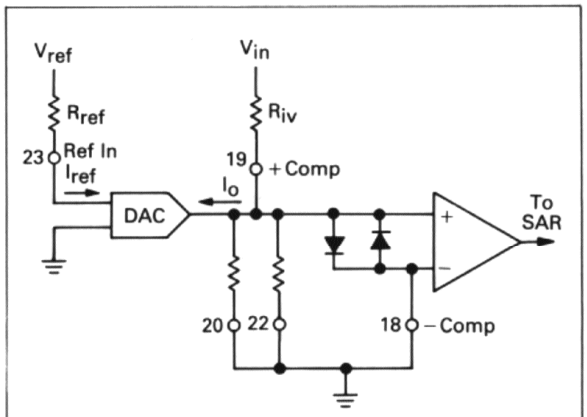


OTHER INPUT RANGES

The MC6108 has internal resistors providing preset input ranges of 0 to +10 volts, 0 to +5.0 volts, and −5.0 to +5.0 volts (see previous section entitled "Signal Voltage"). The input range, and the offset, are determined by the value of the resistors at Pins 20, 22, and 24. Where input ranges other than those listed above are to be digitized, then external resistors of comparable tolerance and temperature coefficient should be used for the reference (at Pin 23), ***and*** for the input signal (at Pin 19), ***and*** for the bipolar offset function (also at Pin 19). See Figures 12 and 13. R_{in} and R_{off} should be connected to A. Gnd when not used. Due to the tolerances of the absolute value of the internal resistors, they should not be used in conjunction with external resistors.

Figure 13 shows the reference current and the offset current supplied from the same reference source, which may be the internal reference (Pin 25). However, separate sources may be used for the two currents if desired.

FIGURE 12 — UNIPOLAR CONVERSION USING EXTERNAL REFERENCE AND RESISTORS



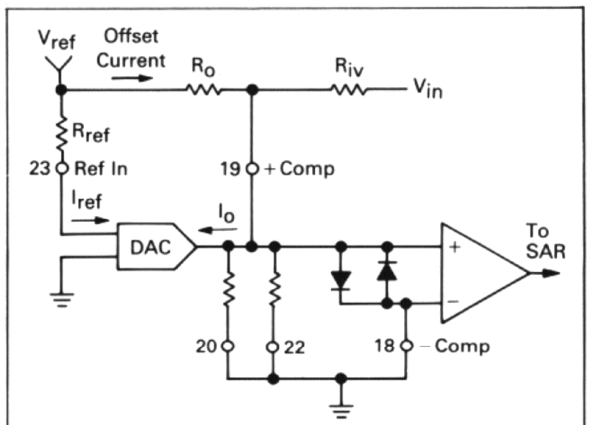
$$\text{Max } V_{in} = \frac{4 \times V_{ref} \times R_{iv}}{R_{ref}}$$

A modulation of the input signal (for waveform manipulation or signal processing) may be done by applying the modulating signal to the reference current. Rewriting equation 1 to determine the output code results in:

$$A = \frac{I_o \times 256}{4 \times I_{ref}} = \frac{V_{in} \times 256}{R_{in} \times 4 \times I_{ref}} \qquad (5)$$

(The offset term has been omitted to simplify the equation.) As can be seen, the output code varies inversely with the reference. When varying the reference current, its value must be maintained between 0.5 and 2.0 mA, and the current flow ***must*** always be ***into*** Pin 23 or 24.

FIGURE 13 — BIPOLAR CONVERSION USING EXTERNAL REFERENCE & RESISTORS



$$\text{Max } V_{in} = V_{ref} \times R_{iv} \left[\frac{4}{R_{ref}} - \frac{1}{R_o}\right]$$

$$\text{Min } V_{in} = -\frac{V_{ref} \times R_{iv}}{R_o}$$

MAXIMUM CONVERSION RATE

Although a conversion, once initiated, requires 7+ clock cycles, the maximum conversion repetition rate is once per 9 clock cycles, due to the DAC and SAR reset times. This is easily achieved by connecting $\overline{CC}$ to $\overline{S}$, through a D-type flip-flop, allowing the MC6108 to restart itself at the end of each conversion (see Figure 8). In this mode, the data outputs may be connected directly to the microprocessor bus, and the BUSY output used to indicate when valid data is available. Alternately, the data outputs may be connected to latches, which are activated by the BUSY signal, in order that the microprocessor may read the data at its convenience. This configuration may also be used for DMA loading of memory.

MICROPROCESSOR INTERFACING

With the proliferation of microprocessors available today, interfacing schemes can take any one of several hundred configurations. Figures 14, 15, and 16 indicate some generic interfacing schemes which can be adapted to most any microprocessor. Some of the terminology in the Figures is based on the MC6800 series of processors — other processors have similar functions by different names.

Figure 14 depicts a simple basic interface using a port (such as an MC6821) and/or an interrupt. A conversion is initiated when the active low address decoder switches low, R/$\overline{W}$ is high, and the port outputs one active low pulse to $\overline{S}$. At the end of the conversion, $\overline{CC}$ goes low, alerting the processor through the port or through an interrupt. The processor can then read the data at its convenience by switching $\overline{R}$ and $\overline{CS}$ low.

Figure 15 eliminates the need for an interrupt, and instead periodically checks the conversion status at D7 (D/$\overline{ST}$ = low) by reading the data bus. When D7 is low, the conversion is complete, and the D/$\overline{ST}$ input is then taken high so as to read the data at D0–D7.

Figure 16 eliminates the need for an interrupt or a port, but requires the processor to wait during the conversion until it is complete. The conversion is initiated when the address decoder switches low, and R/$\overline{W}$ goes high — that brings $\overline{CS}$ low ***and*** provides the $\overline{Start}$ pulse. The processor waits 9 clock cycles, and then reads the data.

In the above examples, the timing of the $\overline{S}$ pulse must be such that it is low for >50 ns concurrently with $\overline{CS}$ and CLK low, and must include one rising clock edge. If the $\overline{S}$ pulse timing is synchronized with the other inputs, this is relatively easy to guarantee. If, however, in Figure 16, the $\overline{CS}$ and CLK are not synchronized, then the SN74LS122 must be set for a pulse width that is equal to or greater than one clock cycle.

FIGURE 14 — BASIC MICROPROCESSOR INTERFACE

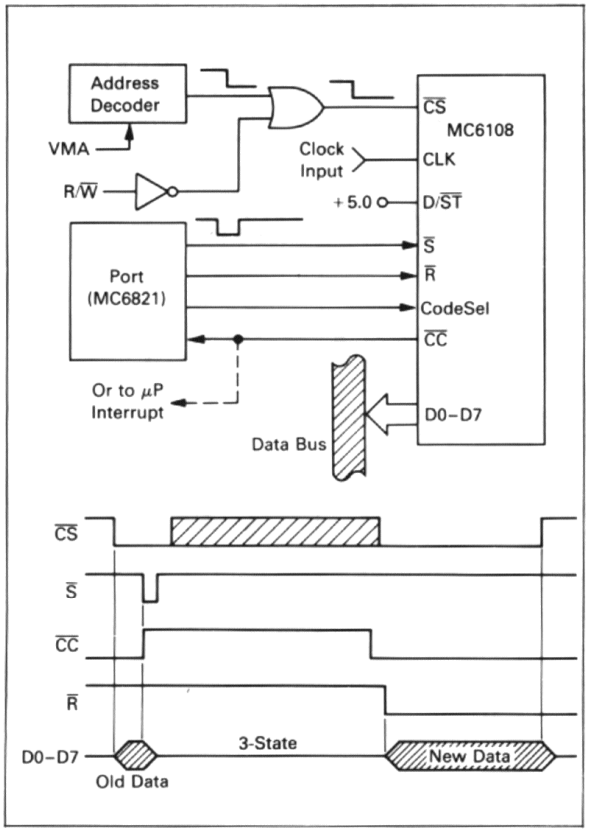


FIGURE 15 — MICROPROCESSOR INTERFACE WITHOUT AN INTERRUPT

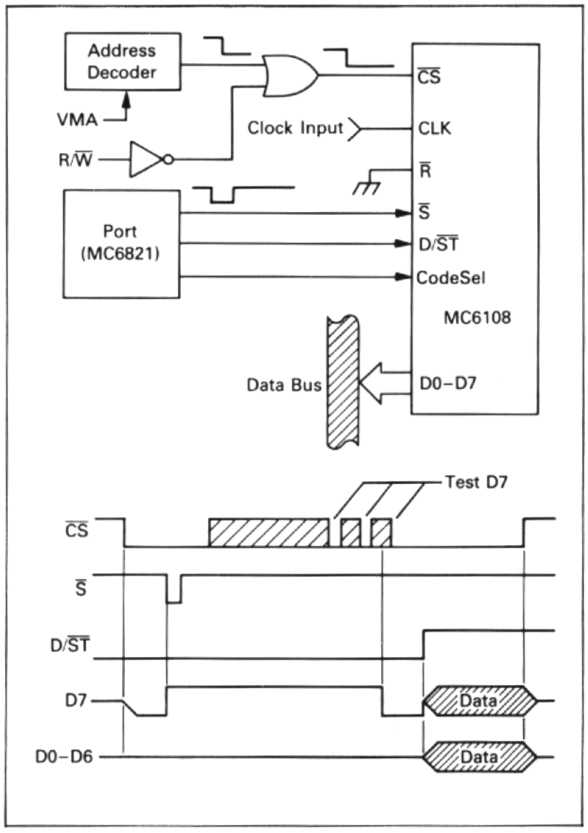
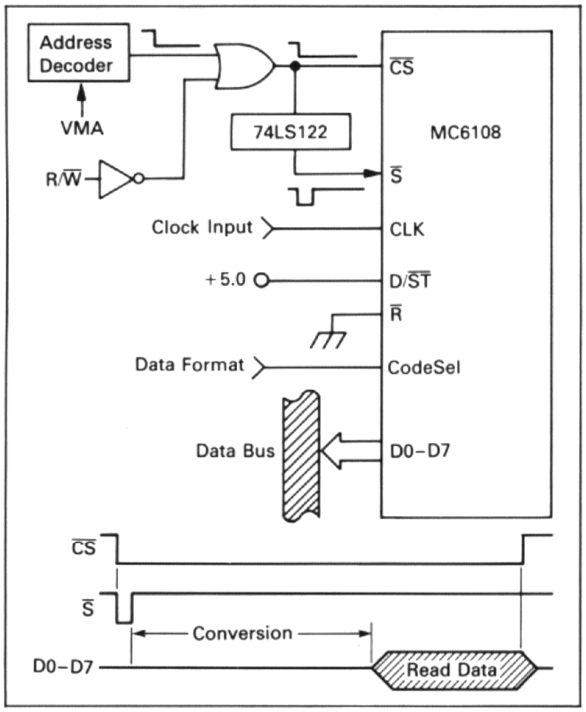


FIGURE 16 — MICROPROCESSOR INTERFACE WITHOUT USING A PORT OR INTERRUPT



STAND-ALONE USE

Although the MC6108 was designed for use with microprocessors, it can be used in a stand-alone mode. The digital inputs may be controlled by other digital circuitry, or hard-wired in a simple application. Figure 17 shows a simple configuration whereby the MC6108 is permanently enabled, and each $\overline{S}$ input pulse provides new data at the outputs. Figure 18 shows a circuit whereby the MC6108 is continually self-updating the information into latches. The latches are necessary since in this mode of operation, the MC6108 data outputs are in the 3-state mode the majority of the time. The 430 Ω resistor and 68 pF capacitor provide a ≈60 ns delay from $\overline{CC}$'s falling edge to allow D0–D7 to stabilize, and to allow the setup time required by the SN74LS374 latches. The clock high time in this circuit must be ≥100 ns.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −5.2 volts, nor a higher negative voltage from which to derive the −5.2 volts — the circuit of Figure 19 can be used to generate the −5.2 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC6108. The MC34063 is a switching regulator, and in Figure 19 is configured in an inverting mode of operation. The regulator operating specifications are given in the Figure.

FIGURE 17 — STAND-ALONE OPERATION (CONTINUOUSLY ENABLED)

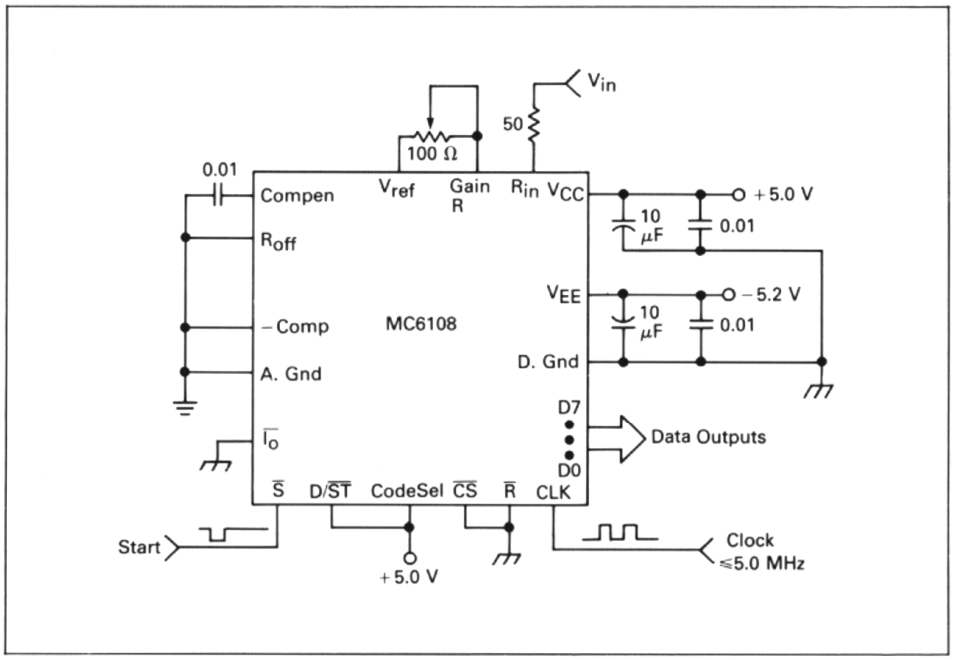


FIGURE 18 — STAND-ALONE OPERATION AT MAXIMUM UPDATE RATE

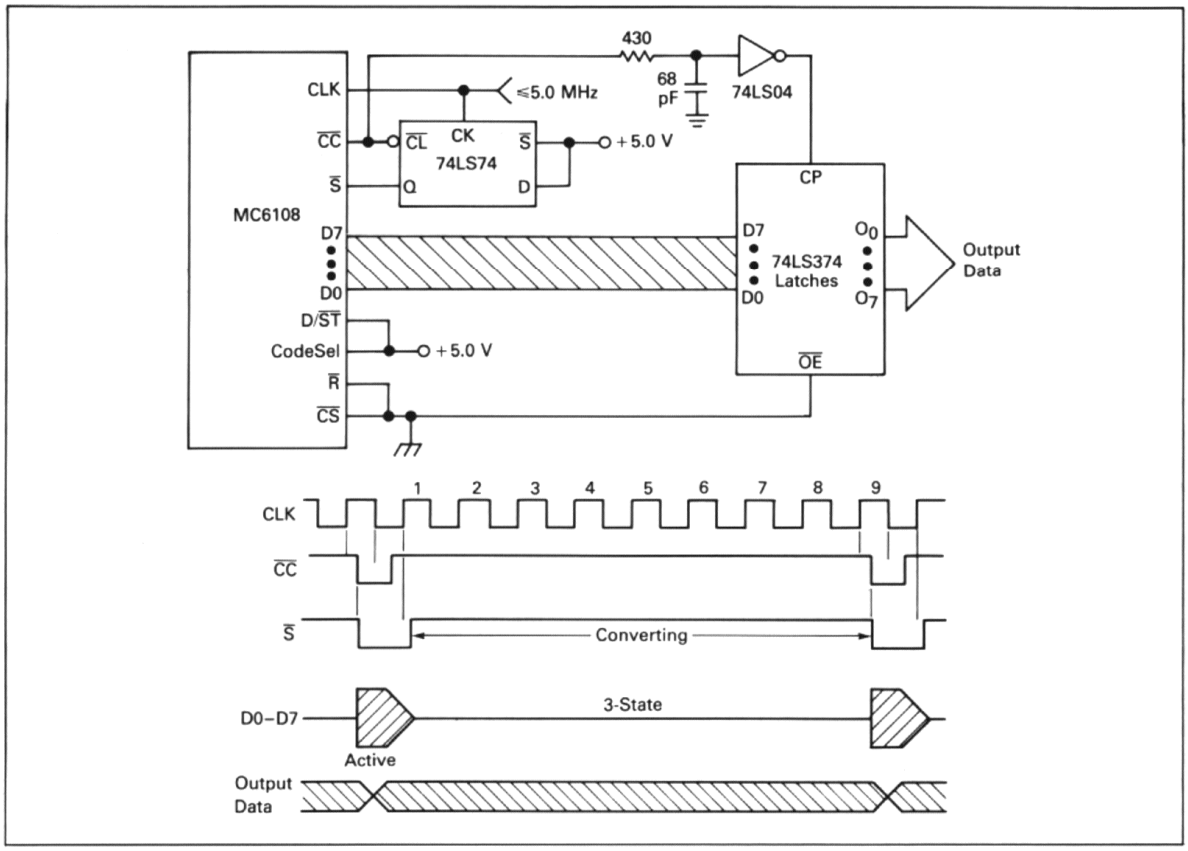
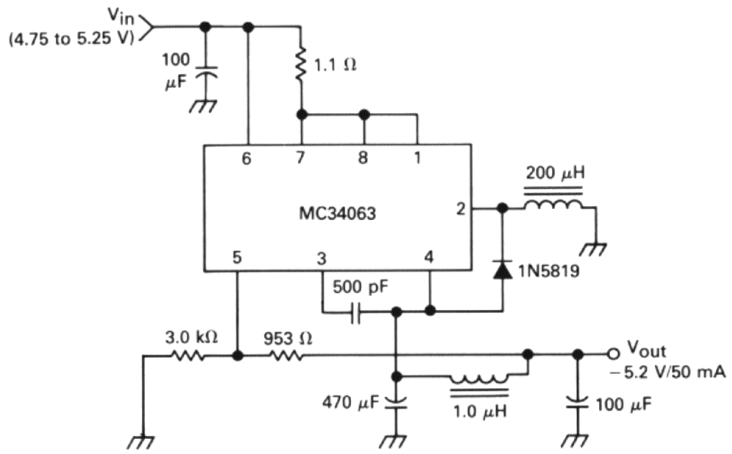


FIGURE 19 — −5.2 VOLTAGE REGULATOR



Line Regulation	4.75 V < V_{in} < 5.25 V (I_{out} = 20 mA)	0.04%
Load Regulation	V_{in} = 5.0 V, 20 mA < I_{out} < 50 mA	0.8%
Output Ripple	V_{in} = 5.0 V, I_{out} = 50 mA	3.0 mV p-p
Short Circuit I_{out}	V_{in} = 5.0 V, R1 = 0.1 Ω	300 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	57%

GLOSSARY

BANDGAP REFERENCE — A voltage reference circuit based on the predictable base-emitter voltage of a transistor. The silicon bandgap voltage of ≈1.2 volts is the basis for generating other voltages which are stable with time and temperature.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −5 to +5 V, −2 to +8 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of an A-D) of the $7F_H$ to 80_H transition. The ideal location is 1/2 LSB below zero volts in the case of an A-D set up for a symmetrical bipolar input (e.g., −5 to +5 V).

DAC CURRENT GAIN — The internal gain the DAC applies to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.

DIFFERENTIAL NON-LINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n.(n = number of bits). This error must be within ±1 LSB for proper operation.

FULL SCALE CURRENT or RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), or output (of a DAC).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), or output (of a DAC), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point) of a data converter, with respect to the device's internal reference. The gain error is usually expressed in LSBs.

INTEGRAL NON-LINEARITY — The maximum error of an A-D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A-D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code whose normalized decimal value is defined by:

$$N = A_n2^n + \ldots + A_32^3 + A_22^2 + A_12^1 + A_02^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes corresponds to a zero input voltage of an A-D, and all ones corresponds to the most positive input voltage.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative input voltage (of an A-D), while all ones corresponds to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

RESOLUTION — The smallest change which can be discerned by an A-D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

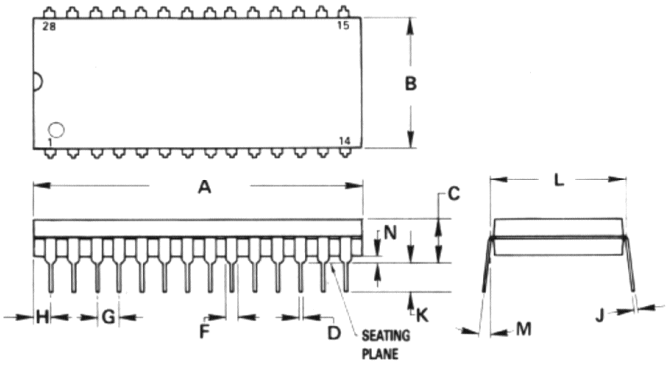
SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A-D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

TWO'S COMPLEMENT CODE — A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeroes, plus a carry. It is the same as Offset Binary Code, with the MSB inverted.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A-D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +10 V, 0 to −5 V, +2 to +8 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

OUTLINE DIMENSIONS



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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