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by MC54HCT533A/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

# MC54/74HCT533A

*Advance Information*

# Octal 3-State Inverting Transparent Latch with LSTTL Compatible Inputs

## High-Performance Silicon-Gate CMOS

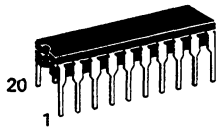
The MC54/74HCT533A is identical in pinout to the LS533. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

When Latch Enable is high, these latches appear transparent to data (i.e., the outputs change asynchronously). The data appears at the outputs in inverted form. When Latch enable is taken low, data meeting the set-up and hold times becomes latched.

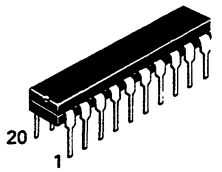
The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC533A is identical in function to the HCT563 which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT373.

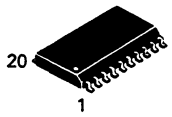
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 $\mu$A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates




J SUFFIX
CERAMIC
CASE 732-03




N SUFFIX
PLASTIC
CASE 738-03

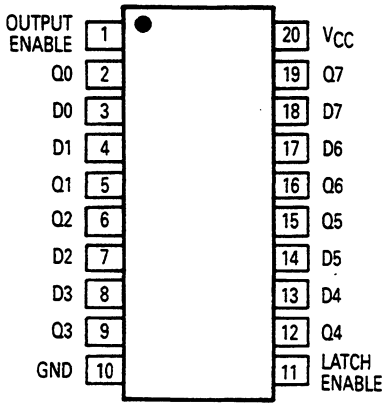



DW SUFFIX
SOIC
CASE 751D-03

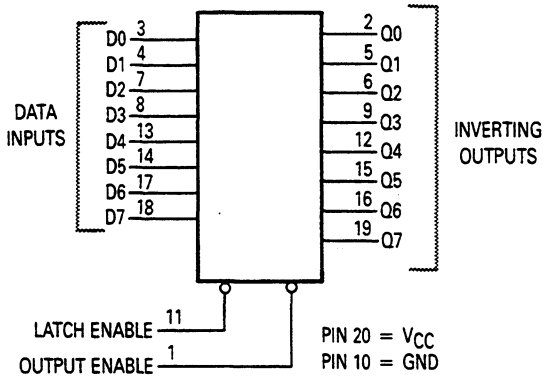
### ORDERING INFORMATION

| | |
|---|---|
| MC74HCTXXAN | Plastic |
| MC54HCTXXAJ | Ceramic |
| MC74HCTXXADW | SOIC |

### PIN ASSIGNMENT




### LOGIC DIAGRAM




| Design Criteria | Value | Unit |
|---|---|---|
| Internal Gate Count* | 66.5 | ea |
| Internal Gate Propagation Delay | 1.0 | ns |
| Internal Gate Power Dissipation | 5.0 | $\mu$W |
| Speed Power Product | 0.005 | pJ |

*Equivalent to a two-input NAND gate.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

### FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| Output Enable | Latch Enable | D | Q |
| L | H | H | L |
| L | H | L | H |
| L | L | X | no change |
| H | X | X | Z |

X = Don't Care
Z = High Impedance



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## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | −0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | −1.5 to $V_{CC}$+1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | −0.5 to $V_{CC}$+0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±35 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±75 | mA |
| $P_D$ | Power Dissipation in Still Air,<br>Plastic or Ceramic DIP<br>SOIC Package | <br>750<br>500 | mW |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds<br>(SOIC or Plastic DIP)<br>(Ceramic DIP) | <br>260<br>300 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| $V_{in}$,$V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 2.0<br>2.0 | 2.0<br>2.0 | 2..0<br>2.0 | V |
| $V_{IL}$ | Maximum Low-Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 0.8<br>0.8 | 0.8<br>0.8 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 4.4<br>5.4 | 4.4<br>5.4 | 4.4<br>5.4 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 6.0 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 0.1<br>0.1 | 0.1<br>0.1 | 0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 6.0 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0 μA | 5.5 | 4.0 | 40 | 160 | μA |
| $I_{OZ}$ | Maximum Three-State Leakage Current | Output in High-Impedance State<br>$V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 5.5 | ±0.5 | ±5.0 | ±10 | μA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{in}$ = 2.4 V, Any One Input<br>$V_{in}$ = $V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0 μA | 5.5 | ≥ −55°C | 25°C to 125°C | mA |
| | | | | 2.9 | 2.4 | |

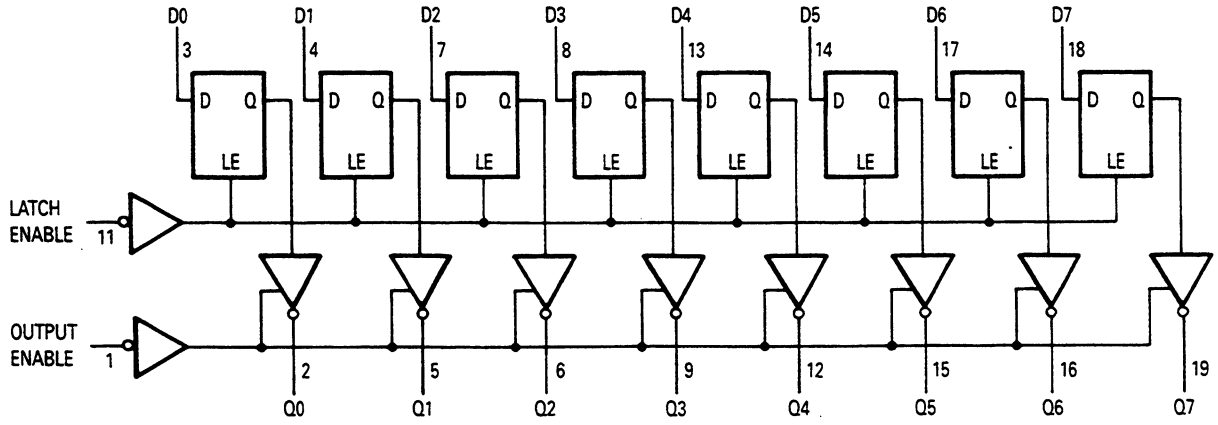
**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V ±10%, $C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|
| | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input D to Q (Figures 1 and 5) | 30 | 38 | 45 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5) | 33 | 41 | 50 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay Time, Output Enable to Q (Figures 3 and 6) | 31 | 39 | 47 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Propagation Delay Time, Output Enable to Q (Figures 3 and 6) | 35 | 44 | 53 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, any Output (Figures 1 and 5) | 12 | 15 | 18 | ns |
| $C_{in}$ | Maximum Input Capacitance | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Tri-State Output Capacitance, Output in Hi-Impedance State | 15 | 15 | 15 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ | Typical @ 25°C, $V_{CC}$ = 5.0 V | | | pF |
| | | 83.5 | | | |

**TIMING REQUIREMENTS** ($V_{CC}$ = 5.0 V ±10%, $C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Figure | Guaranteed Limit | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 25°C to −55°C | | ≤85°C | | ≤125°C | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{su}$ | Minimum Setup Time, Input D to Latch Enable | 4 | 10 | | 13 | | 15 | | ns |
| $t_h$ | Minimum Hold Time, Latch Enable to Input D | 4 | 8 | | 10 | | 12 | | ns |
| $t_w$ | Minimum Pulse Width, Latch Enable | 2 | 12 | | 15 | | 18 | | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times | 1 | | 500 | | 500 | | 500 | ns |

## EXPANDED LOGIC DIAGRAM



## SWITCHING WAVEFORMS

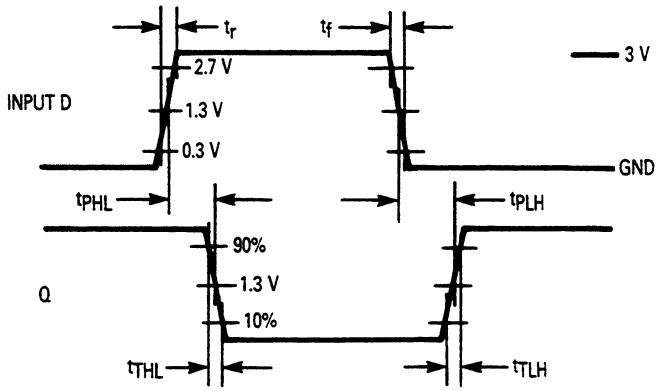



**Figure 1.**

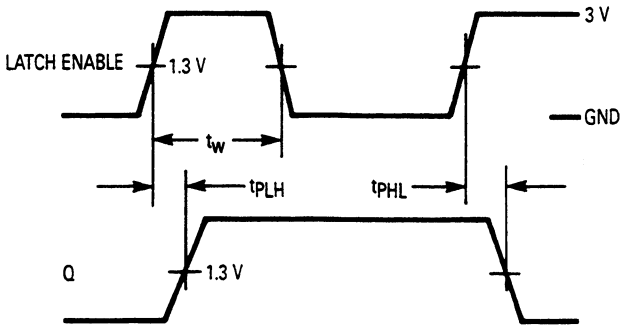



**Figure 2.**

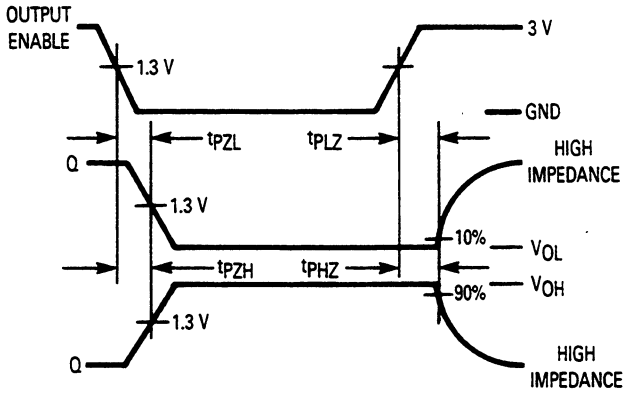



**Figure 3.**

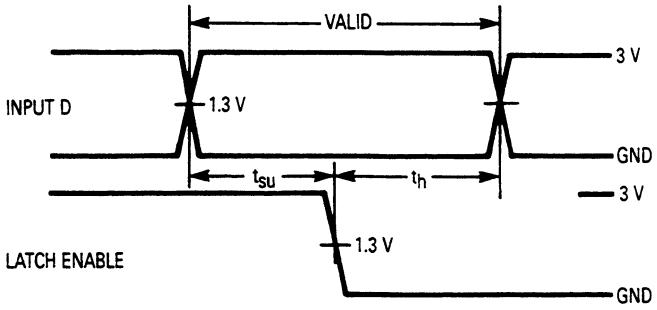
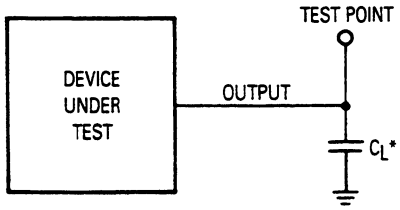
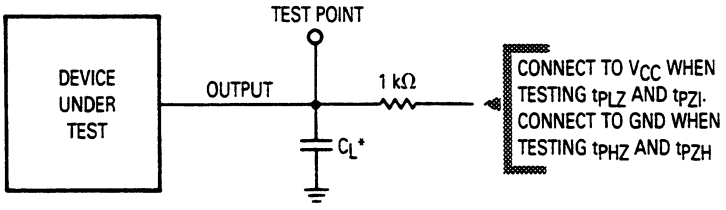



**Figure 4.**




*Includes all probe and jig capacitance

**Figure 5. Test Circuit**

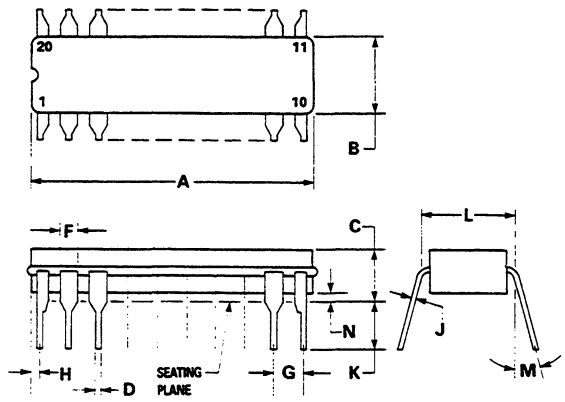



*Includes all probe and jig capacitance

**Figure 6. Test Circuit**

## OUTLINE DIMENSIONS

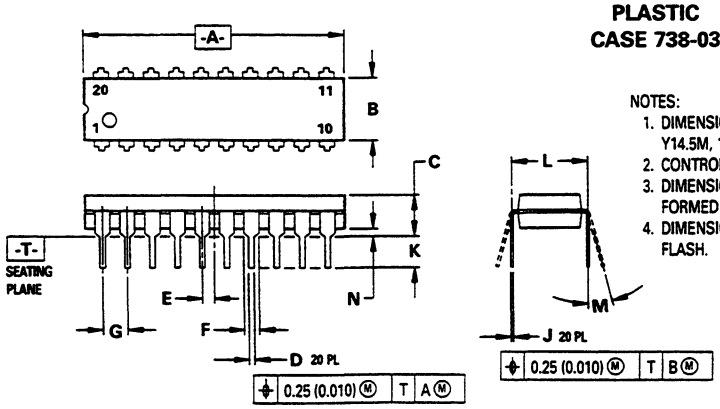
### J SUFFIX
### CERAMIC
### CASE 732-03




NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 23.88 | 25.15 | 0.940 | 0.990 |
| B | 6.60 | 7.49 | 0.260 | 0.295 |
| C | 3.81 | 5.08 | 0.150 | 0.200 |
| D | 0.38 | 0.56 | 0.015 | 0.022 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.51 | 1.27 | 0.020 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.25 | 1.02 | 0.010 | 0.040 |

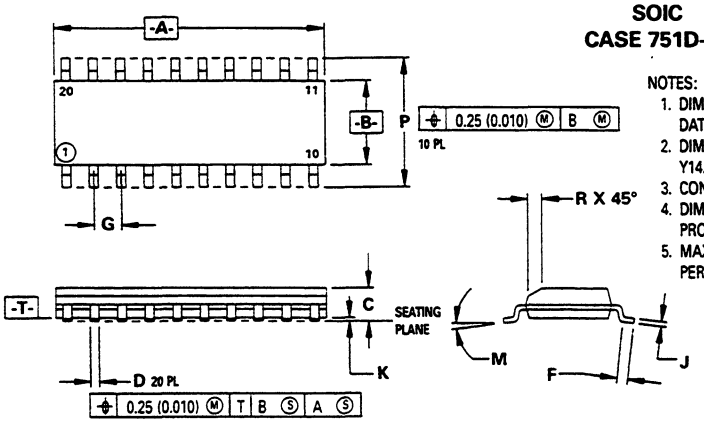
### N SUFFIX
### PLASTIC
### CASE 738-03




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 25.66 | 27.17 | 1.010 | 1.070 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.81 | 4.57 | 0.150 | 0.180 |
| D | 0.39 | 0.55 | 0.015 | 0.022 |
| E | 1.27 BSC | | 0.050 BSC | |
| F | 1.27 | 1.77 | 0.050 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.21 | 0.38 | 0.008 | 0.015 |
| K | 2.80 | 3.55 | 0.110 | 0.140 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.01 | 0.020 | 0.040 |

### DW SUFFIX
### SOIC
### CASE 751D-03




NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 12.65 | 12.95 | 0.499 | 0.510 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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