



Product Preview

Picture-in-Picture (PIP) Controller

The MC44463 Picture-In-Picture (PIP) controller is a low cost member of a family of high performance PIP controllers and video processors for television. It is a follow-up to the MC44461 PIP, in which two additional modes of operation have been added. A replay mode is provided, which captures several seconds of the main picture for replay in four different speeds. The capture time is programmable in four resolutions (ratio of captured fields to total fields), which trade the number of fields captured to the length of replay time. The second additional mode provides for multiple small picture overlays from a second non-synchronized source. The number of PIP images is 3 for the 1/9 screen area and 4 for the 1/16 screen area. Like the MC44461 this is NTSC compatible, I²C bus controlled and available in the 56-pin shrink dip (SDIP) package.

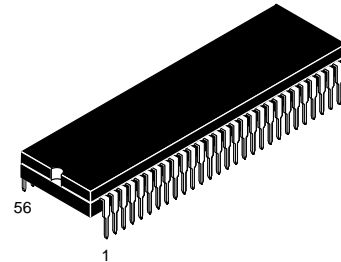
The main features of the MC44463 are:

- Three PIP Functional Modes: Standard Single Active PIP Mode, Up to 8 Seconds of Capture and Replay Mode, and a 3 or 4 Multiple PIP Mode – Vertical Stacked with 1 Active at Any One Time
- 4 Capture Resolutions – 1 out of 10, 1:8, 1:6, 1:4. 4 Playback Speeds = 1 Times Acquire Speed; 1/2; 1/4; 1/8
- Full 2 Frame Store for the Single PIP Removes the Rolling Store/Playback Memory Interference – “Joint Line”
- External Memory for Replay and Multiple Modes: 4 Meg and 16 Meg
- Two NTSC CVBS Inputs – Switchable Main and PIP Video Signals
- Single NTSC CVBS Output Allows Simple TV Chassis Integration
- Two PIP Sizes; 1/16 and 1/9 Screen Area – Freeze Field Feature
- Variable PIP Position in 64–X by 64–Y Steps
- PIP Border with Programmable Color
- Programmable PIP Tint and Saturation Control
- Automatic Main to PIP Contrast Balance
- Vertical Filter
- I²C Bus Control – No External Variable Adjustments Needed
- Operates from a Single 5.0 V Supply
- Economical 56–Pin Shrink DIP Package

MC44463

REPLAY AND MULTIPLE PICTURE-IN-PICTURE (PIP) CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

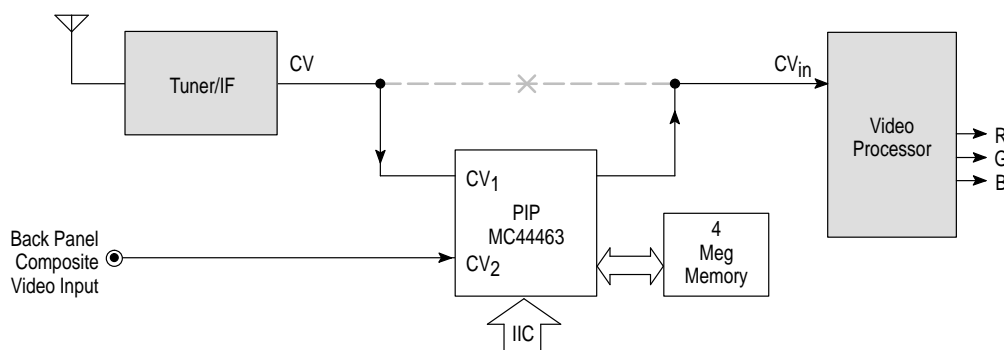


B SUFFIX
PLASTIC PACKAGE
CASE 859
(SDIP)

ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|----------|---------------------------------|---------|
| MC44463B | T _J = –65° to +150°C | SDIP |

Composite Video Simplified System Diagram



MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|--------------------------|-------------------------|-----------|
| Power Supply Voltage | V_{DD} | –0.5 to +6.0 | V |
| Power Supply Voltage | V_{CC} | –0.5 to +6.0 | V |
| Input Voltage Range | V_{IR} | –0.5, $V_{DD} + 0.5$ | V |
| Output Current | I_O | 160 | mA |
| Power Dissipation Maximum Power Dissipation @ 70°C Thermal Resistance, Junction-to-Air | P_D $R_{\theta JA}$ | 1.3 59 | W °C/W |
| Junction Temperature (Storage and Operating) | T_J | –65 to +150 | °C |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS ($V_{CC} = V_{DD} = 5.0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

POWER SUPPLY

| | | | | | |
|--------------------------------------|--------------------|---|-----|-----|----|
| Total Supply (Pins 8, 15, 43 and 50) | Total I_{Supply} | – | 110 | 160 | mA |
|--------------------------------------|--------------------|---|-----|-----|----|

VIDEO

| | | | | | |
|--|--------|---|-----------|---|----------|
| Composite Video Input (Pin 34 or 36) | CV_i | – | 1.0 | – | V_{pp} |
| Composite Video Output (Pin 49, Unterminated) | – | – | 2.0 | – | V_{pp} |
| Video Output DC Level (Sync Tip) | – | – | 1.0 | – | Vdc |
| Video Gain | – | – | 6.0 | – | dB |
| Video Frequency Response (Main Video to –1.0 dB) | – | – | 10 | – | MHz |
| Color Bar Accuracy | – | – | ± 4.0 | – | deg |
| Video Crosstalk (@ 75% Color Bars) | – | – | 55 | – | dB |
| Main to PIP | – | – | 55 | – | |
| PIP to Main | – | – | 55 | – | |
| Output Impedance | – | – | 5.0 | – | Ω |

HORIZONTAL TIMEBASE

| | | | | | |
|--|---|---|-----------|---|---------------|
| Free Run HPLL Frequency (Pin 16) | – | – | 15734 | – | Hz |
| HPLL Pull-In Range | – | – | ± 400 | – | Hz |
| HPLL Jitter | – | – | ± 4.0 | – | ns |
| Burst Gate Timing (from Trailing Edge Hsync, Pin 24) | – | – | 1.0 | – | μs |
| Burst Gate Width | – | – | 4.0 | – | μs |

VERTICAL TIMEBASE

| | | | | | |
|--------------------------------|---|---|---------|---|---------------|
| Vertical Countdown Window | – | – | 232/296 | – | H lines |
| Vertical Sync Integration Time | – | – | 31 | – | μs |

ANALOG TO DIGITAL CONVERTER

| | | | | | |
|---|---|---|---------|---|------|
| Resolution | – | – | – | 6 | Bits |
| Integral Non-Linearity | – | – | ± 1 | – | LSB |
| Differential Non-Linearity | – | – | $+2/-1$ | – | LSB |
| ADC – Y Frequency Response @ –5.0 dB | – | – | 1.0 | – | MHz |
| ADC – U, V Frequency Response @ –5.0 dB | – | – | 200 | – | kHz |
| Sample Clock Frequency ($4/3 F_{SC}$) | – | – | 4.773 | – | MHz |

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = V_{DD} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

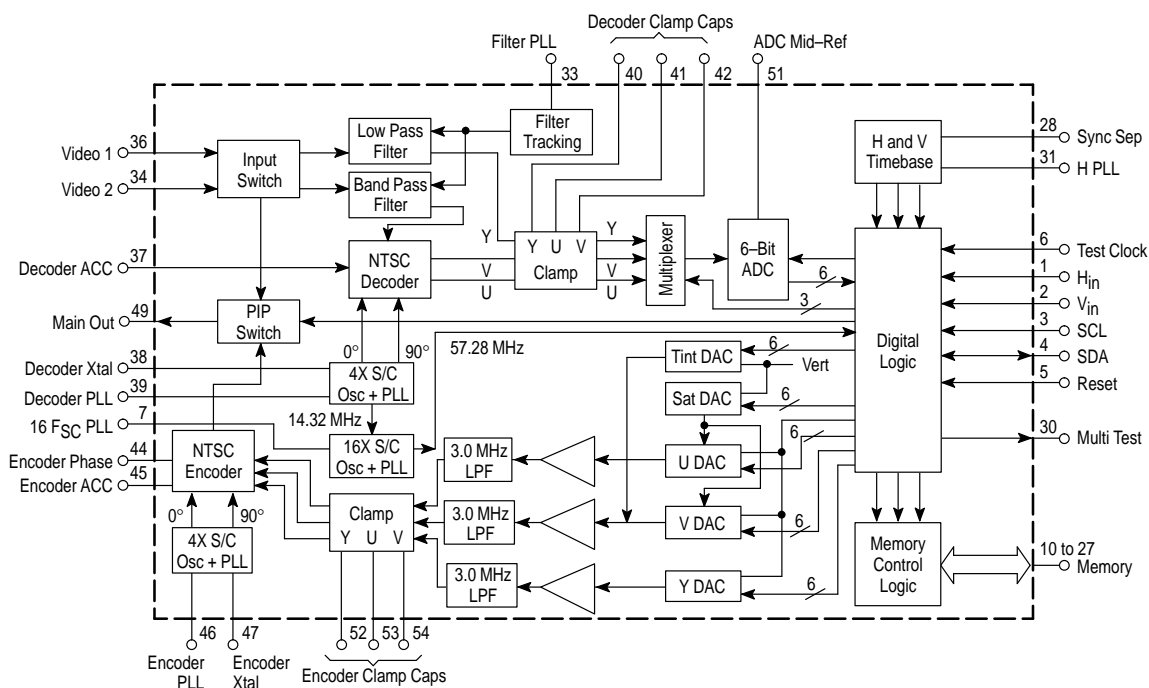
| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------|-----|-----------|-----|------|
| DIGITAL TO ANALOG CONVERTER | | | | | |
| Resolution | — | — | — | 6 | Bits |
| Integral Non-Linearity | — | — | ± 1 | — | LSB |
| Differential Non-Linearity | — | — | $+2/-1$ | — | LSB |
| Tint DAC Control Range (in 64 Steps) | — | — | ± 10 | — | Deg |
| Saturation DAC Control Range (in 64 steps) | — | — | ± 6.0 | — | dB |

NTSC DECODER

| | | | | | |
|--|---|---|-----------|---|----|
| Color Kill Threshold | — | — | $-24/-16$ | — | dB |
| Threshold Hysteresis | — | — | ± 1.0 | — | dB |
| ACC (Chroma Amplitude Change, +3.0 dB to -12 dB) | — | — | ± 5.0 | — | dB |

PIP CHARACTERISTICS

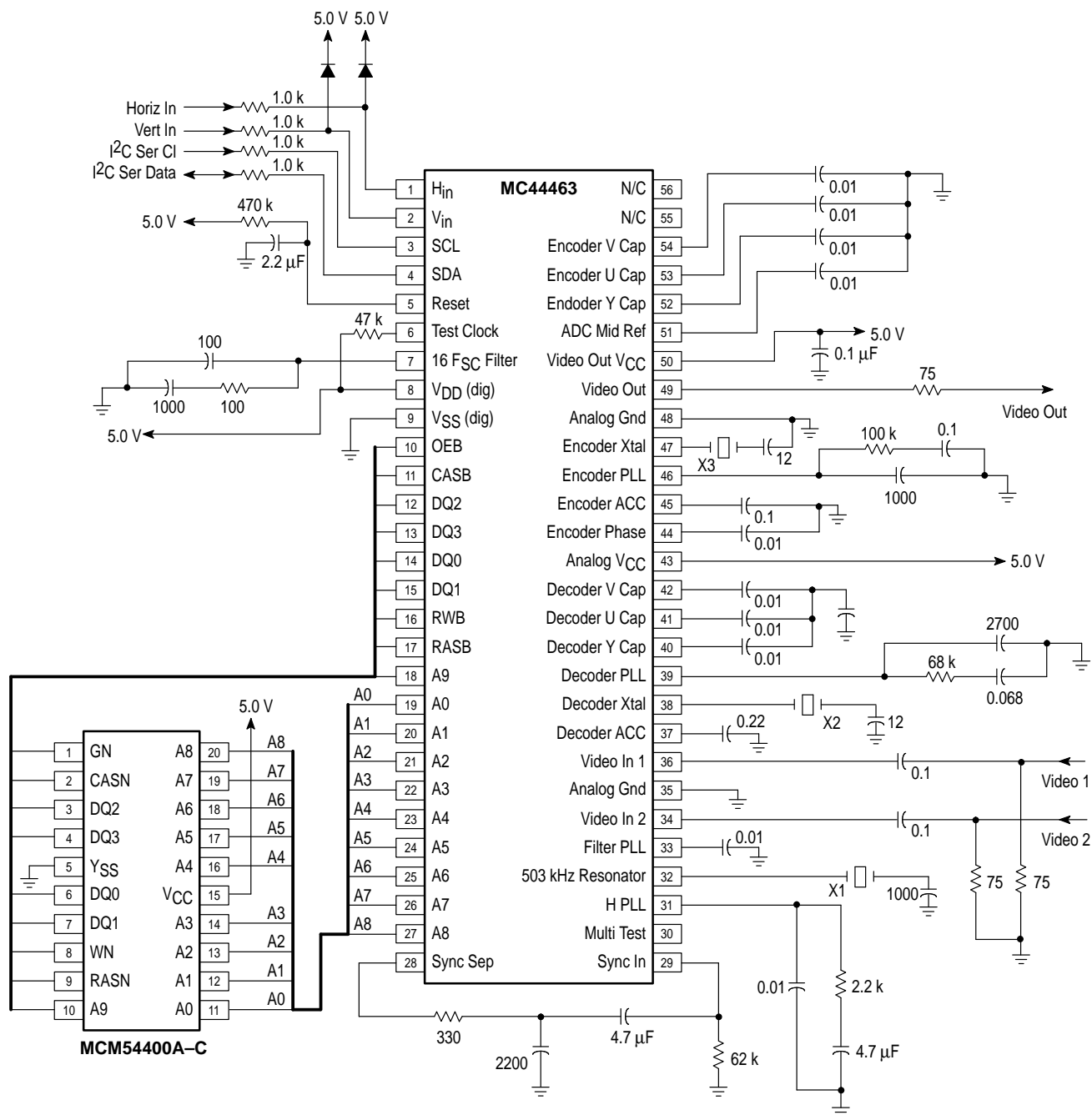
| | | | | | |
|---|---|---|--------|---|-------|
| PIP Size | — | — | — | — | — |
| 1/9 Screen Horizontal | — | — | 114 | — | pels |
| 1/9 Screen Vertical | — | — | 71 | — | lines |
| 1/16 Screen Horizontal | — | — | 84 | — | pels |
| 1/16 Screen Vertical | — | — | 53 | — | lines |
| Border Size Horizontal | — | — | 3 | — | pels |
| Border Size Vertical | — | — | 2 | — | lines |
| Output PEL Clock ($4 F_{SC}$) | — | — | 14.318 | — | MHz |
| Position Control Range Horizontal (% of Main Picture), 64 Steps | — | — | 100 | — | % |
| Position Control Range Vertical (% of Main Picture), 64 Steps | — | — | 100 | — | % |

Figure 1. Representative Block Diagram

This device contains approximately 300,000 active transistors.

MC44463

Figure 2. Application Circuit



X1 – 503 kHz – Murata Erie CSB503F2 or equivalent
X2 – 14.31818 MHz – Fox 143–20 or equivalent
X3 – 14.31818 MHz – Fox 143–20 or equivalent

I²C REGISTER DESCRIPTIONS

Base write address = 26h

Base read address = 27h

Read Register

There are two active bits in the single read byte available from the MC44463 as follows:

Write Vertical Indicator (WVIO) – D7

When 0 indicates that the write operation specified by the last I²C command has been completed.

PIP Sync Detect Bit (PSD0) – D1

When 0 indicates that the PIP video H pulses are present and the horizontal timebase oscillator is within acceptable limits.

Write Registers**Read Start Position/Write Start Position Registers**

Sub-address = 00h

Write Raster Position Start Bits (WPS0–2) – D0–D2

Establishes the horizontal beginning of the PIP and its black level measurement gate. This beginning may be varied by approximately 3.0 μ s. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub-address 03h).

Read Raster Position Bits (RPS0–3) – D4–D7

Establishes the clamp gate position for the black level reference for the main picture. This position may be varied by approximately 5.0 μ s. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub-address 03h).

Pip Switch Delay/Vertical Filter Register

Sub-address = 01h

PIP Switch Delay Bits (PSD0–3) – D0–D3

Delays the start of PIP on time relative to the PIP picture. These bits are used to center the PIP border and PIP picture in the horizontal direction.

Vertical Filter Bit (VFON) – D4

When the filter is activated (VFON = 1) a three line weighted average is taken to provide the data stored in the field memory.

Border Color Register

Sub-address = 02h

Border Color Bits (BC0–2) – D0–D2

These Bits control the color of the border. Note that when using one of the saturated border colors it is possible to get objectionable dot crawl at the edge of the border in some TVs unless appropriate comb filtering is used in the TV circuitry.

| BC (2:0) | Border Color |
|----------|-------------------|
| 000 | Black |
| 001 | White 70% |
| 010 | No Border (clear) |
| 011 | No Border (clear) |
| 100 | Blue |
| 101 | Green |
| 110 | Red |
| 111 | White |

Test Mode/Main Vertical and Horizontal Polarity Register

Sub-address = 03h

Internal Test Mode Register (ITM0–2) – D0–D2

Sets the Multi Test Pin output to provide one of several internal signals for test and production alignment. Also controls the test memory address counter.

| ITM (2:0) | Multi-Test I/O and Function |
|-----------|-----------------------------|
| 000 | Input – Analog Test mode |
| 001 | Input – Digital Test mode |
| 010 | Output – Sync Detect |
| 011 | Output – PIP Switch |
| 100 | Output – PIP H Detect |
| 101 | Output – PIP V Detect |
| 110 | Output – PIP Clamp |
| 111 | Output – Main Clamp |

Main vertical polarity select bit (MVP0) – D6

Selects polarity of active level of vertical reference input. 0 = positive going, 1 = negative going.

Main horizontal polarity select bit (MHP0) – D7

Selects polarity of active level of horizontal reference input. 0 = positive going, 1 = negative going.

PIP Freeze/PIP Size/Main and PIP Video Source Register

Sub-address = 04h

LIVE PIP Select Bits (LIVE_P0–1) – D0–D1

Selects which of the multiple PIP pictures is the active “live” one.

| LIVE_P (1:0) | 1/16 Size | 1/9 Size |
|--------------|---------------------|---------------------|
| 00 | Top = LIVE | Top = LIVE |
| 01 | 2nd from Top = LIVE | 2nd from Top = LIVE |
| 10 | 3rd from Top = LIVE | 3rd from Top = LIVE |
| 11 | 4th from Top = LIVE | 3rd from Top = LIVE |

PIP Freeze Bit (STILO) – D4

When set to one, the most recently received field is continuously displayed until the freeze bit is cleared.

PIP Size Bit (PSI90) – D5

Switches the PIP size between 1/16 main size (when 0) and 1/9 main size (when 1).

Main Video Source Select Bit (MSEL0) – D6

Selects which video input will be applied to the PIP switch as the main video out.

PIP Video Source Select Bit (PSEL0) – D7

Selects which video input will be applied to the video decoder to provide the PIP video.

| MSEL/PSEL | Function |
|-----------|--|
| 0 | Video 1 Input to Main/ Video 1 Input to PIP |
| 1 | Video 2 Input to Main/ Video 2 Input to PIP |

PIP On/PIP Blank Register

Sub-address = 05h

PIP On Bits (PON0–3) – D4–D3

When on (1) turns the corresponding PIP display on.

| PON (3:0) | 1/16 Size | 1/9 Size |
|-----------|-------------------|-------------------|
| 0000 | No PIP | No PIP |
| 0001 | Top = On | Top = On |
| 0010 | 2nd from Top = On | 2nd from Top = On |
| 0100 | 3rd from Top = On | 3rd from Top = On |
| 1000 | 4th from Top = On | 3rd from Top = On |

PIP Blanking Bits (PBL0–3) – D4–D7

When on (1) sets the corresponding PIP to black. If the individual PIP is off, then it will be black when it is turned on.

| PBL (7:4) | Function |
|-----------|---------------------------------------|
| 0000 | PIP Picture Normal |
| 0001 | Top = Blanked (Set to Black) |
| 0010 | 2nd from Top = Blanked (Set to Black) |
| 0100 | 3rd from Top = Blanked (Set to Black) |
| 1000 | 4th from Top = Blanked (Set to Black) |

PIP X Position Register

Sub-address = 06h

X Position Bits (XPS0–5) – D0–D5

Moves the PIP start position from the left to the right edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Y Position Register

Sub-address = 07h

Y Position Bits (YPS0–5) – D0–D5

Moves the PIP start position from the top to the bottom edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Chroma Level Register

Sub-address = 08h

Chroma (C0–5) – D0–D5

The color of the PIP can be adjusted to suit viewer preference by setting the value stored in these bits. A total of 64 steps varies the color from no color to maximum. This control acts in conjunction with the auto phase control.

PIP Tint Level Register

Sub-address = 09h

*Tint (T0–5) – D0–D5*An auto phase control compares the main color burst to the internally generated pseudo color burst so that the tints are matched. In addition to this, the tint of the PIP can be varied $\pm 10^\circ$ in a total of 64 steps by changing the value of these bits to suit viewer preference.**PIP Luma Delay Register**

Sub-address = 0Ah

Y Delay (YDL0–2) – D0–D2

Since the Chroma passes through a bandpass filter and the color decoder, it is delayed with respect to the Luma signal. Therefore, to time match the Luma and Chroma these

bits are set to a single value determined to be correct in the application.

PIP Acquire/Playback Register

Sub-address = 0Bh

PIP Acquire Speed Bits (ACQ_SP0–1) – D0–D1

These select the speed of the video acquisition. This is only active when RE_AQ = 1.

| ACQ_SP (1:0) | Function |
|--------------|----------------------------------|
| 00 | Acquire 1 Out of Every 4 Fields |
| 01 | Acquire 1 Out of Every 6 Fields |
| 10 | Acquire 1 Out of Every 8 Fields |
| 11 | Acquire 1 Out of Every 10 Fields |

PIP Save/Clear Bit (RE_AQ) – D2

This bit controls the save and clear function for the instant replay. The bit value 1 is only effective when PON0–3 = 0000. (No PIP display.)

| RE_AQ (2:2) | Function |
|-------------|-----------------|
| 0 | Save Memory |
| 1 | Clear Reacquire |

PIP Playback Speed Bits (PB_SP0–1) – D4–D5

These bits control the relative playback speed, to the acquired speed.

| PB_SP (5:4) | Function |
|-------------|--------------------------------|
| 00 | Playback at 1 x ACQ_SP Speed |
| 01 | Playback at 1/2 x ACQ_SP Speed |
| 10 | Playback at 1/4 x ACQ_SP Speed |
| 11 | Playback at 1/8 x ACQ_SP Speed |

PIP Playback Control Bit (PB) – D6

This bit controls the start/stop of the instant replay function.

| PB (6:6) | Function |
|----------|--------------------------|
| 0 | No Action |
| 1 | Instant Replay Activated |

PIP Fill/Background/Free Run/Test Register

Sub-address = 0Ch

PIP Fill Bits (PIPFILL0–1) – D0–D1

May be used to fill the PIP with one of three selectable solid colors

| PIPFILL (1:0) | Function |
|---------------|----------|
| 00 | Normal |
| 01 | Red |
| 10 | Green |
| 11 | Blue |

Test Register Bits (INTC0 and MACR0) – D6–D7

When the FRUN is set to 1 the circuitry provides a generated sync and displays a flat field that can be either dark blue or gray determined by the BGND bit.

| BGND (2:2) | Function |
|------------|-----------|
| 0 | Blue |
| 1 | 50% White |

MC44463

I²C REGISTER TABLE

| Sub-address | Data Bit | | | | | | | |
|-------------|----------|-------|--------|--------|------|-------|----------|----------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | RPS3 | RPS2 | RPS1 | RPS0 | – | WPS2 | WPS1 | WPS0 |
| 01 | – | – | – | VFON | PSD3 | PSD2 | PSD1 | PSD0 |
| 02 | – | – | – | – | – | BC2 | BC1 | BC0 |
| 03 | MHP0 | MVP0 | – | – | – | ITM2 | ITM1 | ITM0 |
| 04 | PSEL0 | MSEL0 | PSI90 | STIL0 | – | – | LIVE_P1 | LIVE_P0 |
| 05 | PBL3 | PBL2 | PBL1 | PBL0 | PON3 | PON2 | PON1 | PON0 |
| 06 | – | – | XPS5 | XPS4 | XPS3 | XPS2 | XPS1 | XPS0 |
| 07 | – | – | YPS5 | YPS4 | YPS3 | YPS2 | YPS1 | YPS0 |
| 08 | – | – | C5 | C4 | C3 | C2 | C1 | C0 |
| 09 | – | – | T5 | T4 | T3 | T2 | T1 | T0 |
| 0A | – | – | – | – | – | YDL2 | YDL1 | YDL0 |
| 0B | – | PB | PB_SP1 | PB_SP0 | – | RE_AQ | ACQ_SP1 | ACQ_SP0 |
| 0C | INTC | MACR | FRUN | – | – | BGND | PIPFILL1 | PIPFILL0 |

Function Control of the MC44463

There are three modes of operation; Single PIP, Multiple PIP and Replay. These are enabled by setting specific register bits in the I²C register set.

Single PIP (SPIP) Operation

Register 0Bh : D6 → 0

Register 05h : D0–D7 → 01h

Multiple PIP (MPIP) Operation

Register 05h : D0–D3 → 07h or 0Fh

Register 04h : D0–D1 → 0 to 3

Register 0Bh : D6 → 0

Register 0Ch : D5 → 1, D2 → 0 or 1 (Optional)

Replay PIP (RPIP) Operation

In sequence, the Capture Ready mode must be first activated, allowing up to 8 seconds of fill memory with the desired video stream. Then the Capture mode must be set, disabling further write to memory. The Capture data may be re–displayed at any time afterword.

Capture Ready

Register 05h : D0–D3 → 0

Register 0Bh : D6 → 0, D2 → 1, D0–D1 → 0 to 3

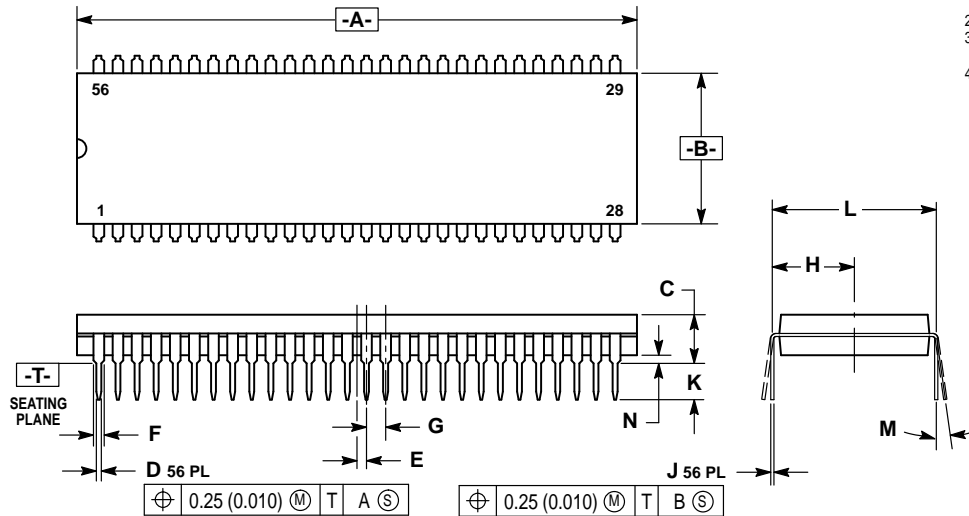
Capture

Register 0Bh : D6 → 1, D2 → 0, D4–D5 → 0 to 3

Register 05h: D0 → 1

OUTLINE DIMENSIONS


B SUFFIX
PLASTIC PACKAGE
CASE 859-01
(SDIP)
ISSUE O



NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.035 | 2.065 | 51.69 | 52.45 |
| B | 0.540 | 0.560 | 13.72 | 14.22 |
| C | 0.155 | 0.200 | 3.94 | 5.08 |
| D | 0.014 | 0.022 | 0.36 | 0.56 |
| E | 0.035 BSC | | 0.89 BSC | |
| F | 0.032 | 0.046 | 0.81 | 1.17 |
| G | 0.070 BSC | | 1.778 BSC | |
| H | 0.300 BSC | | 7.62 BSC | |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.600 BSC | | 15.24 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.02 |

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USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

