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MOTOROLA

MC44302A

Advanced Information

Advanced Multi-Standard TV Video/Sound IF

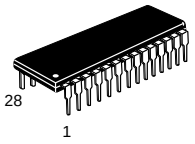
ADVANCED MULTI–STANDARD VIDEO/SOUND IF

SEMICONDUCTOR TECHNICAL DATA

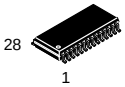
The MC44302A is a multi–standard single channel TV Video/Sound IF and PLL detector system specifically designed for use with all standard modulation techniques including NTSC, PAL, and SECAM. This device enables the designer to produce a high quality IF system with a minimum number of external components.

The MC44302A contains a high gain video IF with an AGC range of 80 dB, enhanced phase–locked loop carrier regenerator for low static phase error, doubly balanced full wave synchronous video demodulator featuring wide bandwidth positive and negative video outputs with extremely low differential gain and phase distortion, video AFT amplifier, multistage sound IF limiter with FM quadrature detector and AFT for self tuning, AM sound detector, constant and variable audio outputs, dc volume control for reduced hum and noise pickup, unique signal acquisition circuit that prevents false PLL lockup and AFT push out, horizontal gating system with sync separator and phase–locked loop circuitry for self–contained RF/IF AGC operation, RF AGC delay circuitry, and programmable control logic that allows operation in NTSC, and PAL SECAM systems. This device is available in wide body 28 pin dual–in–line and surface mount plastic packages.

- Multi–Standard Detector System for NTSC, PAL, and SECAM
- High Gain Video IF Amplifier with 80 dB AGC Range
- Enhanced PLL Carrier Regenerator for Low Static Phase Error
- Synchronous Video Demodulator with Positive and Negative Video Outputs
- Sound IF with Self Tuning FM Quadrature Detector
- AM Sound Detector
- DC Volume Control
- Unique Signal Acquisition Circuit Prevents False PLL Lockup
- Horizontal Gating System for Self Contained RF/IF AGC Operation
- RF AGC Delay Circuitry

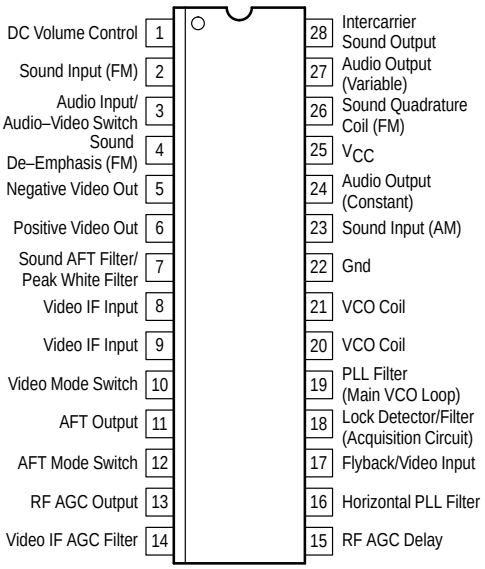


P SUFFIX
PLASTIC PACKAGE
CASE 710



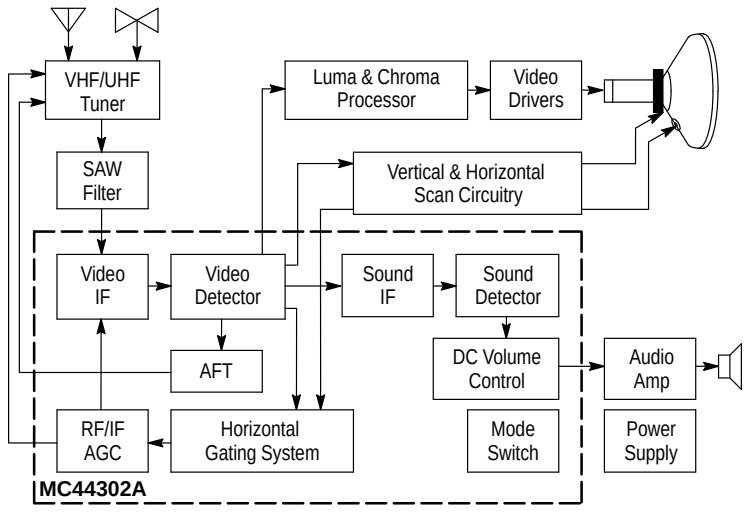
DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO–28L)

PIN CONNECTIONS



(Top View)

Simplified Television Block Diagram



ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC44302ADW	T_A = 0° to +70°C	SO–28L
MC44302AP		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	V
Input Voltage Range Video IF (Pins 8, 9) FM Sound IF (Pin 2) AM Sound IF (Pin 23) AFT Switch (Pin 12) Audio Input/Audio Switch/Video Invert (Pin 3) Mode Switch (Pin 10) RF AGC Delay (Pin 15) Volume Control (Pin 1)	V_{IR}	–0.3 to V_{CC}	V
Sound Quadrature Coil Voltage (Pin 26)	V_{QC}	V_{CC}	V
VCO Coil Voltage (Pins 20, 21)	V_{VCO}	V_{CC}	V
Flyback/Video Input Current (Pin 17)	I_{in}	±1.0	mA
Output Current Positive and Negative Video (Pins 5, 6) Intercarrier Sound (Pin 28) Constant and Variable Audio (Pins 24, 27) RF AGC, Internally Limited (Pin 13) AFT Source or Sink (Pin 11)	I_O	 15 15 15 2.0 4.0	mA
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package Case 751F Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 710 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 1000 80	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
VIDEO IF AMPLIFIER					
Differential Input Impedance Components Parallel Resistance Parallel Capacitance	 $R_{in(VIF)}$ $C_{in(VIF)}$	 – –	 3.4 4.0	 – –	 kΩ pF
Differential Input Voltage for Full Video Output Swing	$DV_{in(VIF)}$	–	40	–	μVrms
Automatic Gain Control Range	AGC_{VIF}	–	80	–	dB
Noise Figure (V_{in} = 1.0 mV, R_S = 300 Ω)	NF	–	7.0	–	dB
Bandwidth, –3.0 dB (R_S = 300 Ω)	BW_{VIF}	–	120	–	MHz
Sound Intercarrier Output, 4.5 MHz (V_{in} = 1.0 mV, Note 2)	$V_{O(Snd\ IC)}$	–	0.1	–	Vrms
VIDEO DETECTOR					
Output Voltage Swing (Pin 5 or 6, R_L = 2.0 k, Note 1)	$V_{O(VD)}$	–	2.2	–	Vpp
Output Impedance (Pin 5 or 6, 1.0 MHz, 1.0 mA)	$\|Z_O\|$	–	100	–	Ω
Bandwidth, –3.0 dB, (R_L = 2.0 k) Negative Output (Pin 5) Positive Output (Pin 6)	BW_{VD}	 – –	 8.0 7.0	 – –	MHz
Output Distortion, Uncorrected (R_L = 2.0 k, Note 1) Differential Gain Negative Video Output Positive Video Output Differential Phase Negative Video Output Positive Video Output	 DG DP 	 – – – –	 2.0 2.0 1.0 1.0	 5.0 5.0 5.0 5.0	 % Deg

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
VIDEO DETECTOR (CONTINUED)					
Residual 920 kHz Beat Output, dB Below 100% Modulated Video (Pin 5 or 6, Note 2)	B_O	–	–60	–	dB
FM SOUND IF AND DETECTOR					
Input Impedance Components					
Parallel Resistance	$R_{in(FM)}$	–	2.2	–	kΩ
Parallel Capacitance	$C_{in(FM)}$	–	4.0	–	pF
Input Limiting Threshold (f = 4.5 MHz)	$V_{in(Snd)}$	–	80	–	μV
AM Rejection (V_{in} = 10 mV, Notes 4, 5, 6)	AMR				dB
f = 4.5 MHz		–	50	–	
f = 5.5 MHz		–	50	–	
Recovered Audio Output (Pin 24, V_{in} = 10 mV, Note 4)	$V_{O(Snd)}$				Vpp
f = 4.5 MHz		–	2.0	–	
f = 5.5 MHz		–	2.0	–	
Output Distortion (Pin 24, V_{in} = 10 mV, Note 4)	THD				%
f = 4.5 MHz		–	1.0	–	
f = 5.5 MHz		–	1.0	–	
Sound AFT (Note 7)	$\Delta f_{AFT(Snd)}$				MHz
Pull–in Range		–	±0.6	–	
Hold–in Range		–	±0.6	–	
Sound De–Emphasis Internal Resistance (Pin 4)	R_{DE}	–	18	–	kΩ
AM Detector Crosstalk	$Ctlk_{AM}$	–	–6.0	–	dB
AM DETECTOR					
Input Impedance Components					
Parallel Resistance	$R_{in(AM)}$	–	5.6	–	kΩ
Parallel Capacitance	$C_{in(AM)}$	–	4.0	–	pF
Recovered Audio Output (Pin 24, V_{in} = 100 mV, Note 5)	$V_{O(Snd)}$	–	2.0	–	Vpp
Output Distortion (Pin 24, V_{in} = 10 mV, Note 5)	THD	–	1.0	–	%
FM Sound IF and Detector Crosstalk	$Ctlk_{FM}$	–	–60	–	dB
DC VOLUME CONTROL					
Volume Control Range (Pin 1, Pin 3 = V_{in})	$\Delta V_{O(Snd)}$	–	+12 to –70	–	dB
Output Signal at Minimum Volume Setting (Pin 1 = Gnd, Pin 3 = V_{in})	$V_{O(Snd)}$	–	1.0	–	mV
Video Detector Sync to Audio Channel Crosstalk	$Ctlk_{VD}$				dB
Fixed Output		–	–60	–	
Variable Output		–	–60	–	
Audio Channel Crosstalk	$Ctlk_{Snd}$				dB
Fixed Output to Variable Output		–	–60	–	
Variable Output to Fixed Output		–	–60	–	

NOTES: 1. V_{in} = 1.0 mVrms signal at 45.75 MHz with 75% modulated staircase at 3.58 MHz.
2. V_{in} = 100 μVrms signal at 41.25 MHz added to signal in Note 1.
3. Differential carrier level at video IF inputs to cause the negative detector output to go positive by 0.1 V from ground.
4. FM Modulation = ±25 kHz deviation at 1.0 kHz for 4.5 MHz intercarrier.
±50 kHz deviation at 1.0 kHz for 5.5 MHz intercarrier.
5. AM Modulation = 30% depth at 1.0 kHz for 4.5 MHz and 5.5 MHz intercarrier.
6. AM Rejection (dB) = $20 \log \frac{V_{O(FM)}}{V_{O(AM)}}$
7. Tested with 15 μH sound quadrature coil in parallel with 68 pF and 10 kΩ.
8. The AFT output can be disabled by leaving Pin 12 disconnected or by biasing it to the voltage level shown above. When disabled, the output will be internally clamped to one half of V_{CC}.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
PHASE–LOCKED LOOP					
Acquisition Circuit Filter Voltage (Pin 18)	$V_{PLL(Acq)}$				V
Unlocked with No–Signal		–	2.7	–	
Unlocked to Locked Sweep Range upon Signal Acquisition		–	1.2 to 4.3	–	
Locked, Final Static Condition		–	4.3	–	
VCO Filter Voltage (Pin 19)	$V_{PLL(VCO)}$				V
Unlocked		–	3.2	–	
Locked, Final Static Condition		–	3.2	–	
Video IF Lock–Up Time	$t_{IF(lock)}$	–	5.0	–	ms
HORIZONTAL GATING SYSTEM					
Sync Separator Input Threshold Voltage (Pin 17)	$V_{th(Sync)}$	–	3.4	–	V
PLL Filter Voltage, Locked or Unlocked with No–Signal (Pin 16)	$V_{PLL(Horiz)}$	–	2.9 ± 1.1	–	V
RF AGC					
RF AGC Delay Voltage Range (Pin 15)	$V_{AGC(DLY)}$	–	1.7 to 2.4	–	V
RF AGC Output Current (Pin 13)	$I_{O(sink)}$	1.0	2.0	–	mA
LOGIC CONTROL					
Mode Select Voltage Range (Pin 10)	$V_{th(Mode)}$				V
PAL 1		4.7 to 5.0	4.6 to 5.0	–	
PAL 2		3.5 to 4.1	3.4 to 4.2	–	
SECAM		2.3 to 2.9	2.2 to 3.0	–	
NTSC		0 to 0.3	0 to 0.4	–	
AFT Switch Threshold (Pin 12)	$V_{th(AFT)}$				
AFT Output, Pin 11, Sourcing when IF Frequency is Low		–	5.0	–	
AFT Output, Pin 11, Sinking when IF Frequency is Low		–	0	–	
AFT Output, Pin 11, Disabled (Note 8)		–	2.5	–	
Audio Switch/Video Invert Voltage Range (Pin 3)	$V_{th(AS/VI)}$				V
Audio 1, Internal Audio (AM or FM) appears at Pins 24 and 27, Positive Video appears at Pin 6, Negative Video appears at Pin 5		3.4 to 5.0	3.3 to 5.0	–	
Audio 2, Internal Audio (AM or FM) appears at Pin 24, External Audio appears at Pin 27, Positive Video appears at Pin 6, Negative Video appears at Pin 5		1.8 to 2.2	1.7 to 2.3	–	
Video 1, Internal Audio (AM or FM) appears at Pins 24 and 27, Positive Video appears at Pin 6, Negative Video appears at Pin 5		0.6 to 0.9	0.5 to 1.0	–	
Video 2, Internal Audio (AM or FM) appears at Pins 24 and 27, Positive Video appears at Pin 5, Negative Video appears at Pin 6		0 to 0.2	0 to 0.3	–	
TOTAL DEVICE					
Operating Voltage	V_{CC}				V
T_A = 25°C		4.5	5.0	5.5	
T_A = 0°C to 70°C		4.75	–	5.5	
Power Supply Current (V_{CC} = 5.0 V)	I_{CC}	–	100	–	mA

NOTES:
1. V_{in} = 1.0 mVrms signal at 45.75 MHz with 75% modulated staircase at 3.58 MHz.
2. V_{in} = 100 μVrms signal at 41.25 MHz added to signal in Note 1.
3. Differential carrier level at video IF inputs to cause the negative detector output to go positive by 0.1 V from ground.
4. FM Modulation = ±25 kHz deviation at 1.0 kHz for 4.5 MHz intercarrier.
   ±50 kHz deviation at 1.0 kHz for 5.5 MHz intercarrier.
5. AM Modulation = 30% depth at 1.0 kHz for 4.5 MHz and 5.5 MHz intercarrier.
6. AM Rejection (dB) = $20 \log \frac{V_{O(FM)}}{V_{O(AM)}}$
7. Tested with 15 μH sound quadrature coil in parallel with 68 pF and 10 kΩ.
8. The AFT output can be disabled by leaving Pin 12 disconnected or by biasing it to the voltage level shown above. When disabled, the output will be internally clamped to one half of V_{CC}.

Figure 1. IF AGC Filter Voltage versus Carrier Differential Input Voltage

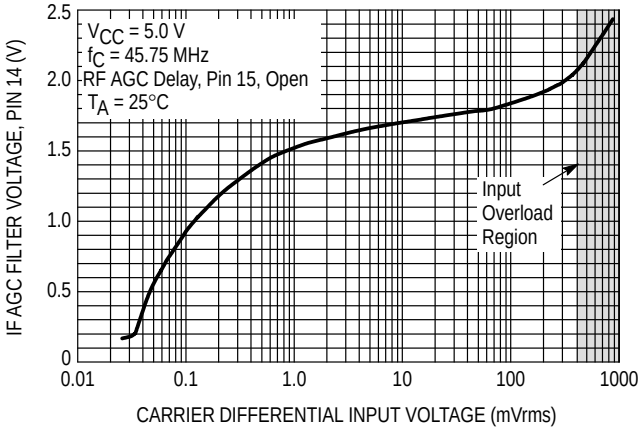


Figure 2. Carrier Differential Input Voltage versus RF AGC Takeover Threshold

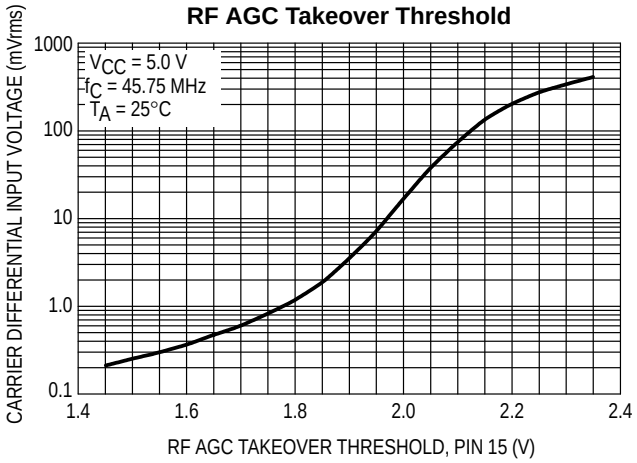


Figure 3. VCO Characteristics

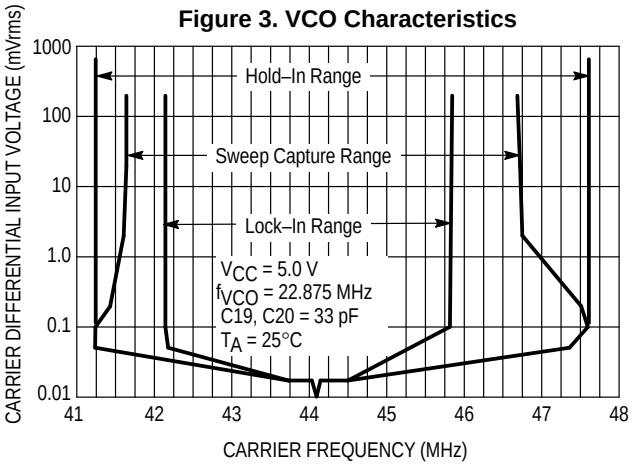


Figure 4. VCO Free–Running and Offset Frequency Change versus Supply Voltage

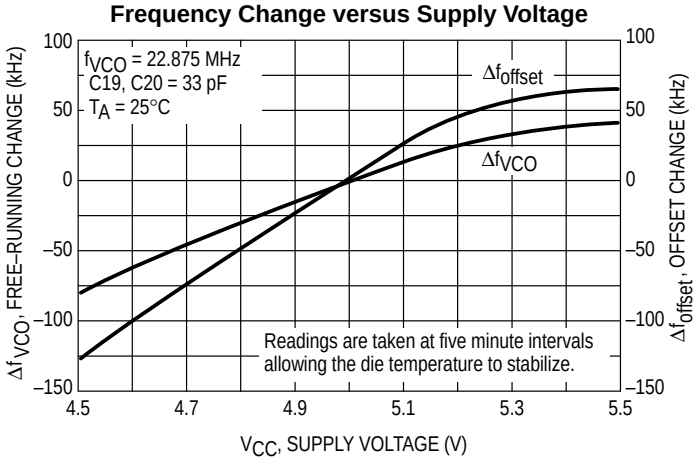


Figure 5. PLL Filter Voltage versus Carrier Frequency Change

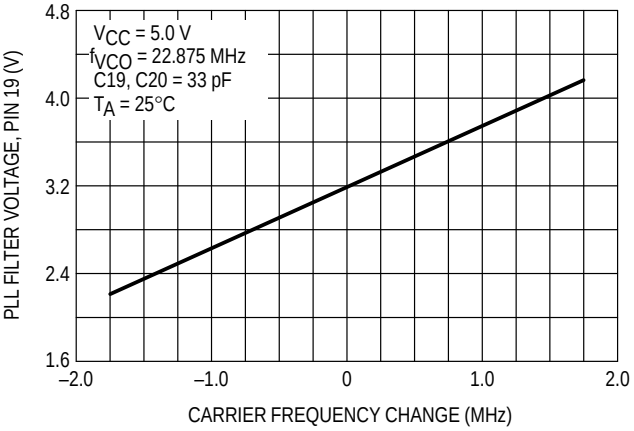


Figure 6. AFT Output Current versus Carrier Frequency Change

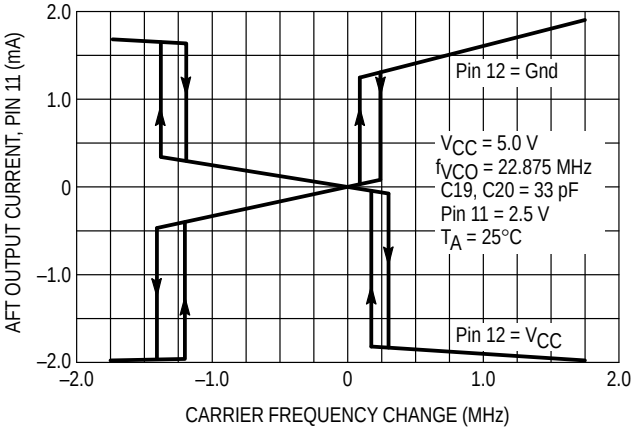


Figure 7. Video Output Frequency Response

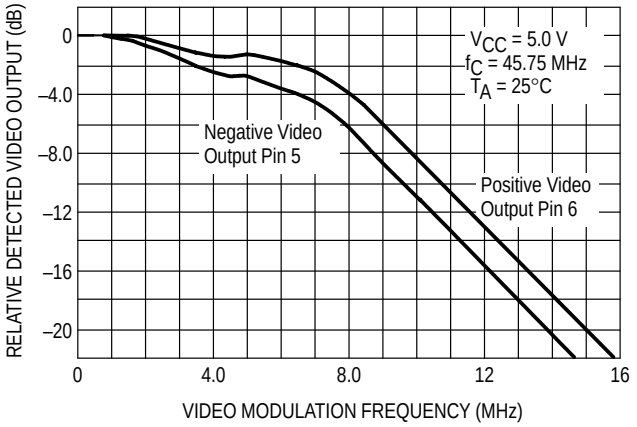


Figure 8. Vectorscope Display of 75% Saturated NTSC Color Bars

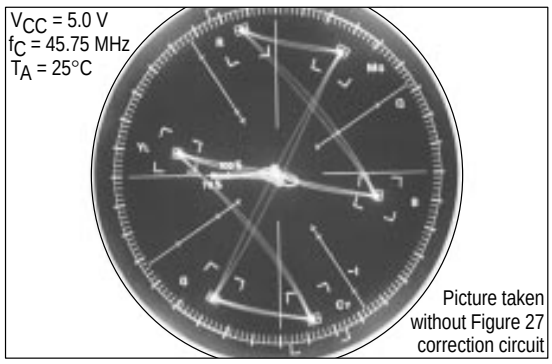


Figure 9. FM Sound AFT Filter Voltage versus Internal Tuning Capacitance

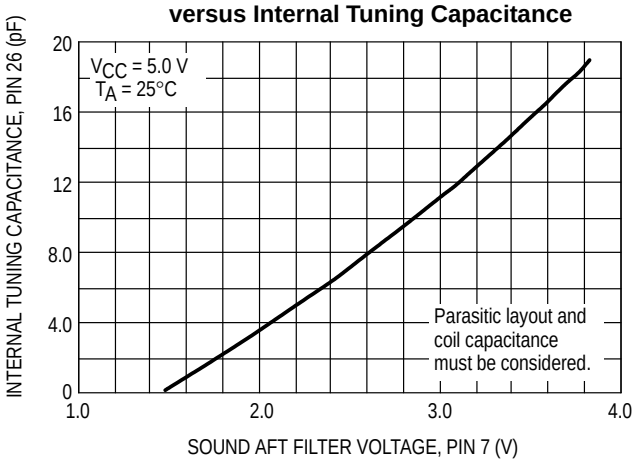


Figure 10. FM Sound Intercarrier Self–Tuning Frequency Range versus External Tank Capacitance

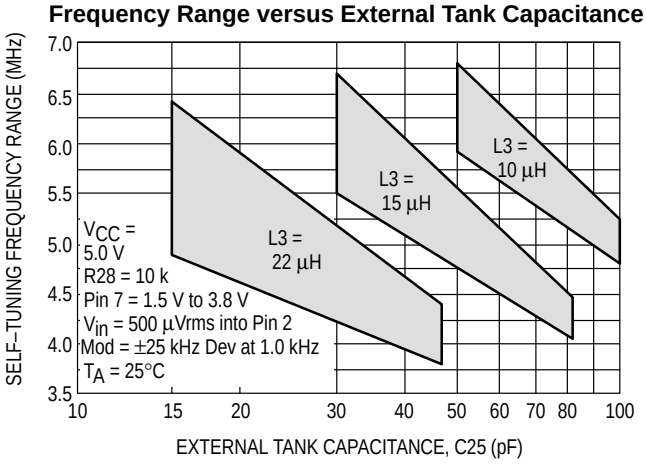


Figure 11. FM Sound Detector Relative Output, and Signal to Noise Ratio versus Intercarrier Input Voltage

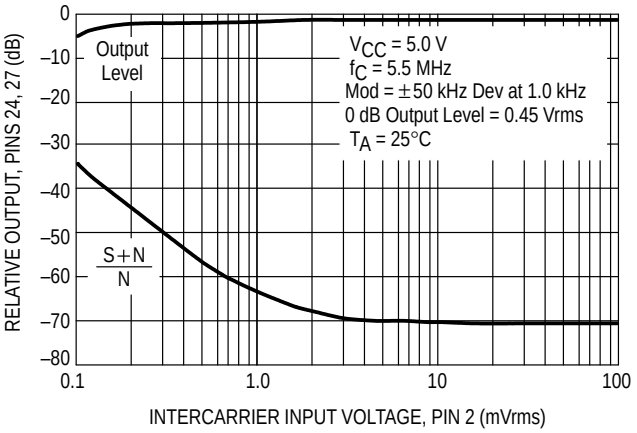


Figure 12. FM Sound Detector Frequency Response

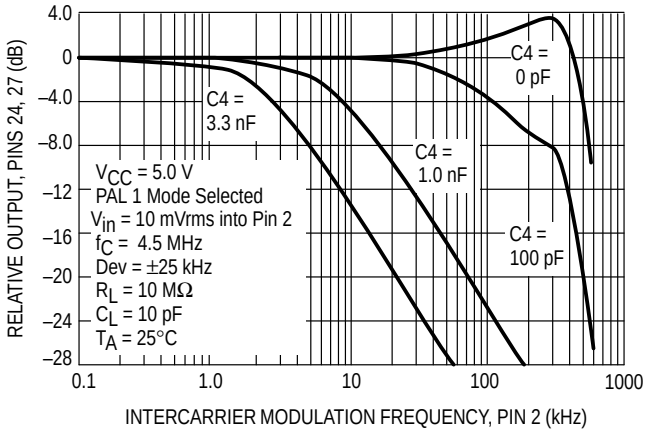


Figure 13. AM Sound IF Frequency Response

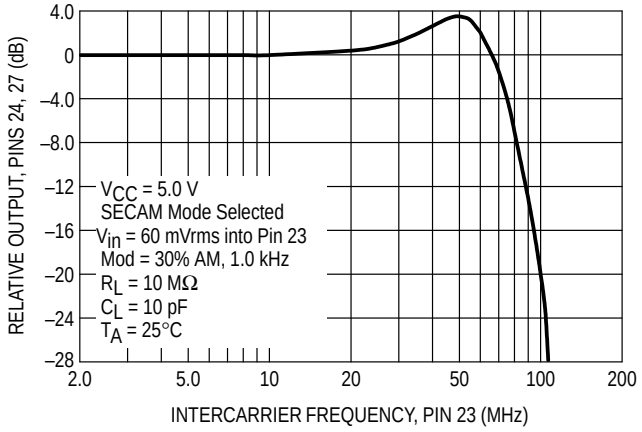


Figure 14. AM Sound Detector Frequency Response

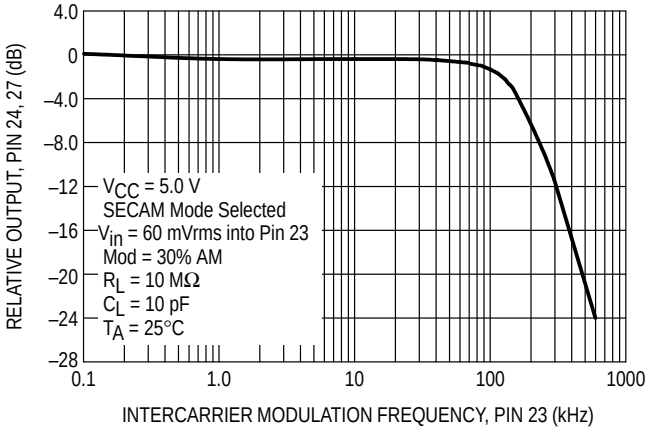


Figure 15. AM Sound Detector Linearity

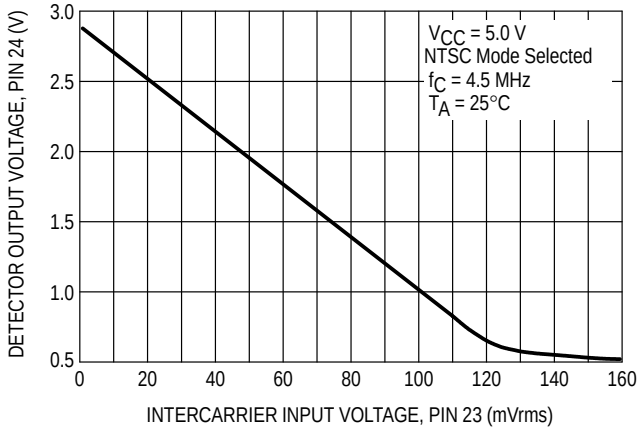


Figure 16. Variable Audio Output Frequency Response

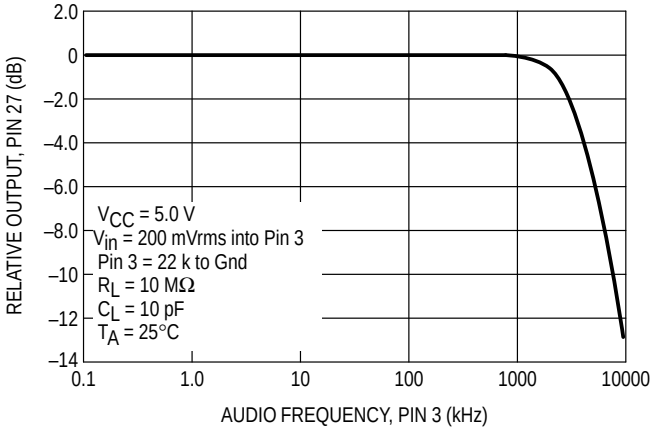


Figure 17. Variable Audio Output Gain versus Volume Control Voltage

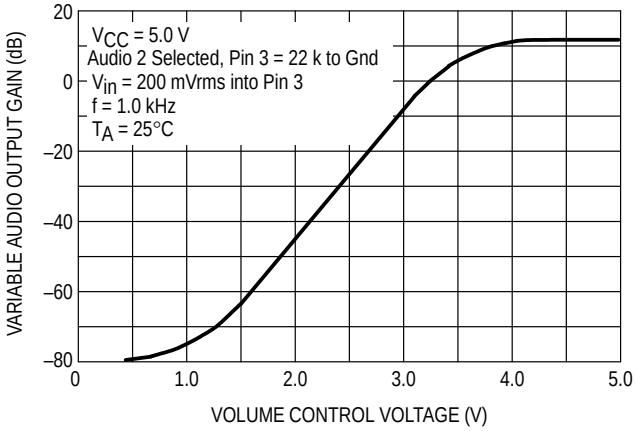


Figure 18. Supply Current Versus Supply Voltage

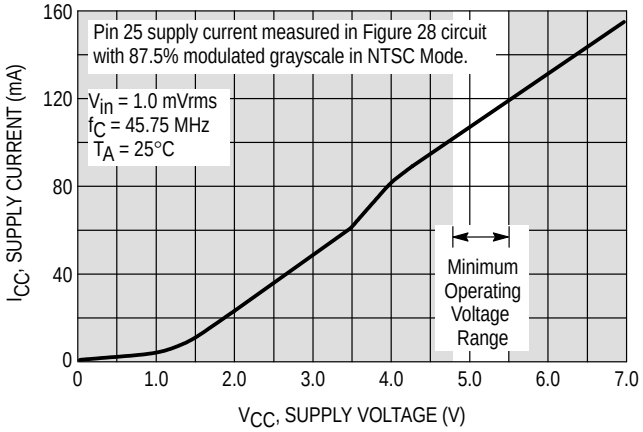
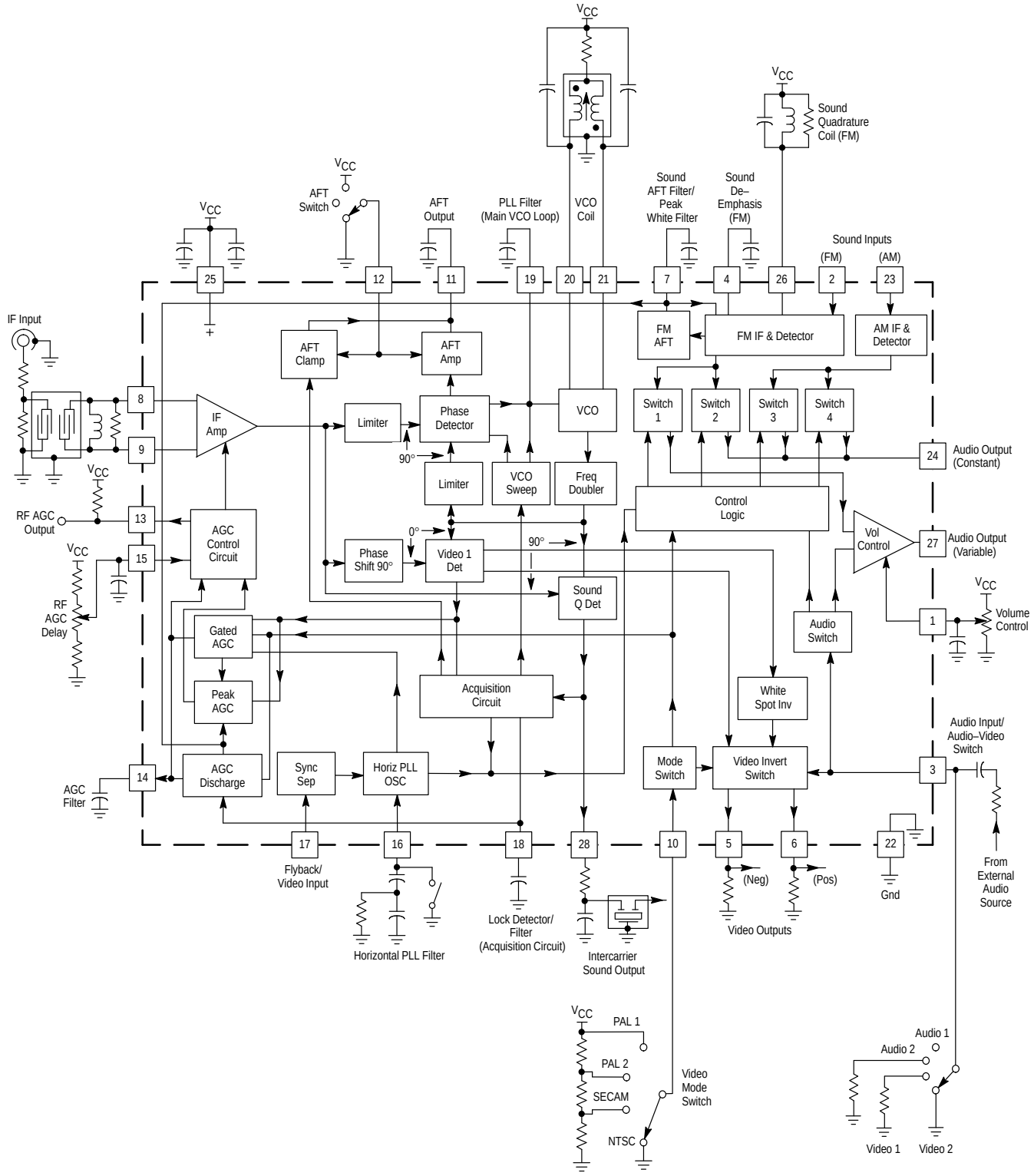


Figure 19. Representative Block Diagram



This device contains 2,641 active transistors.

FUNCTIONAL DESCRIPTION

Introduction

The MC44302A is an advanced high performance multistandard IF system specifically designed for use with all of the world's major television modulation techniques including NTSC, PAL, and SECAM. This device performs the function of intermediate frequency (IF) amplification, automatic gain control (AGC), automatic frequency tuning (AFT) and signal demodulation for transmitting systems that use either positive or negative amplitude modulated video along with frequency modulated (FM) or amplitude modulated (AM) sound. The television designer is offered a new level of circuit simplicity along with enhanced system performance when compared to present day television IF amplifiers. Numerous unique design techniques are incorporated resulting in only a single tuned circuit adjustment for a completely aligned video and sound IF system with tuner AFT output. Special design attention was given to enhance noise performance and to reduce differential gain and phase distortion. Additional internal circuitry is provided to meet the European Peritel socket requirements along with a means for descrambling video signals that use either or both amplitude modulated sync and alternate line video inversion. A detailed block diagram of the internal architecture is shown in Figure 19 and an operating description of the major circuit blocks is given below.

IF Amplifier and AGC

The IF amplifier consists of four cascaded ac coupled gain stages yielding an input sensitivity of 40 μV for a full video output swing of 2.2 Vpp. This level of sensitivity allows the use of a single IF block filter without incurring the additional cost of a preamplifier. A quite acceptable level of signal to noise performance is achievable by utilizing a tuner with a gain of 33 dB to 36 dB combined with a low insertion loss (≤18 dB) surface acoustic wave (SAW) or passive block filter. The first three stages of the IF amplifier are gain controlled to provide an AGC range of 80 dB. This extended AGC range enhances the signal handling capability, resulting in superior differential phase and gain performance with a significant reduction of intermodulation products. AGC of the first stage is internally delayed so as to preserve the amplifier's low noise figure characteristics.

An on–chip sync separator and horizontal phase–locked loop oscillator is provided for noise immune AGC gating in self contained applications where a horizontal scan signal may not be available. A positive going sync source connected to the Flyback/Video input at Pin 17 is used to lock the PLL and generate an internal AGC keying pulse. The sync separator allows direct use of the Negative Video output at Pin 5 as a source for the keying pulse. If horizontal scan circuitry is available, a positive going flyback pulse can also be used to set the keying pulse.

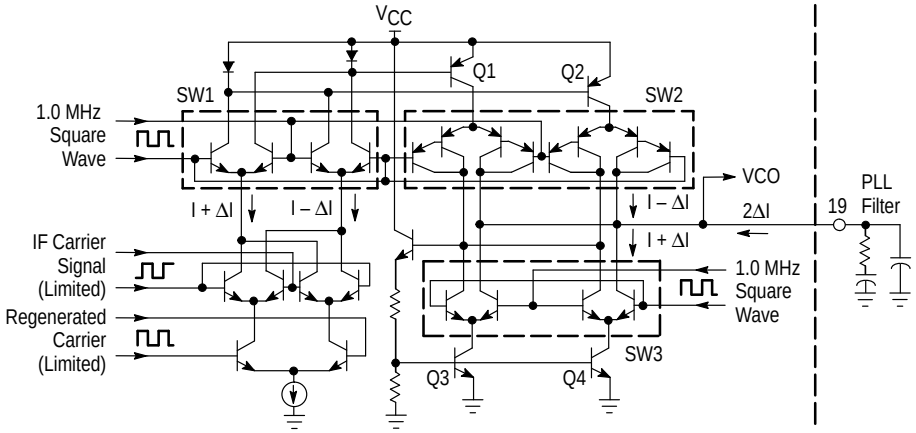
A video signal and a reference level are required to implement automatic gain control of the IF and tuner. The video AGC reference is selected for a specific modulation standard by the Video Mode Switch voltage setting at Pin 10; refer to Table 2. With PAL 1, PAL 2, or NTSC mode selected, a black level reference is established by AGC keying during the tip of sync. With SECAM mode selected, a black level reference is established by AGC keying during the back porch. In order to correct for the inconsistent back porch level that is common between SECAM transmitters, a long time constant non–keyed peak white reference level is also established, and is used in conjunction with the black level reference to control the video output level. The peak white level is used in effect to slowly readjust the black level reference threshold over a limited range of ±10%. With this dual reference approach, the accuracy associated with a typical peak white detecting system is maintained without the usual sacrifice of speed, thus allowing a quick AGC response to airplane flutter and channel changes.

The tuner AGC control function consists of an RF AGC delay adjustment at Pin 15 and an RF AGC output at Pin 13. The delay adjustment sets the threshold where tuner gain reduction is to begin. This usually corresponds to a signal level of 1.0 mV to 2.0 mV at antenna input. The AGC output is designed to control a reverse AGC type of tuner. As the antenna signal level increases, the voltage at Pin 13 decreases, causing a gain reduction in the tuner. Since Pin 13 is an NPN open collector output, an external pull–up resistor must be added if one is not provided in the tuner. Pin 13 is guaranteed to sink a minimum of 1.0 mA. Note that when operating with a tuner that requires in excess of 5.6 V, current will flow into Pin 13 due to conduction of the upper internal clamp diode.

Carrier Regeneration

Carrier regeneration is attained by the use of a phase–locked loop, thus enabling true synchronous demodulation to be achieved with all of its advantages. Following the IF amplifier and preceding the PLL phase detector is a limiting amplifier designed to remove the amplitude modulation that is present on the carrier. The amplifier consists of two cascaded differential stages with direct coupled feedback to set a closed loop gain of 40 dB. This two stage approach has several distinct advantages when compared to conventional integrated demodulators that utilize a single stage limiter. With a two stage limiter, the gain requirement to remove the video amplitude modulation can be designed–in without the large voltage swings that are required by a single stage limiter with equivalent gain. The large voltage swings lead to poor differential phase and gain performance, and consequently the need for an external tuned circuit with two cross coupled limiting diodes. Use of direct coupled feedback diminishes the effects of the amplifier's input offset voltage which can be an additional source for differential phase and gain errors. The combination of low voltage swing per stage with dc feedback eliminates the need for a tuned circuit at the output of the limiter. This results in a significant component and alignment cost savings as well as removing the necessity to pin out a high level IF signal. This high level signal is a potential radiation source that can result in IF instability at low signal levels. The only problem of using the two stage limiter is the potential for an additional static phase shift which will result in a change of the demodulating angles at both the video and sound demodulators inputs. This problem is solved by placing an identical two stage limiter between the frequency doubler output and the phase detector input. This adds an identical amount of static phase shift to bring the demodulating angles back to 0° and 90°.

Figure 20. Phase Detector

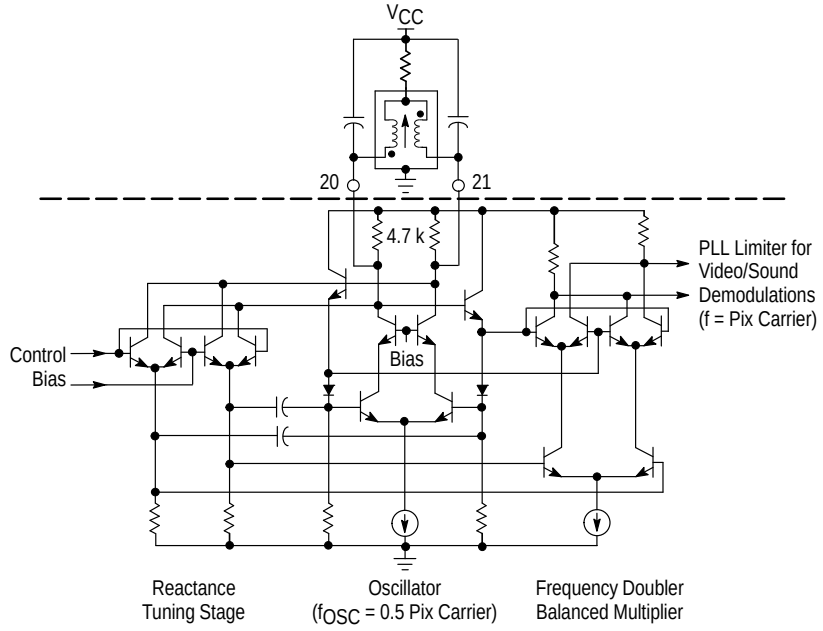


Phase errors, resulting in quadrature video distortion, can also be caused by dc errors in the phase detector and AFT amplifier. Most of the dc offsets are caused by mismatches in the current mirrors of the push–pull output stage, refer to Figure 20. Switches SW1, SW2, and SW3 are driven by a 1.0 MHz square wave with an accurate 1:1 mark/space ratio. Switches SW1 and SW2 maintain the same sense of error signal, while SW2 ensures errors due to the top PNP current mirrors average to zero on the external loop filter capacitor. In a similar way, SW3 by interchanging Q3 and Q4, cancels errors due to the bottom NPN mirror. With phase errors reduced to a minimum, there is no need for any external phase adjustments. The phase detector output is filtered and it is used to control the VCO in a corrective manner. When the PLL establishes a locked condition, there will be a 90° phase shift between the two phase detector inputs.

The Voltage Controlled Oscillator and Frequency Doubler circuits are shown in Figure 21. The oscillator operates at one half of the picture carrier frequency and is tuned by a control bias that is applied to the reactance stage input. Reactance tuning allows a higher Q to be maintained in the tank circuit as opposed to a phase shift type of oscillator with the same tuning range. The oscillator frequency is internally doubled to picture carrier frequency by a balanced multiplier. Note that the multiplier input signals are at 90° to each other for frequency doubling.

Since the oscillator operates at one half of the picture carrier frequency, radiation from the external tuned circuit components will not desensitize the system, even if picked up by the amplifier input leads. This significantly reduces the possibility of a PLL push–off condition. Running the oscillator at twice the picture carrier and dividing it down is another way of solving the IF input radiation problem, but there are two significant disadvantages. First and foremost, radiation into the antenna now becomes a problem. In the U.S.A. twice the picture carrier falls directly into the passband of channel 6, producing a very noticeable beat. Any second order harmonics, four times picture carrier, will fall into the passband of channel 8. Second, it is more difficult to produce a stable oscillator that operates at twice the IF frequency than one that operates at one half of the IF frequency.

Figure 21. VCO and Frequency Doubler

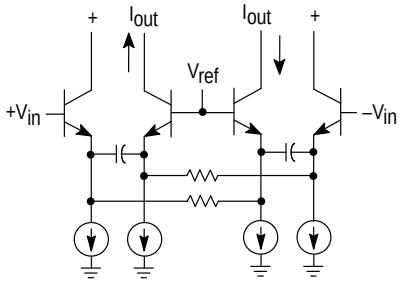


Video and Sound Intercarrier Demodulation

To ensure that the above performance improvements were not lost elsewhere, great care was taken with the design of the video demodulator and video amplifiers. One example is in the architectural placement of the phase shift amplifier (Figure 22) that is required for video demodulation. This amplifier was placed in series with the IF signal side of the demodulator, instead of the oscillator side as is common practice. The 90° phase shift is obtained by a capacitively coupling each of the differential amplifier driver emitters to the video demodulator inputs. This results in an output current that is at 90° with respect to the input voltage over a wide range of frequencies. Small phase errors that are caused by the transistor dynamic small–signal emitter resistance are corrected with the use of cross–coupled emitter resistors. This arrangement leads to a simpler design with the ability to tailor the demodulation angle for the lowest possible distortion at the IF/demodulator interface. The dynamic emitter resistances, which can give rise to distortion, are now in quadrature with the capacitive reactance and therefore contribute very little to the resultant output.

After the PLL attains phase–lock, video and sound demodulation is obtained by the use of two separate double balanced multipliers. Video demodulation is accomplished by multiplying the non–limited 90° phase shifted carrier signal, with the regenerated vision carrier that is obtained from the Frequency Doubler output. Both positive and negative video outputs are produced. The phase relationship between the video demodulator inputs is 0° since the carrier signal is phase shifted 90°. This is done in order to cancel out the 90° phase shift that is present at the inputs of the Phase Detector when it is locked. The sound intercarrier signal is also recovered by a multiplier in a similar manner to that of the video. In this case the carrier signal is not phase shifted, and the phase relationship between the sound demodulator inputs is 90°. A consequence of this phase relationship is that only the higher frequency video components are demodulated while the lower frequency components, those that fall within the vestigial sideband, are suppressed. With negative polarity modulation systems, a significant reduction in the level of white character sound buzz and hum is achieved. This is most noticeable when demodulating video signals that contain a high luma level which can cause the modulation index to exceed 100 percent.

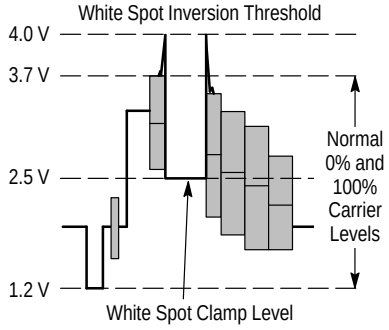
Figure 22. 90° Phase Shift Amplifier



Video Outputs

Each of the video outputs are part of a wide bandwidth operational amplifier with internal dc feedback and frequency compensation. The AGC reference provides the same composite video output level of approximately 2.2 Vpp for both positive and negative polarities of video modulation. The positive video output appears at Pin 6 and is intended to drive the luma and chroma channels. This output contains a White Spot Inverter that is used to invert and clamp any demodulated noise that is significantly above the white level. This effectively removes the whiter than white noise produced by the true synchronous demodulator and prevents the CRT from being overdriven and defocused. The white spot inversion threshold and clamp levels are set to approximately 4.0 V and 2.5 V respectively. The negative video output appears at Pin 5 and is intended to be used as a sync separator source. With a simple preseparator low pass noise filter, this output will provide optimum sync performance. The video outputs are designed to drive a resistive load that is in the range of 2.0 kΩ. Lower resistance values could increase differential phase and gain distortion.

Figure 23. Positive Video Output with White Spot Inversion



AM & FM Sound IF and Detection

The intercarrier sound that is present at Pin 28 normally connects through a ceramic bandpass filter to either the FM IF and Detector input at Pin 2, or the AM IF and Detector input at Pin 23. With the FM IF, intercarrier sound is limited by a five stage ac coupled amplifier yielding high sensitivity and a high level of AM rejection. The typical limiting threshold is 80 μV, and the AM rejection ratio is in excess of 50 dB. FM detection is accomplished by a self tuning quadrature demodulator. An internal reactance stage with phase compensation is controlled to automatically adjust the tuning of an external tank circuit eliminating the need for manual alignment. The tank is a parallel circuit consisting of a fixed value inductor, capacitor, and resistor. The tuning range is controlled by the ratio of the internal capacitance change to that of the fixed external tank capacitance. The internal capacitance is controlled by the voltage present on the Sound AFT Filter, Pin 7. The capacitance ranges from 0.25 pF to 19 pF, refer to Figure 9. Figure 10 shows the self tuning frequency range for three inductor values. In general, for fixed frequency applications, the external tank capacitance should be in the range of 56 pF to 82 pF. This should allow sufficient tuning range to account for the component tolerances. The L–C values should be selected so that the AFT filter operates below 2.4 V when properly tuned to the sound intercarrier. This yields the best low signal lock–in performance, since the AFT filter voltage approaches 1.0 V under no signal conditions. Multi–standard applications that require a wide intercarrier tuning range can be accomplished by using a small external capacitance with a

large inductance. Parasitic layout and coil capacitance must be considered for optimum performance. Suggested component values are given in Table 3.

The sound AFT time constant is set by an external capacitor that is connected from Pin 7 to ground. This capacitor is driven by an internal 300 μA current source and sink. The demodulated sound bandwidth is in excess of 100 kHz making this device well suited for MTS (multi–channel television sound) stereo and SAP (second audio program) TV applications. Sound de–emphasis is controlled by the time constant of an internal 18 kΩ resistor and an external capacitor that is connected from Pin 4 to ground. The FM IF is active in PAL 1, PAL 2 and NTSC modes, and provides 2.0 Vpp of audio at the Variable and Constant outputs.

With the AM IF, intercarrier sound is amplified and detected by a fully balanced exalted carrier demodulator. The detector provides in excess of 2.0 Vpp recovered audio output at Pin 24. An internal low pass filter is incorporated to suppress any high frequency harmonics that may be present at the demodulator output. The AM IF is active in both the SECAM and NTSC modes.

Audio Input/ Audio–Video Switch

The Audio Input/Audio–Video Switch is a multifunction input that selects the source for the audio that appears at Pin 27, and the polarity of the video that appears at Pins 5 and 6. There are four possible modes for this input and they are each selected by applying a specific dc voltage level to Pin 3. Refer to Table 1 and to the circuit description for Pin 3 in Table 3. Audio 1 is intended for applications where internally demodulated audio is present at the Variable and Constant outputs. The Variable output can be used internal to the TV chassis and the Constant output can be connected to a jack for earphone or recorder use. Audio 1 is selected by not having a dc path from Pin 3 to ground. Internally demodulated audio (AM or FM) will appear at Pins 24 and 27, negative video at Pin 5, and positive video at Pin 6. If there is an ac coupled audio source present at Pin 3, it will be internally disconnected. Audio 2 is intended for European applications where internal and external audio sources must be routed through the Peritel socket. Internally demodulated audio present at the Constant output can be routed out the Peritel socket while external audio can be routed in, ac coupled to Pin 3, and level adjusted at Pin 1 for use within the TV chassis. Audio 2 is selected by connecting a 22 kΩ resistor from Pin 3 to ground. Internally demodulated audio (AM or FM) appears at Pin 24, negative video at Pin 5, positive video at Pin 6, and the ac coupled external audio source at Pin 3 appears at Pin 27 inverted. The audio level into Pin 3 must be limited so that the selected mode of operation is not changed during the peak excursions with Audio 2 selected, and the valley excursion with Audio 1 selected. With the component values shown in Table 3, the audio level should be limited to less than 1.1 Vrms. Video 1 and 2 modes provide a simple means to recover scrambled video in systems that use some form of alternate line video inversion. Descrambling is accomplished by switching between the two video modes. Video 1 is selected by connecting a 3.3 kΩ resistor from Pin 3 to ground. Internally demodulated audio (AM or FM) will appear at Pins 24 and 27, negative video at Pin 5, and positive video at Pin 6. Video 2 is enabled when Pin 3 is grounded, usually by an IC or a transistor that is gated on alternate or multiple lines. Internally demodulated audio (AM or FM) appears at Pins 24 and 27, positive video with white spot inversion at Pin 5, and negative video at Pin 6. Note that Video 1 mode is identical to Audio 1. Video 1 is provided so that when descrambling, Pin 3 does not have to pass through the voltage range that selects Audio 2. This prevents unwanted switching noise and buzz from appearing at the audio outputs.

It should be noted that when combining the features of Pin 3 with the Peritel socket, the TV chassis can provide the audio and video source to drive an external monitor or video recorder. Also an externally generated audio and video source can be used to drive the TV chassis as a monitor.

DC Volume Control

The dc volume control consists of an electronically controlled audio amplifier that has a range of 12 dB gain, to 60 dB attenuation. The audio output level is set by applying a control voltage to Pin 1. This can be derived from an electronic source such as a digital to analog converter, or a manual source such as the wiper of a potentiometer that is connected from V_{CC} to ground. The potentiometer should be 20 kΩ or less. Because no audio signal is present on Pin 1, any potential for hum and noise pickup can easily be bypassed by connecting a capacitor from this pin to ground. In most cases, an unshielded wire or printed circuit board trace is all that is required to connect the variable voltage source to the IF board.

Table 1. Audio Input/Audio–Video Switch

Inputs to Pin 3			Outputs			
			Audio[1]		Video	
Mode	AC Signal	DC Level (V_{CC} = 5.0 V)	Constant Pin 24	Variable[2] Pin 27	Negative Pin 5	Positive Pin 6
Audio 1	External Audio	Open or 3.4 V to 5.0 V	Internal Audio (AM or FM)	Internal Audio (AM or FM)	Negative Video	Positive Video with White Spot Inversion
Audio 2	External Audio	22 kΩ to Ground or 1.8 V to 2.2 V	Internal Audio (AM or FM)	External Audio	Negative Video	Positive Video with White Spot Inversion
Video 1	–	3.3 kΩ to Ground or 0.6 V to 0.9 V	Internal Audio (AM or FM)	Internal Audio (AM or FM)	Negative Video	Positive Video with White Spot Inversion
Video 2	–	Grounded or 0 V to 0.03 V	Internal Audio (AM or FM)	Internal Audio (AM or FM)	Positive Video with White Spot Inversion	Negative Video

NOTES: 1. Refer to Table 2 to determine the active demodulator (AM and or FM) and the associated audio output pins.
2. The Variable output audio level is controlled by Pin 1.

Table 2. Television Standard Modes

Television Standard		Mode Selection		AGC		Sound		
						IF and Modulation		Audio Output Pin #
System	Video Modulation Polarity	Pin 10 Voltage (V)	Pin 16 DC Loading	Reference and Method	Time Constant Pin #	Active	Inhibited	
PAL 1	Negative	4.0 to 5.0	Open	Black Level Sync Tip Keyed	14	FM	AM	24, FM 27, FM
PAL 2	Negative	3.2 to 4.0	Open	Black Level Sync Tip Keyed	14	FM	AM	24, FM 27, FM
SECAM	Positive	1.9 to 3.0	Open	Black Level Back Porch Keyed White Level Peak Detected Video	14 7	AM	FM	24, AM 27, AM
NTSC	Negative	Ground	Open	Black Level Sync Tip Keyed	14	AM & FM	–	24, AM 27, FM

Multi–Standard Operating Modes

The MC44302A is designed to operate properly with PAL (B, G, I,) SECAM (L), and NTSC (M) television transmission standards. There are two multifunction inputs that are used to select the proper control methods for video demodulation, sound intercarrier demodulation, and AGC. This keeps the sense of the video signal at the outputs the same, whether positive or negative modulation is being received. Refer to Table 2 and the following operating description.

The PAL, NTSC, and SECAM standard are each selected by applying a specific dc voltage level to the Video Mode Switch at Pin 10. With PAL 1 selected, AGC is keyed on the sync pulse by the horizontal PLL which is locked to the flyback or video sync pulse present at Pin 17. The FM sound IF and detector is active with the demodulated audio appearing at Pins 24 and 27. The PAL 2 selection is identical to PAL 1 with the addition of sound muting when the Acquisition Circuit is unlocked or vertical sync is absent. With SECAM selected, the video level is established by both, a long time constant peak white detector, and a back porch keyed AGC that corrects for transmitted black level errors while maintaining fast AGC response. The AM sound detector is active with the demodulated audio appearing at Pins 24 and 27. With NTSC selected, AGC and sound muting is the same as for PAL 1 mode. The FM and AM detectors are both active with the FM output at Pin 27 and the AM output at Pin 24. The AM output can be used to obtain the sync signal, in suppressed sync scrambling systems, that is amplitude modulated on the sound carrier.

Signal Acquisition and AFT

The automatic fine tuning (AFT) portion of this integrated circuit is unconventional in form. AFT control is derived by amplifying the phase detector error voltage and applying it to the tuner local oscillator (LO) after phase lock is established. This method eliminates the need for a discriminator coil along with the associated alignment, and the potential for IF instability due to coil radiation.

The MC44302A is unique in that it uses the VCO loop as a frequency reference for the tuner AFT loop. After signal acquisition and phase lock, the VCO and AFT loops will reach a steady state condition. The VCO will have moved only a small amount from it's nominal frequency (Δf_{VCO}) with the tuner local oscillator (Δf_{LO}) correcting for the majority of the frequency error (Δf_e). Therefore in steady state condition $\Delta f_e = \Delta f_{VCO} + \Delta f_{LO}$, and $\Delta f_{LO} >> \Delta f_{VCO}$. This is due to the much higher gain in the tuner LO loop when compared to that of the VCO loop. In this way, the VCO can be used as the frequency reference for the AFT system provided that the PLL can be initially locked to the incoming IF signal. This combination of the tuner LO loop and the VCO loop forms a double loop PLL system. Analysis shows that the overall system stability can be assured by treating the VCO loop as a single stand alone PLL. This is valid if the VCO loop has low gain and high bandwidth which guarantees initial capture, while the tuner LO loop has high gain and low bandwidth which minimizes frequency and phase offsets.

The AFT system is designed to acquire the vision carrier, without false locking to the sound or adjacent sound carriers, with an initial tuner LO frequency error of ±2.0 MHz. This error is reduced to less than ±10 kHz upon establishing acquisition and after both the VCO loop and tuner AFT loop have reached their steady state condition. In contrast, the discriminator coil type of AFT has a highly asymmetric lock characteristics with a frequency error in the range of about –2.0 MHz to 1.0 MHz. This large frequency error is due to the effects of lower loop gain combined with the IF filter slope. Higher loop gain can be incorporated into the discriminator coil type of AFT but circuit problems due to large dc offsets, and IF stability due to coil radiation at the picture carrier frequency can be difficult to resolve. In order to achieve a high performance level, without encountering the ill effects associated with high gain discriminator circuits, a novel approach to establishing PLL lock up was developed.

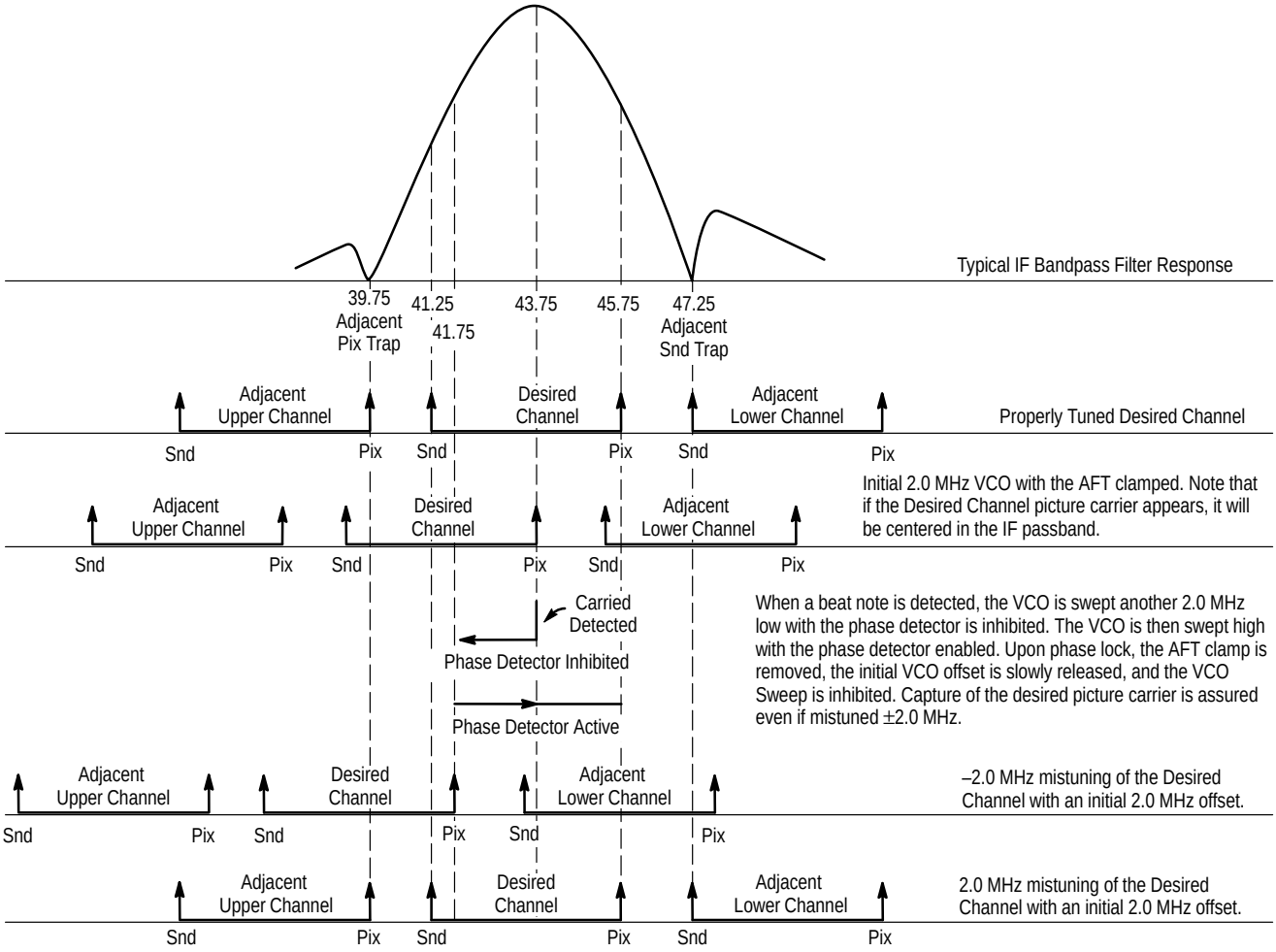
Figures 24 and 25 graphically illustrate the Acquisition Circuit operation. In the absence of an IF signal, the Acquisition Circuit examines the state of the Video (I) and Sound (Q) demodulators, detecting that the VCO is out of lock. On loss of lock, the AFT Output at Pin 11 (tuner LO drive) is clamped, and the Lock Detector output at Pin 18 is placed in a sink mode, causing its filter capacitor to discharge. As the capacitor voltage falls below 3.7 V, the application of a VCO offset starts and is completed at 3.0 V. The capacitor voltage will continue to fall stopping at 2.7 V until the Acquisition Circuit detects a signal. At this point both the tuner and IF are offset by the same amount from their nominal frequency of 45.75 MHz. Thus a picture carrier would now be converted to 43.75 MHz and the Main VCO Loop voltage at Pin 19 would be centered within its dynamic range at 3.2 V.

The AFT offset is controlled by the system designer to approximately –2.0 MHz. This is done so that if a nominal IF signal appeared, its picture carrier would be centered in the IF filter passband where there is minimum attenuation. Note that even if the tuner LO drifts by as much as ±2.0 MHz, the signal will still not be significantly attenuated.

On the arrival of a signal, beat notes are detected at the output of the demodulators, and the Lock Detector output is again placed in a sink mode to further discharge the filter capacitor. When the capacitor voltage falls below 1.3 V, the VCO Sweep is initiated at Pin 19. This causes the VCO to be swept an additional –2.0 MHz from its out of lock nominal centered IF frequency. During this negative sweep, the PLL Phase Detector is inhibited so that a phase lock cannot be obtained. When the capacitor voltage at Pin 19 falls to 2.0 V, the Phase Detector is made active and the VCO is swept in a positive direction from –2.0 MHz to 2.0 MHz of the out of lock centered IF frequency. The PLL will therefore lock to the first carrier it encounters. This in fact has to be a vision carrier since the sound carrier is more than 2.0 MHz below the nominal frequency, and the adjacent lower channel sound carrier is higher than the vision carrier. PLL lock can occur at any point during the positive going sweep of Pin 19 from 2.0 V to 4.2 V. On achieving lock, the Lock Detector output is released allowing the voltage across the filter capacitor to rise. When this voltage reaches 3.0 V, a gradual removal of the VCO offset starts. At 3.7 V removal is completed, the VCO Sweep circuit is inhibited, and the AFT clamp is removed. The phase detector remains permanently enabled. Upon removal of the AFT Clamp, the error voltage that appears at the AFT Amplifier output will drive the incoming signal towards the nominal IF frequency of 45.75 MHz. The Main VCO Loop will track the incoming IF signal while maintaining phase and frequency lock as the loops settle. This is attainable because the tuner AFT loop response is slow while the Main VCO loop is fast. For large frequency errors during this period, the slew rate of the tuner LO loop is automatically increased but not to the extent where it would cause a VCO tracking problem. This technique allows the acquisition time of the circuit to be reduced considerably while still using a larger than normal time constant in the tuner LO loop. In this way, any possibility of phase modulating the LO with video is removed.

The amount of AFT offset is controlled by the output swing of Pin 11, the voltage to frequency sensitivity of the tuner's AFT input, voltage gain or attenuation of any interface level shifting circuitry, and the alignment accuracy of the VCO coil. The amount of VCO offset and VCO sweep is controlled by the change in capacitance ratio of the internal tuning capacitance to that of the fixed external tank capacitors C19 and C20. To insure proper PLL lock, it is recommended that the VCO sweep is limited to less than 5.0 MHz and that C19 and C20 are not be less than 33 pF.

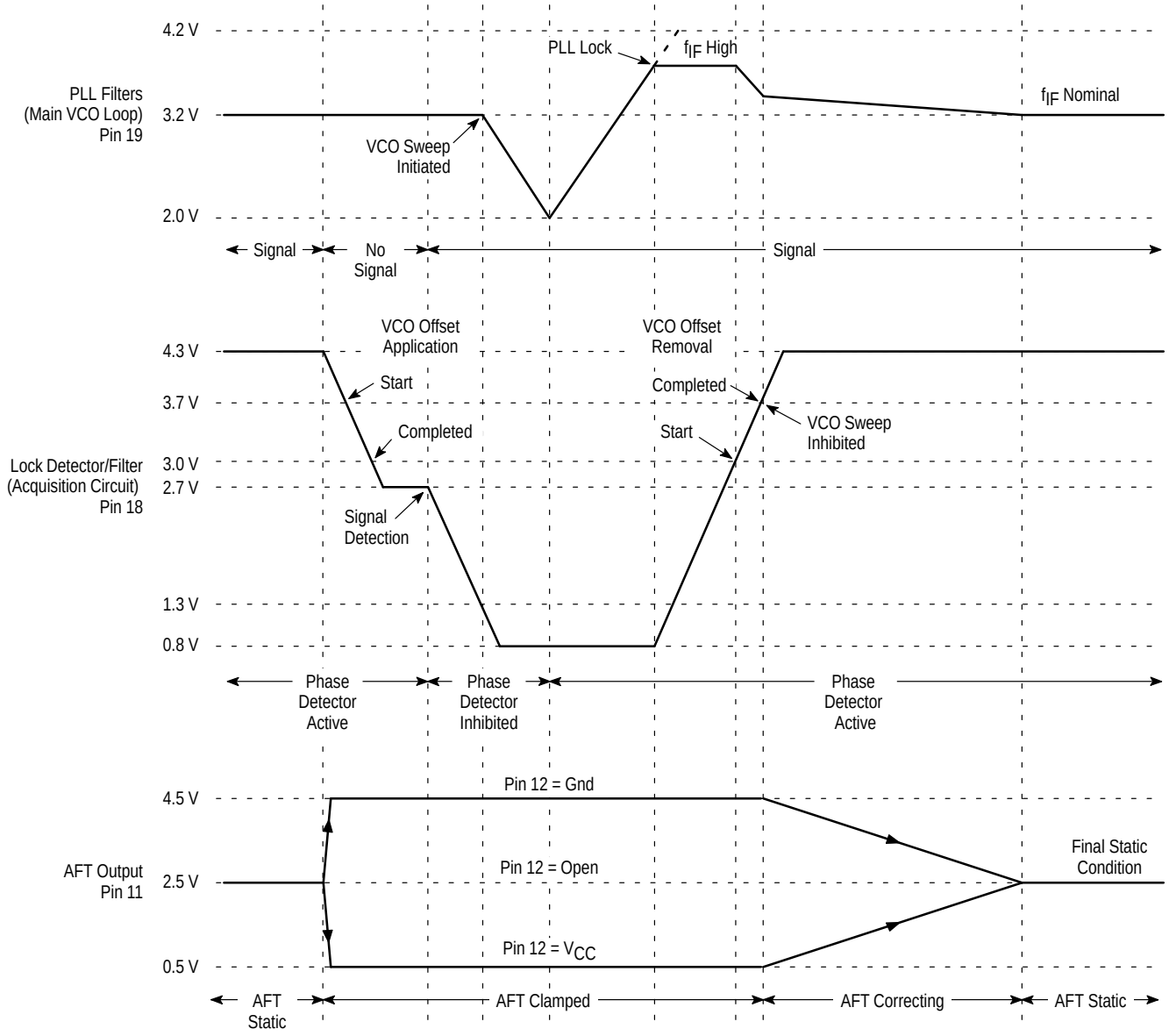
Figure 24. Acquisition Circuit Operation



It must be noted that in the operating description of this device, any reference made to the amount of VCO offset or sweep is the actual effect on the IF passband. The true VCO frequency change is only one half of that stated due to the Frequency Doubler circuit.

The AFT system is designed to control all types of varactor tuned local oscillators via the AFT Mode Switch input at Pin 12. This input is used to activate the output of the AFT control amplifier that appears at Pin 11, and to select the control voltage polarity versus IF frequency. With the AFT Mode Switch input connected to V_{CC}, Pin 11 is placed in a sourcing mode when the IF carrier frequency is below nominal. With the AFT Mode Switch input grounded, Pin 11 is placed in a sinking mode when the IF carrier frequency is below nominal. With the AFT Mode Switch input disconnected, Pin 11 is internally clamped to one half of V_{CC}, refer to Figures 6 and 25. Under this condition the TV set can be tuned manually and appear to have a conventional type of AFT with a smooth capture characteristic. Most other PLL AFT systems cannot be manually tuned in this manner as they tend to exhibit an undesirable abrupt capture characteristic. Digital phase–locked loop tuning systems can also be controlled with the addition of a varactor diode used to shift the PLL reference oscillator.

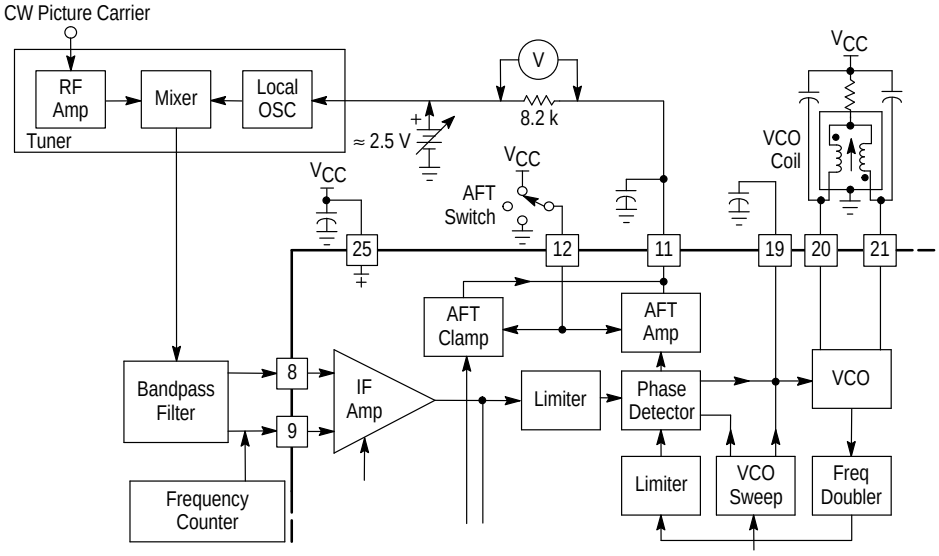
Figure 25. Acquisition Circuit Timing



In order to make the above drawing easier to comprehend, the vertical voltage axis was drawn to scale but the horizontal time axis was not. The typical slewing time for each output with the component values shown in the application circuit is as follows:

PLL Filter (Main VCO Loop) Pin 19 – 3.5 ms total sweep time when discharging down from 4.2 V to 2.0 V and charging back up to 4.2 V.
Lock Detector/Filter (Acquisition Circuit) Pin 18 – 4.0 ms when slewing up from 0.8 V to 4.3 V.
AFT Output Pin 11 – 12 ms when slewing from 4.5 V or 0.5 V to the final static condition of 2.5 V.

Figure 26. Alignment Configuration



Alignment

Tuning of a single coil is all that is required for complete alignment of the IF amplifier. This is most easily accomplished with the test set–up shown in Figure 26. The tuner is set to a given channel and a CW signal that is precisely set to the picture carrier frequency of that channel, is connected to the tuner RF input. The dc power supply is adjusted until the tuner output, measured by the frequency counter, is equal to the required IF picture carrier (45.75 MHz in the USA). The VCO coil is then adjusted so that the voltage across the 8.2 k resistor approaches zero. A voltage level of less than 5.0 mV should be easy to attain. The RF signal and the dc supply are removed and alignment is completed.

The tuning system should be designed so that the required varactor bias is approximately 2.5 V when phase–locked to the nominal IF signal. This centers the AFT amplifier's current source/sink output, Pin 11, yielding the maximum compliance voltage for optimum hold–in and pull–in characteristics. When interfacing Pin 11 with the tuning system's control bias, the output current must not exceed 4.0 mA. This current can be limited with the addition of a series output resistor if the AFT amplifier is required to drive a low resistance load.

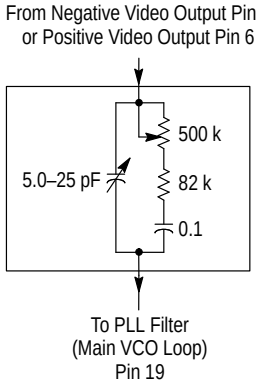
Differential Phase and Sound Buzz

Even with all the care taken in this design, some residual differential phase still remains. Although small, refer to Figure 8, it results in an output on the phase detector that modulates the VCO and the sound intercarrier. This in turn has the potential of degrading the stereo sound performance. In addition, there is a quadrature differential phase shift that is produced by the shape of the IF bandpass filter. Both produce currents in the output of the phase detector which in turn phase modulates the VCO. This phase modulation is imposed on the sound intercarrier resulting in a video related sound buzz. These currents can be canceled by injecting the correct amplitude and phase of demodulated video into the PLL filter. This can be accomplished with the addition of the differential phase correction circuit shown in Figure 27. The phase detector current that is due to the in–phase differential gain is canceled by the resistor current, and the quadrature component that is induced by the IF filter is canceled by the capacitor current. With proper adjustment, the differential phase distortion can be reduced to less than 0.5 degrees as well as eliminating any perceptible sound buzz. The source for the demodulated video to be injected into the PLL filter can be obtained from Pins 5 or 6. This must be determined experimentally for a given printed circuit board layout in order to obtain the best results. With the use of the correction circuit, this system achieves a similar level of performance to that of a parallel sound IF system.

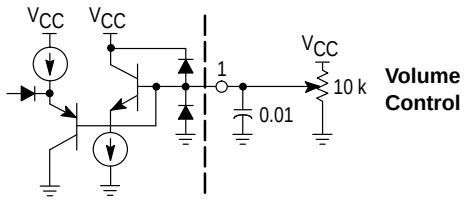
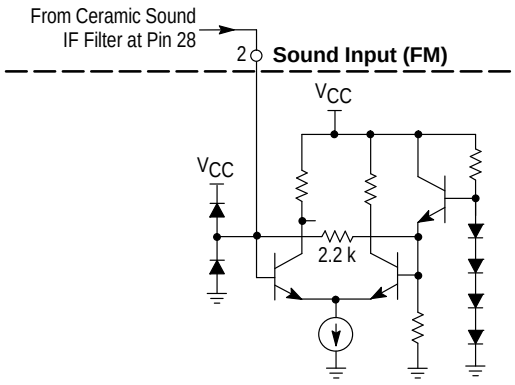
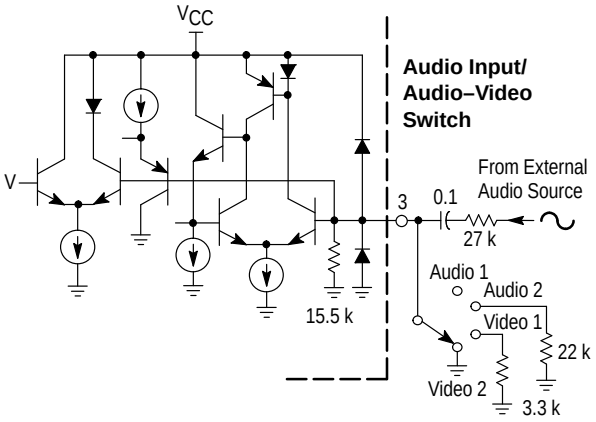
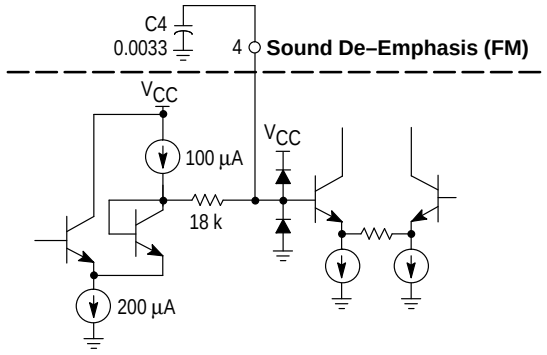
Electrostatic Protection

Most pins on the IC have electrostatic protection diodes to V_{CC} and ground. It is therefore imperative that no pin is taken below ground or above V_{CC} by more than one diode drop, approximately 0.6 V, without current limiting.

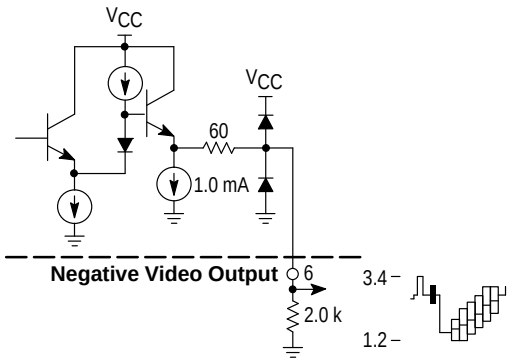
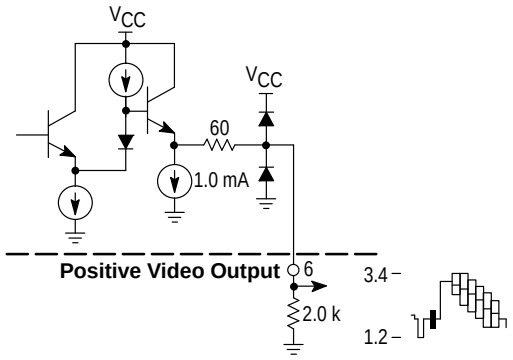
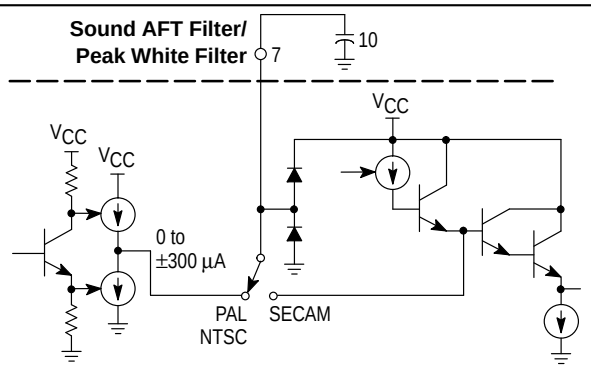
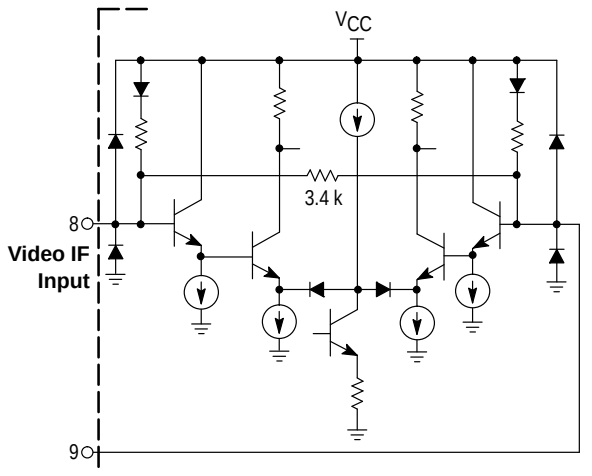
Figure 27. Differential Phase Correction Circuit



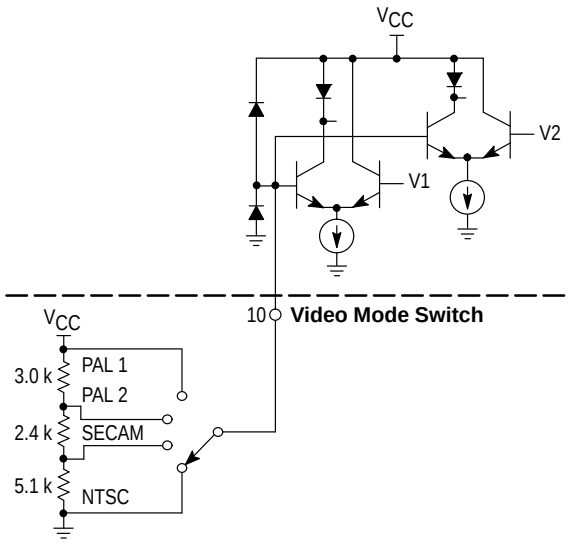
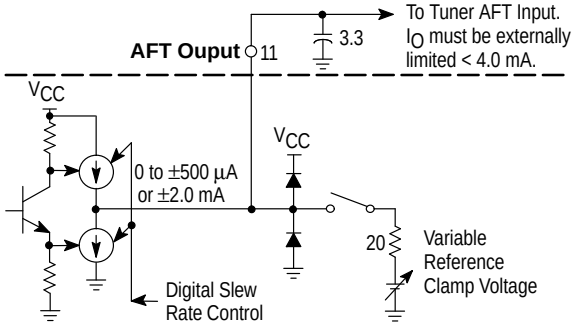
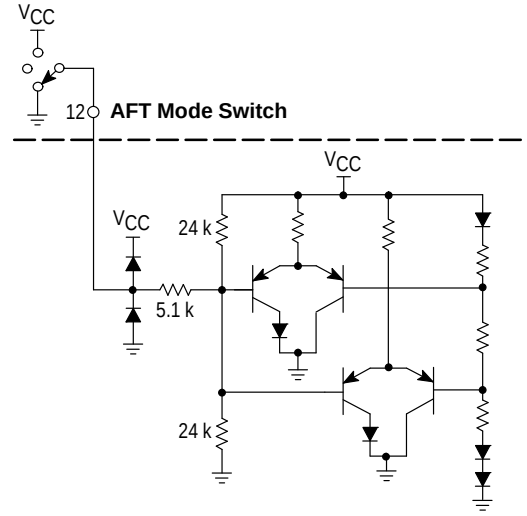
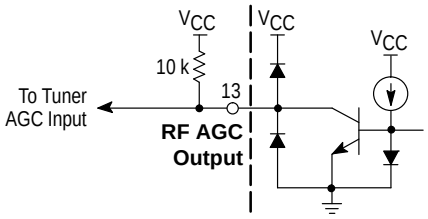
PIN FUNCTION DESCRIPTION

Pin No.	Equivalent Internal Circuit	Description
1		**DC Volume Control** A potentiometer of 20 kΩ or less, connected as shown, is used to adjust the audio output level at Pin 27. There is no audio signal present at this pin, allowing the use of unshielded wire between the IF board and the potentiometer. To prevent hum and noise pickup, a bypass capacitor connects from this pin to ground. Refer to Figure 17.
2		**Sound Input (FM)** This pin is the input of the FM IF. The intercarrier sound output at Pin 28 connects to this input through a ceramic bandpass filter. The FM detector is active in PAL 1, PAL 2, and NTSC modes. Refer to Table 2.
3		**Audio Input/Audio–Video Switch** This is a multifunction input that selects the audio source that appears at Pin 27, and the video polarity at Pins 5 and 6. Audio 1 is without a dc path from Pin 3 to ground. Internally demodulated audio (AM of FM) appears at Pins 24 and 27, negative video at Pin 5, and positive video at Pin 6. The audio source at Pin 3 is internally disconnected. Audio 2 is with the 22 kΩ resistor connected. Internally demodulated audio (AM or FM) appears at Pin 24, negative video at Pin 5, positive video at Pin 6, and the audio source at Pin 3 appears at Pin 27. Video 1 is with the 3.3 kΩ resistor connected. Internally demodulated audio (AM or FM) appears at Pins 24 and 27, negative video at Pin 5, and positive video at Pin 6. Video 2 is with Pin 3 grounded. Internally demodulated audio (AM of FM) appears at Pins 24 and 27, positive video at Pin 5, and negative video at Pin 6. Refer to Table 1.
4		**Sound De–Emphasis (FM)** A capacitor is connected from this pin to ground. It is used in conjunction with internal 18 kΩ resistor to set the FM sound de–emphasis time constant. The typical de–emphasis time constant required for a flat audio response is 75 µs in the United States and 50 µs in Europe. The FM sound detector frequency response for different de–emphasis capacitor values is shown in Figure 12.

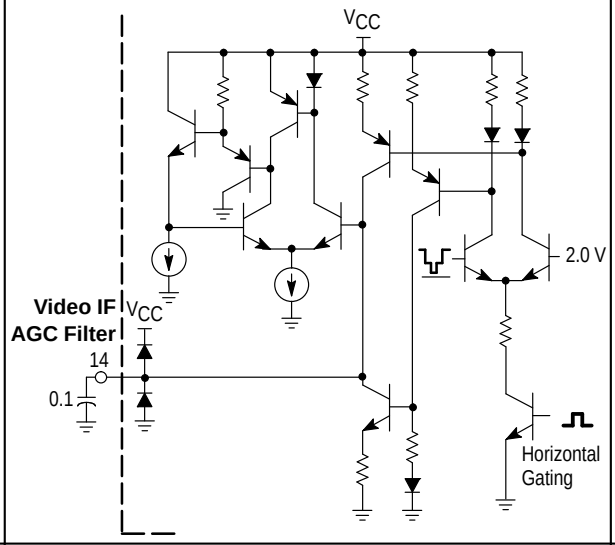
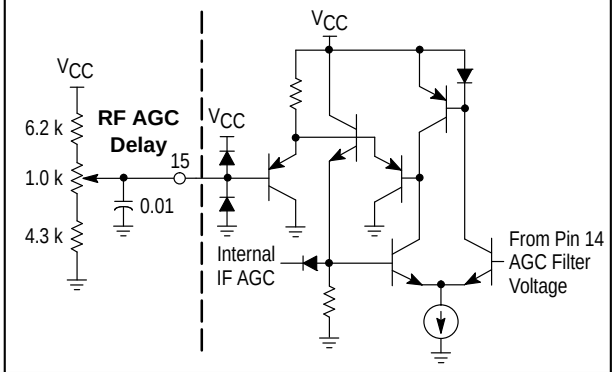
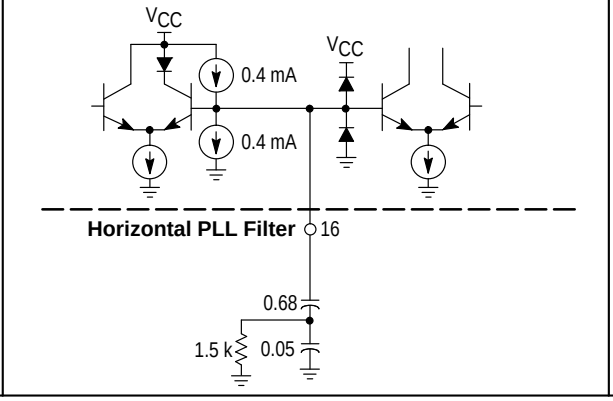
PIN FUNCTION DESCRIPTION (continued)

Pin No.	Equivalent Internal Circuit	Description
5		**Negative Video Output** Negative going video appears at this output and it is intended to drive a sync separator. Positive going video will appear at this output when Pin 3 is grounded. This feature provides a simple means for descrambling the video signal in systems that use alternate line video inversion. Refer to the description of Pin 3. The video output is designed to drive a resistive load that is in the range of 2.0 kΩ. Lower resistance values will tend to increase output distortion.
6		**Positive Video Output** Positive going video appears at this output and is intended to drive the luma and chroma channels. Negative going video will appear at this output when Pin 3 is grounded. This feature provides a simple means for descrambling the video signal in systems that use alternate line video inversion. Refer to the description of Pin 3. The positive going video signal always contains white spot inversion whether it appears at output Pins 5 or 6. The video output is designed to drive a resistive load that is in the range of 2.0 kΩ. Lower resistance values could increase output distortion.
7		**Sound AFT Filter/Peak White Filter** A capacitor connected from this pin to ground is used to adjust the sound AFT time constant in PAL and NTSC modes, and video peak white AGC time constant in SECAM mode. The sound AFT filter voltage controls the internal tuning capacitance that is placed across the sound quadrature coil at Pin 26. Refer to Figure 9.
8, 9		**Video IF Input** These pins are the inputs to the video IF amplifier. The amplifier consists of four ac coupled stages with an input sensitivity of 40 µV for a 2.2 Vpp video output swing. This sensitivity eliminates the need for a preamplifier when used with suitable surface acoustic waves or passive block filters. The IF block filter must be located close to the IC package inputs to prevent unwanted pickup and possible instability problems. The input lead lengths must be kept short with a symmetrical printed circuit board layout.

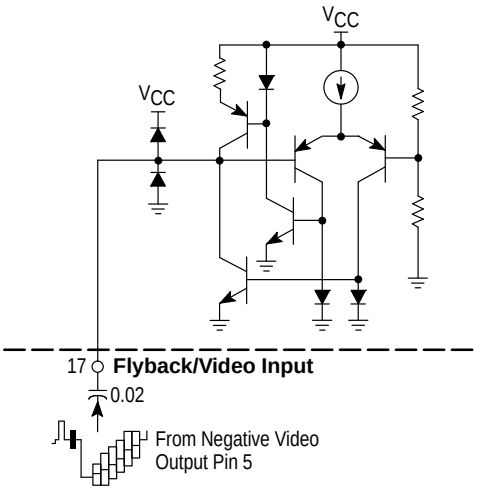
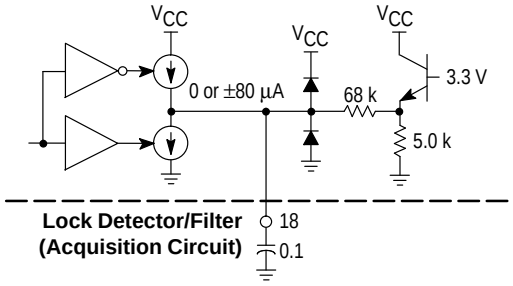
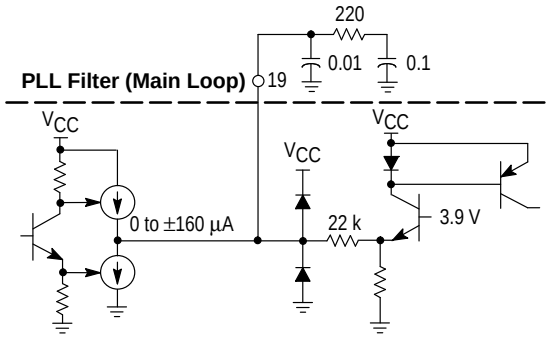
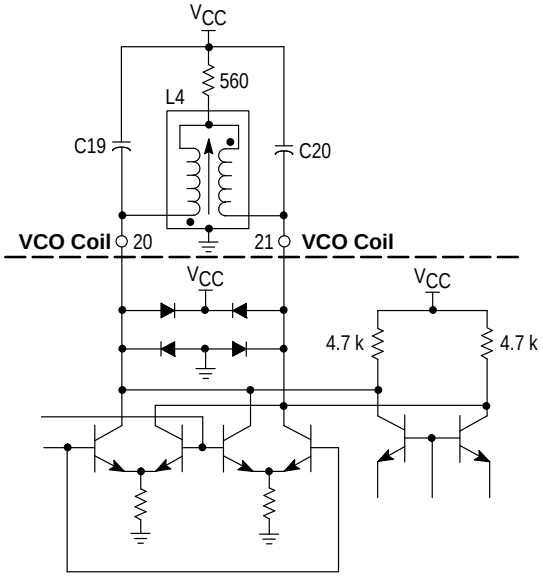
PIN FUNCTION DESCRIPTION (continued)

Pin No.	Equivalent Internal Circuit	Description
10		**Video Mode Switch** A dc voltage at this input selects the proper video AGC and sound demodulation technique for PAL, SECAM, and NTSC. With PAL 1 selected, AGC is keyed on the sync pulse by the horizontal PLL which is locked to the flyback or video sync pulse present at Pin 17. The FM sound IF and detector is active. The PAL 2 selection is identical to PAL 1 with the addition of sound muting when the acquisition circuit is unlocked or vertical sync is absent. With SECAM selected, the video level is established by both, a long time constant peak white detector, and a back porch keyed AGC that corrects for transmitted black level errors while maintaining fast AGC response. The AM sound detector is active. With NTSC selected, AGC and sound muting is the same as in PAL 1 mode. The FM and AM detectors are both active with the FM output at Pin 27 and the AM output at Pin 24. Refer to Table 2.
11		**AFT Output** With detent type tuners, the automatic fine tuning output can be used to directly control the tuner local oscillator varactor. The varactor control input must be high impedance in order to maintain high AFT loop gain with acceptable dynamic response. This output has a linear sink and source current range of 0 to 500 µA, and is digitally switched to ±2.0 mA for large frequency errors. The capacitor from Pin 11 to ground limits the bandwidth of the tuner local oscillator loop. Digital phase–locked loop tuning systems can also be controlled with the addition of a varactor diode used to shift the PLL reference oscillator. Refer to Figures 6, 24, and 25.
12		**AFT Mode Switch** This input is used to activate the output of the AFT control amplifier that appears at Pin 11, and to select the control voltage polarity versus IF frequency. This feature allows the AFT output to work with all types of varactor tuned local oscillators. With the AFT Mode Switch input connected to V_{CC}, Pin 11 is placed in a sourcing mode when the IF carrier frequency is below nominal. With the AFT Mode Switch input grounded, Pin 11 is placed in a sinking mode when the IF carrier frequency is below nominal. With the AFT Mode Switch input disconnected, Pin 11 is internally clamped to one half of V_{CC}, refer to Figures 6 and 25.
13		**RF AGC Output** This output is designed to control a reverse AGC tuner. As the antenna signal level increases, the voltage at Pin 13 decreases, causing a gain reduction in the tuner RF stage. An external pull–up resistor must be added if one is not provided in the tuner. Pin 13 is guaranteed to sink a minimum of 1.0 mA. Note that when operating with a tuner that requires in excess of 5.6 V, current will flow into Pin 13 due to conduction of the upper internal clamp diode.

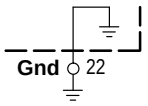
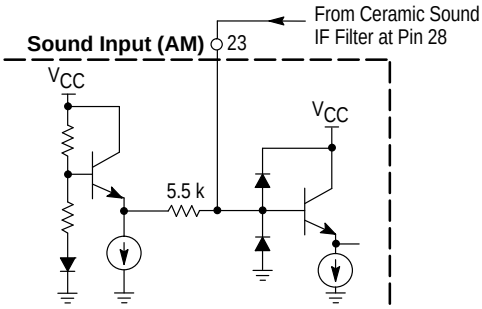
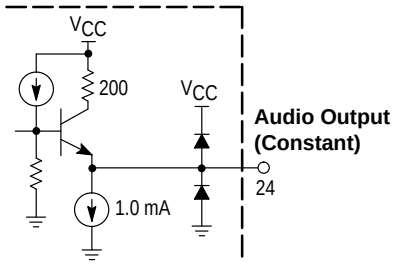
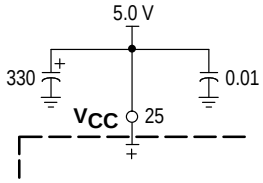
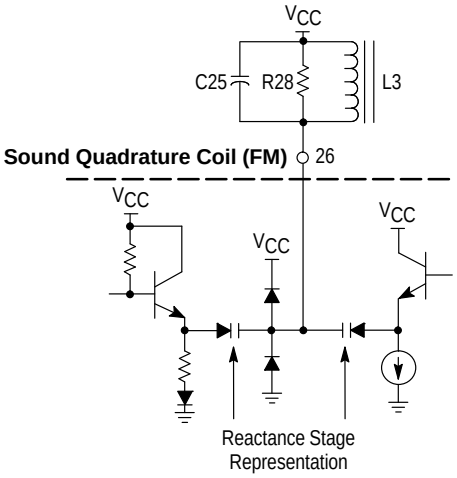
PIN FUNCTION DESCRIPTION (continued)

Pin No.	Equivalent Internal Circuit	Description
14		**Video IF AGC Filter** A capacitor connects from this pin to ground to control the video IF AGC rate of change with respect to a change in input signal level. An increase in input signal level causes an increase in the voltage at Pin 14 which controls the internal AGC action. Pin 14 has an unsymmetrical source and sink current of 150 μA and 8.0 μA respectively. The AGC filter voltage versus IF differential input signal level is shown in Figure 1.
15		**RF AGC Delay** A voltage applied to this input sets the video IF signal level threshold before gain reduction of the tuner begins. The threshold setting is tuner dependent but is usually in the range of 1.0 mV to 2.0 mV of signal at the antenna. Too low of a setting will cause premature tuner gain reduction and a poor picture and sound signal to noise ratio, while too high of a setting will cause tuner overload and picture distortion. The IF differential input signal level versus RF AGC takeover threshold is shown in Figure 2.
16		**Horizontal PLL Filter** This is a dual function pin. With the network shown, the horizontal phase–locked loop oscillator provides a keying pulse to properly gate the AGC when in PAL, SECAM, and NTSC modes. With Pin 16 grounded, both the AM and FM sound IF and detectors are inhibited. By placing Pin 3 in the Audio 2 mode, the variable audio output at Pin 27 is active and can be used to control the level of the externally processed digital sound. Refer to the description of Pin 3.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Equivalent Internal Circuit	Description
17		**Flyback/Video Input** This input connects to a positive going sync source to generate an internal AGC keying pulse. An internal sync separator is provided for use in stand alone applications where a horizontal scan signal is unavailable. The sync separator allows direct use of the negative video output at Pin 5 to set the internal keying pulse. If horizontal scan circuitry is available, a positive going flyback pulse can be used instead to set the keying pulse.
18		**Lock Detector/Filter (Acquisition Circuit)** A filter capacitor for the acquisition circuit lock detector connects from this pin to ground. The capacitor voltage will vary upon signal presence and lock condition. Typical voltages are 2.7 V with the circuit unlocked and without any signal, 0.8 V to 4.3 V during signal acquisition, and 4.3 V when locked. Refer to the Acquisition Circuit Timing in Figure 25.
19		**PLL Filter (Main VCO Loop)** A filter capacitor for the main phase–locked loop circuit connects from this pin to ground. The typical capacitor voltage is 3.2 V when locked and the circuit has reached the final static condition. Refer to Figure 5 for the PLL filter voltage versus carrier frequency change, and to Figure 25 for the acquisition circuit timing.
20, 21		**VCO Coil** These are the voltage controlled oscillator pins. Symmetrical tuning about the VCO frequency is provided by a bifiliar wound coil that resonates at one half of the desired IF frequency. The coil must be placed close to the IC pins to prevent any unwanted pickup or radiation. The printed circuit board layout must have short symmetrical traces with adequate grounding for the can shield. Capacitors C19 and C20 should not be less than 33 pF. Suggested component values for the major IF frequencies are listed in Table 3.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Equivalent Internal Circuit	Description
22		**Gnd** This pin is the internal circuit ground. Care must be taken with the printed circuit board layout to provide a continuous sea of copper around the IC.
23		**Sound Input (AM)** This pin is the input of the AM IF. The intercarrier sound output at Pin 28 connects to this input through a ceramic bandpass filter. The AM detector is active in SECAM and NTSC modes. Refer to Table 2.
24		**Audio Output (Constant)** This is the constant audio output. The audio source is controlled by the mode selection of Pin 3. Refer to the description of Pin 3, and to Tables 1 and 2.
25		**V_{CC}** This pin is the positive supply of the video/sound IF IC. The IC is functional over a minimum range of 4.75 V to 5.5 V and requires 100 mA. Operation from higher input voltages is possible with a preregulator. For optimum performance, it is recommended that circuit board layout contains dual power supply bypass capacitors with short leads connected directly to the V_{CC} pin and ground.
26		**Sound Quadrature Coil (FM)** The sound quadrature tank components connect from this pin to V_{CC}. The internal circuitry is designed to eliminate the time consuming alignment procedure by self tuning to the sound intercarrier frequency. This allows the use of economical fixed value components for a specific frequency or for a range of frequencies. The internal tuning capacitance that is placed across the tank ranges from 0.25 pF to 19 pF. Refer to Figures 9, 10, and Table 3 to select the proper component values for C25, R28, and L3.

PIN FUNCTION DESCRIPTION (continued)

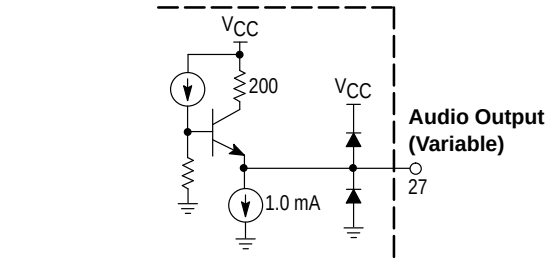
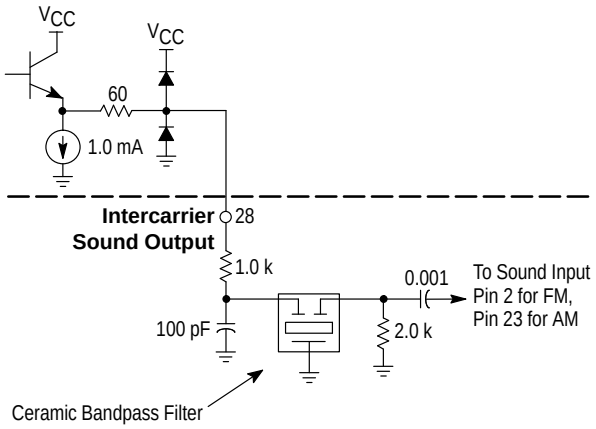
Pin No.	Equivalent Internal Circuit	Description
27		**Audio Output (Variable)** This is the variable audio output. The audio source is controlled by the mode selection of Pin 3, and audio level is controlled by a potentiometer connected to Pin 1. Refer to the description of Pin 3, Table 1, Table 2, and Figure 17.
28		**Intercarrier Sound Output** This pin is the sound intercarrier output and is normally connected to either the AM or FM sound IF input through a bandpass filter. Because quadrature demodulation is used, the video level at this output is greatly suppressed.

Figure 28. Printed Circuit Board Evaluation Circuit

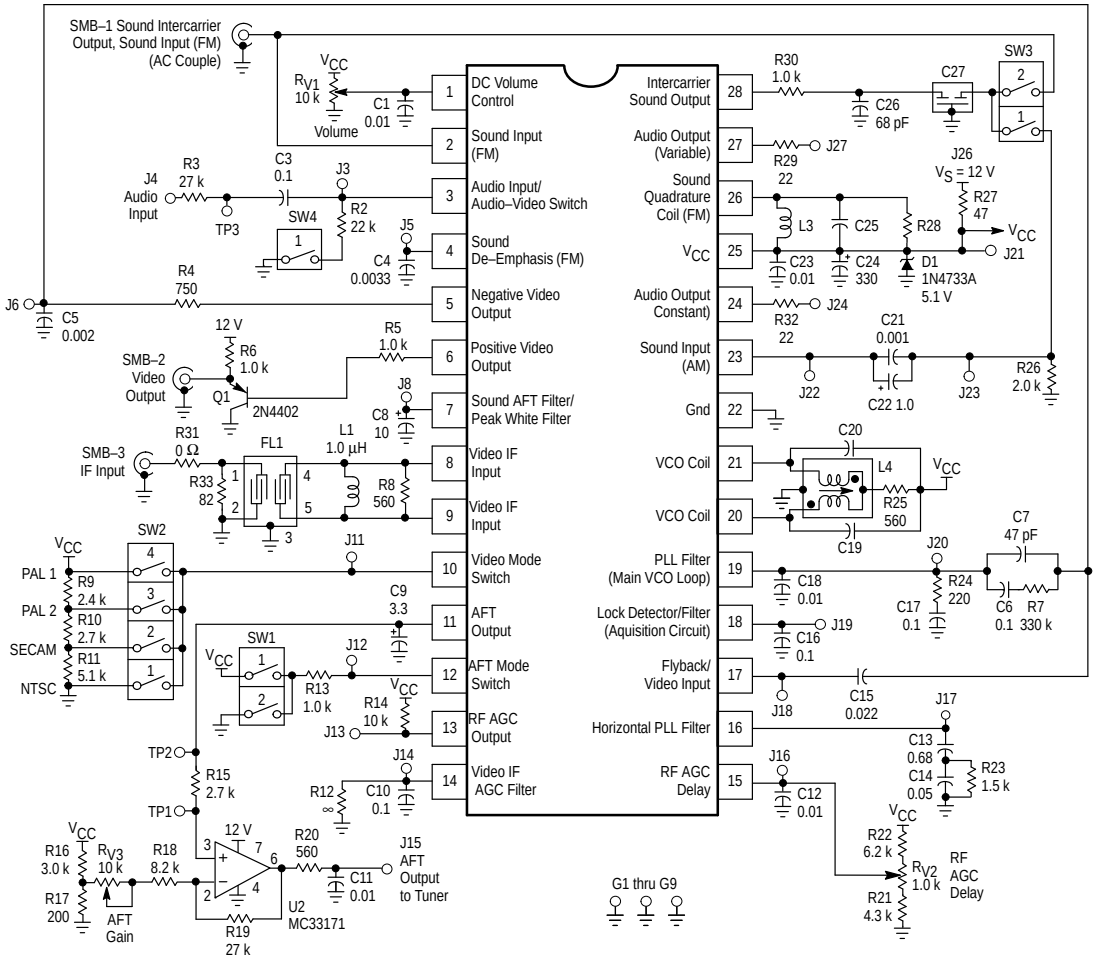
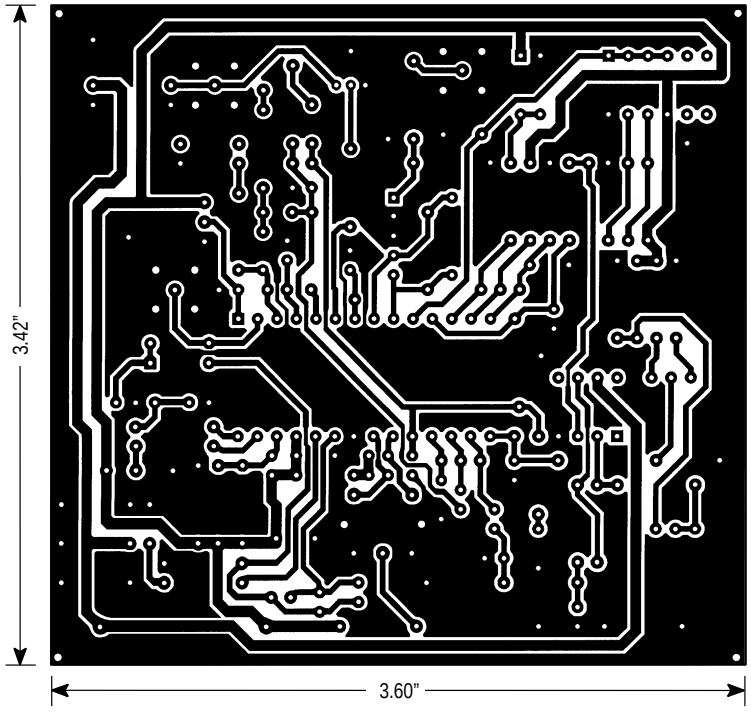


Table 3. Suggested Components Values for Figure 28

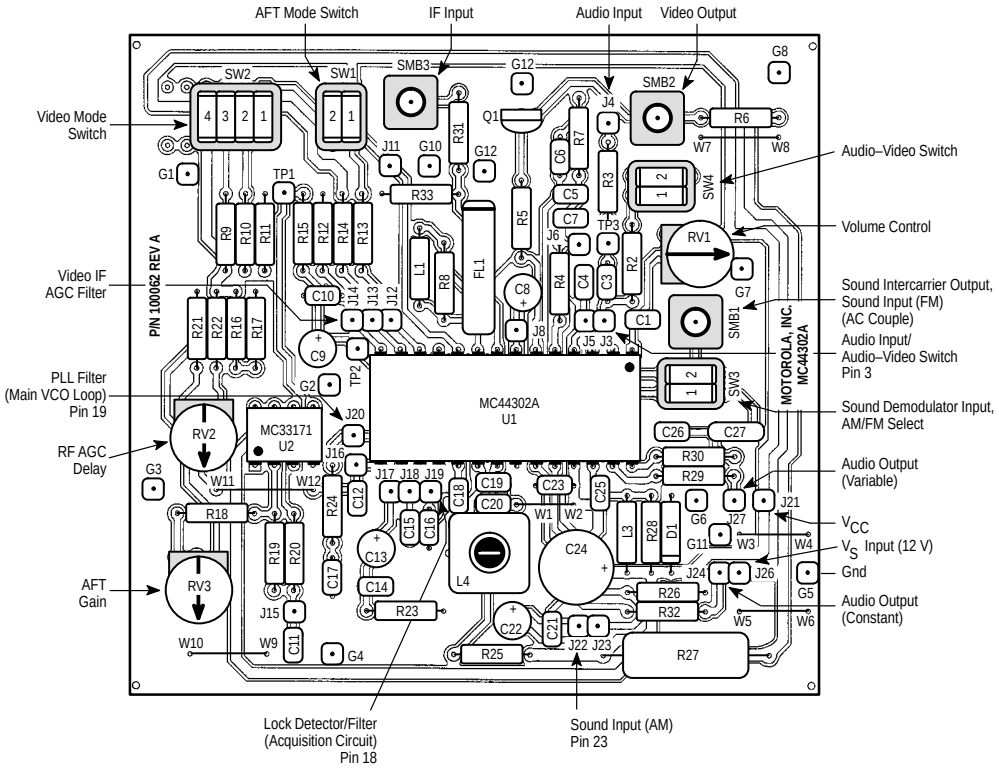
Video IF						
Carrier Frequency (MHz)		SAW Filter FL1	VCO Components			
			Coil L4			Capacitors C19, C20
Picture	Sound	Siemens #	Coilcraft #	Toko #	(μH)	(pF)
38.90	32.40	B39389–K2951–M100	R4715–A	–	1.9 to 3.3	39
39.50	33.50	B39395–J1953–M100	R4715–A	–	1.9 to 3.3	39
38.90	33.40	B39389–K2951–M100	R4715–A	–	1.9 to 3.3	39
45.75	41.25	B39458–M1963–M100	M1300–A	TKANSAS–T1390HK	1.4 to 2.6	33
58.75	54.25	B39588–N1951–M100	R4714–A	–	0.8 to 1.5	47

Sound IF					
Intercarrier Frequency	Ceramic Filter C27	Quadrature Components			
		Coil L3		Capacitor C25	Resistor R28
(MHz)	Murata Erie #	Coilcraft #	(μH)	(pF)	(kΩ)
6.5	SFE6.5MBF	90–23	6.8	75	10
6.0	SFE6.0MBF	90–25	10	56	10
5.5	SFE5.5MBF	90–25	10	68	10
4.5	SFE4.5MBF	90–27	15	62	10
5.5 to 6.5	–	90–29	22	15	10

Figure 29. Evaluation Circuit Board and Component Layout



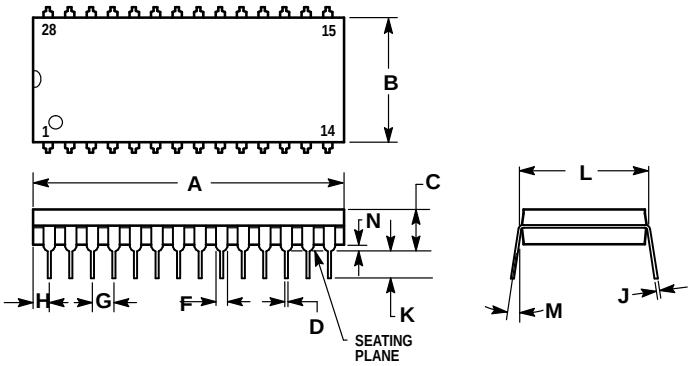
(Bottom View)



(Top View)

OUTLINE DIMENSIONS

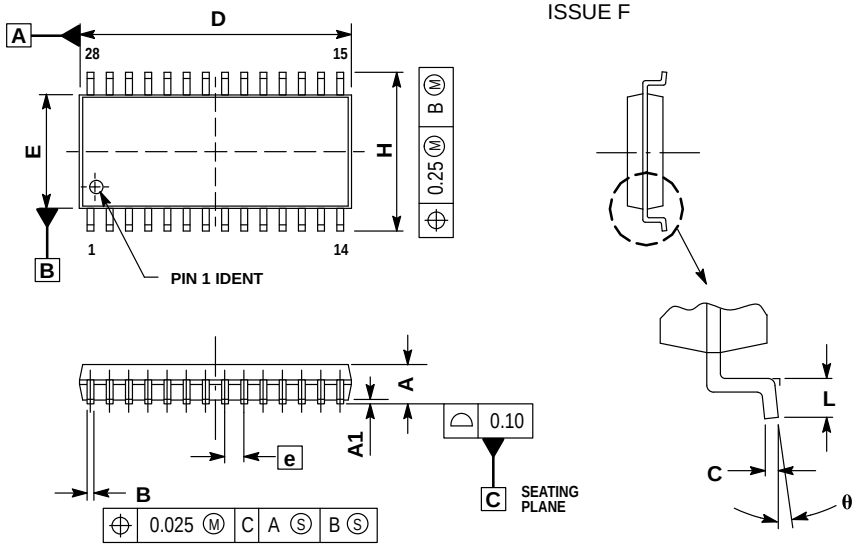
P SUFFIX
PLASTIC PACKAGE
CASE 710–02
ISSUE B



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15°	0 °	15°
N	0.51	1.02	0.020	0.040

DW SUFFIX
PLASTIC PACKAGE
CASE 751F–05
(SO–28L)
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0 °	8 °

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