# MC33762

# Dual Ultra Low–Noise Low Dropout Voltage Regulator with 1V ON/OFF Control

The MC33762 is a dual Low DropOut (LDO) regulator featuring excellent noise performances. Thanks to its innovative concept, the circuit reaches an incredible 40µVRMS noise level ***without*** an external bypass capacitor. Housed in a small µ8 package, it represents the ideal designer's choice when space and noise are at premium.

The absence of external bandgap capacitor unleashes the response time to a wake–up signal and makes it stay within 40µs, pushing the MC33762 as a natural candidate in portable applications.

The MC33762 also hosts a novel architecture which prevents excessive undershoots when the regulator is the seat of fast transient bursts, as in any bursting systems.

Finally, with a static line regulation better than –75dB, it naturally shields the downstream electronics against choppy lines.

### Features

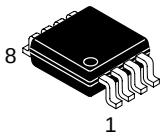
- Nominal output current of 80mA with a 100mA peak capability
- Ultra low–noise: 150nV/√Hz @ 100Hz, 40µVRMS 100Hz – 100kHz typical, Iout = 60mA, Co=1µF
- Fast response time from OFF to ON: 40µs typical
- Ready for 1V platforms: ON with a 900mVhigh level
- Typical dropout of 90mV @ 30mA, 160mV @ 80mA
- Ripple rejection: 70dB @ 1kHz
- 1.5% output precision @ 25°C
- Thermal shutdown
- Vout available from 2.5V to 5.0V

### Applications

- Noise sensitive circuits: VCOs RF stages etc.
- Bursting systems (TDMA phones)
- All battery operated devices

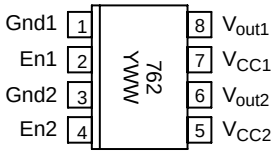
ON Semiconductor

http://onsemi.com




**Micro8**
**DM SUFFIX**
**CASE 846A**

### PIN CONFIGURATION AND MARKING DIAGRAM



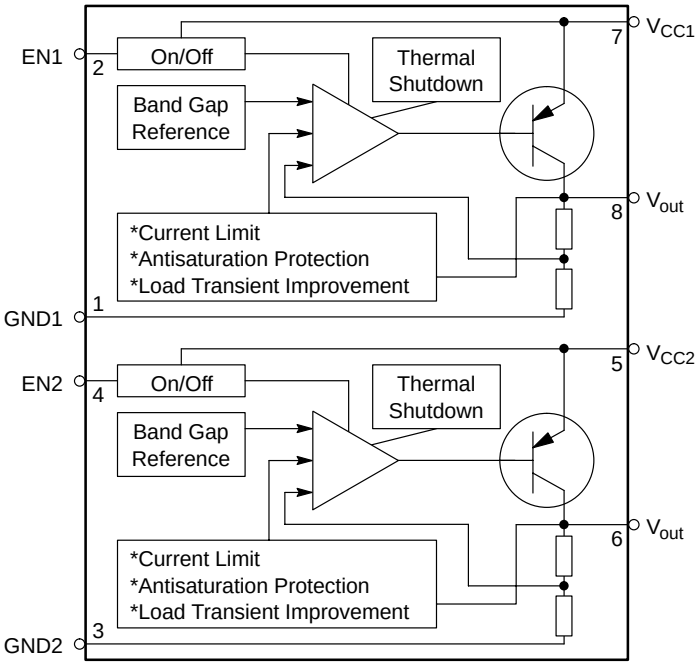

(Top View)

YY, Y = Year
WW, W = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

### Simplified Block Diagram




### PIN FUNCTION DESCRIPTIONS

| Pin # | Pin Name | Function | Description |
|---|---|---|---|
| 1 | Gnd1 | Ground of the 1st LDO | |
| 2 | En1 | Enables the 1st LDO | A 900mV level on this pin is sufficient to start this LDO. A 150mV shuts it down. |
| 3 | Gnd2 | Ground of the 2nd LDO | |
| 4 | En2 | Enables the 2nd LDO | A 900mV level on this pin is sufficient to start this LDO. A 150mV shuts it down. |
| 5 | $V_{cc2}$ | 2nd LDO $V_{cc}$ pin | This pin brings the power to the 1st LDO and requires adequate decoupling. |
| 6 | $V_{out2}$ | Shuts or wakes–up the IC | This pin requires a 1µF output capacitor to be stable. |
| 7 | $V_{cc1}$ | 1st LDO $V_{cc}$ pin | This pin brings the power to the 1st LDO and requires adequate decoupling. |
| 8 | $V_{out1}$ | Delivers the output voltage | This pin requires a 1µF output capacitor to be stable. |

### MAXIMUM RATINGS

| Rating | Pin # | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Power Supply Voltage | 1 | $V_{in}$ | — | 12 | V |
| ESD Capability, HBM Model | All Pins | | | 1 | kV |
| ESD Capability, Machine Model | All Pins | | | 200 | V |
| Maximum Power Dissipation<br>NW Suffix, Plastic Package<br>Thermal Resistance Junction–to–Air | | $P_D$<br><br>$R_{\theta J-A}$ | | Internally Limited<br><br>240 | W<br><br>°C/W |
| Operating Ambient Temperature<br>Maximum Junction Temperature (Note 1.)<br>Maximum Operating Junction Temperature (Note 2.) | | $T_A$<br>$T_{Jmax}$<br>$T_J$ | | –40 to +85<br>150<br>125 | °C<br>°C<br>°C |
| Storage Temperature Range | | $T_{stg}$ | | –60 to +150 | °C |

1. Internally limited by shutdown.
2. Specifications are guaranteed below this value.

## ELECTRICAL CHARACTERISTICS

(For Typical Values $T_A$ = 25°C, for Min/Max values $T_A$ = –40°C to +85°C, Max $T_J$ = 125°C unless otherwise noted)

| Characteristics | Pin # | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Logic Control Specifications** | | | | | | |
| Input Voltage Range | 2–4 | $V_{ON/\overline{OFF}}$ | 0 | | $V_{in}$ | V |
| ON/$\overline{OFF}$ Input Resistance (all versions) | 2–4 | $R_{ON/\overline{OFF}}$ | | 250 | | kΩ |
| ON/OFF Control Voltages (Note 3.)<br>Logic Zero, OFF State, $I_O$ = 50 mA<br>Logic One, ON State, $I_O$ = 50 mA | 2–4 | $V_{ON/\overline{OFF}}$ | <br><br>900 | | <br>150 | mV |
| **Currents Parameters** | | | | | | |
| Current Consumption in OFF State (all versions)<br>OFF Mode Current: $V_{in} = V_{out}$ + 1 V, $I_O$ = 0, $V_{OFF}$ = 150 mV | | $IQ_{OFF}$ | | 0.1 | 2 | μA |
| Current Consumption in ON State (all versions)<br>ON Mode Current: $V_{in} = V_{out}$ + 1 V, $I_O$ = 0, $V_{ON}$ = 3.5 V | | $IQ_{ON}$ | | 180 | | μA |
| Current Consumption in ON State (all versions), ON Mode Saturation Current: $V_{in} = V_{out}$ – 0.5 V, No Output Load | | $IQ_{SAT}$ | | 800 | | μA |
| Current Limit $V_{in} = Vout_{nom}$ + 1 V,<br>Output is brought to $Vout_{nom}$ – 0.3 V (all versions) | | $I_{MAX}$ | 100 | 180 | | mA |
| **Output Voltages** | | | | | | |
| $V_{out}$ + 1 V < $V_{in}$ < 6 V, $T_A$ = 25°C, 1 mA < $I_{out}$ < 80 mA<br>2.5 V | 5–7 | $V_{out}$ | 2.462 | 2.5 | 2.537 | V |
| 2.8 V | 5–7 | $V_{out}$ | 2.758 | 2.8 | 2.842 | V |
| 3.0 V | 5–7 | $V_{out}$ | 2.955 | 3.0 | 3.045 | V |
| 3.3 V | 5–7 | $V_{out}$ | 3.250 | 3.3 | 3.349 | V |
| 3.6 V | 5–7 | $V_{out}$ | 3.546 | 3.6 | 3.654 | V |
| Other Voltages up to 5V Available in 50mV Increments Steps | 5–7 | $V_{out}$ | –1.5 | X | +1.5 | % |
| $V_{out}$ + 1V < $V_{in}$ < 6V, $T_A$ = –40°C to +85°C, 1mA < $I_{out}$ < 80mA<br>2.5 V | 5–7 | $V_{out}$ | 2.425 | 2.5 | 2.575 | V |
| 2.8 V | 5–7 | $V_{out}$ | 2.716 | 2.8 | 2.884 | V |
| 3.0 V | 5–7 | $V_{out}$ | 2.91 | 3.0 | 3.090 | V |
| 3.3 V | 5–7 | $V_{out}$ | 3.201 | 3.3 | 3.399 | V |
| 3.6 V | 5–7 | $V_{out}$ | 3.492 | 3.6 | 3.708 | V |
| Other Voltages up to 5V Available in 50mV Increments Steps | 5–7 | $V_{out}$ | –3 | X | +3 | % |
| **Line and Load Regulation, Dropout Voltages** | | | | | | |
| Line Regulation (all versions)<br>$V_{out}$ + 1 V < $V_{in}$ < 12 V, $I_{out}$ = 80 mA | 5–7 | $Reg_{line}$ | | | 20 | mV |
| Load Regulation (all versions)<br>$V_{in} = V_{out}$ + 1 V, $C_{out}$ = 1 μF, $I_{out}$ = 1 to 80 mA | 5–7 | $Reg_{load}$ | | | 40 | mV |
| Dropout Voltage (all versions) (Note 3.)<br>$I_{out}$ = 30 mA<br>$I_{out}$ = 60 mA<br>$I_{out}$ = 80 mA | <br>5–7<br>5–7<br>5–7 | <br>$V_{in}$–$V_{out}$<br>$V_{in}$–$V_{out}$<br>$V_{in}$–$V_{out}$ | | <br>90<br>140<br>160 | <br>150<br>200<br>250 | mV |

3. Voltage Slope should be Greater than 2 mV/μs

**ELECTRICAL CHARACTERISTICS (continued)**

(For Typical Values $T_A$ = 25°C, for Min/Max values $T_A$ = –40°C to +85°C, Max $T_J$ = 125°C unless otherwise noted)

| Characteristics | Pin # | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Dynamic Parameters** | | | | | | |
| Ripple Rejection (all versions)<br>$V_{in}$ = $V_{out}$ + 1 V + 1 kHz 100 mVpp Sinusoidal Signal | 5–7 | Ripple | | –70 | | dB |
| Output Noise Density @ 1 kHz | 5–7 | | | 150 | | nV/√Hz |
| RMS Output Noise Voltage (all versions)<br>$C_{out}$ = 1 μF, $I_{out}$ = 50 mA, F = 100 Hz to 1 MHz | 5–7 | Noise | | 35 | | μV |
| Output Rise Time (all versions) $C_{out}$ = 1 μF, $I_{out}$ = 50 mA,<br>10% of Rising ON Signal to 90% of Nominal $V_{out}$ | 5–7 | $t_{rise}$ | | 40 | | μs |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown (all versions) | | | | | 125 | °C |

## DEFINITIONS

### Load Regulation

The change in output voltage for a change in output current at a constant chip temperature.

### Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100mV below its nominal value (which is measured at 1V differential value). The dropout level is affected by the chip temperature, load current and minimum input supply requirements.

### Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output current are kept constant during the measurement. Results are expressed in μVRMS.

### Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specs.

### Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

### Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected. One usually distinguishes *static line regulation* or *DC line regulation* (a DC step in the input voltage generates a corresponding step in the output voltage) from *ripple rejection* or *audio susceptibility* where the input is combined with a frequency generator to sweep from a few hertz up to a defined boundary while the output amplitude is monitored.

### Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 125°C, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

### Maximum Package Power Dissipation

The maximum power package power dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient temperature, it is possible to calculate the maximum power dissipation and thus the maximum available output current.

## Characterization Curves

Curves are Common to Both Regulators

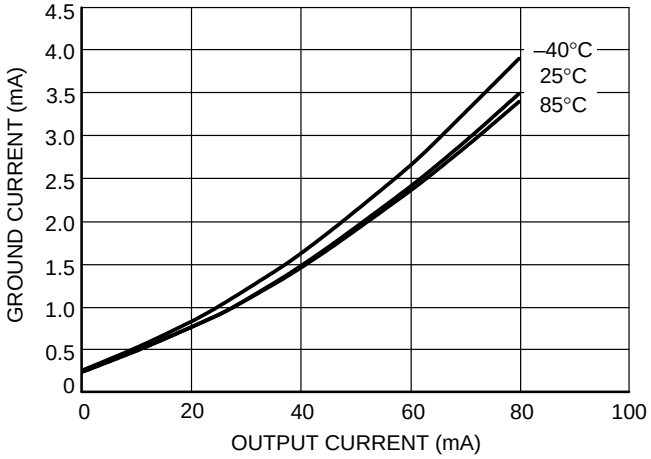



**Figure 1. Ground Current versus Output Current**

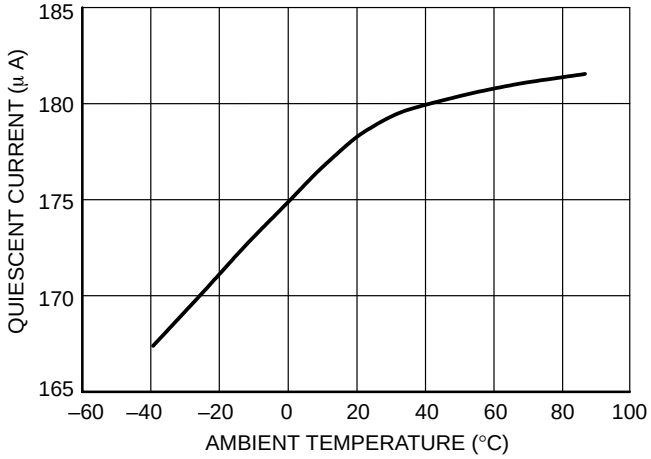



**Figure 2. Quiescent Current versus Temperature**

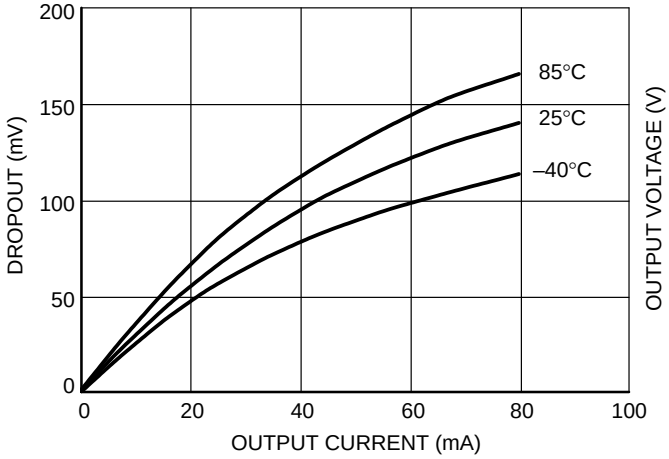



**Figure 3. Dropout versus Output Current**

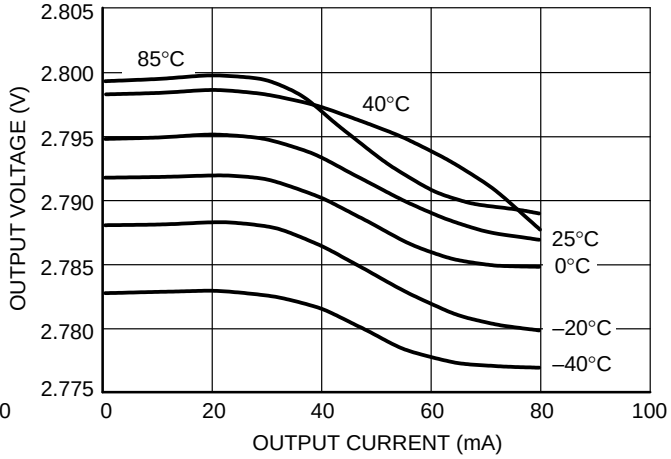



**Figure 4. Output Voltage versus Output Current**

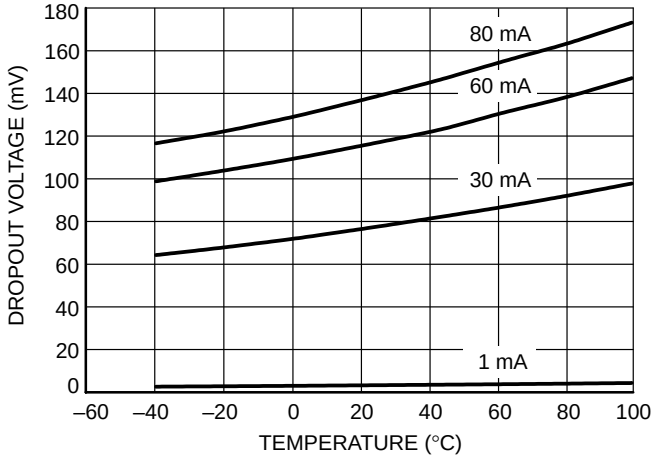



**Figure 5. Dropout versus Temperature**

## APPLICATION HINTS

### Input Decoupling

As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A 1μF capacitor either ceramic or tantalum is recommended and should be connected close to the MC33762 package. Higher values will correspondingly improve the overall line transient response.

### Output Decoupling

Thanks to a novel concept, the MC33762 is a stable component and does not require any specific Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3Ω can thus safely be used. The minimum decoupling value is 1μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

### Noise Performances

Unlike other LDOs, the MC33762 is a true low—noise regulator. Without the need of an external bypass capacitor, it typically reaches the incredible level of 40μVRMS overall noise between 100 Hz and 100 kHz. To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics. The classical bypass capacitor impacts the start—up phase of standard LDOs. However, thanks to its low—noise architecture, the MC33762 operates without a bypass element and thus offers a typical 40μs start—up phase.

### Protections

The MC33762 hosts several protections, giving natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a maximum value of 180 mA *typical* while temperature shutdown occurs if the die heats up beyond 125°C. These values let you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$P_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

If $T_{Jmax}$ is limited to 125°C, then the MC33762 can dissipate up to 395mW @ 25°C. The power dissipated by the MC33762 can be calculated from the following formula:

$$Ptot = \left(V_{in} \times I_{gnd}(I_{out})\right) + \left(V_{in} - V_{out}\right) \times I_{out}$$

or

$$Vin_{max} = \frac{Ptot + V_{out} \times I_{out}}{I_{gnd} + I_{out}}$$

If a 80mA output current is needed, the ground current is extracted from the data–sheet curves: 4mA @ 80mA. For a half 2.8V MC33762 (2.8 V) operating at 25°C, the maximum input voltage will then be 7.3V.

### Typical Applications

The following picture portrays the typical application of the MC33762.

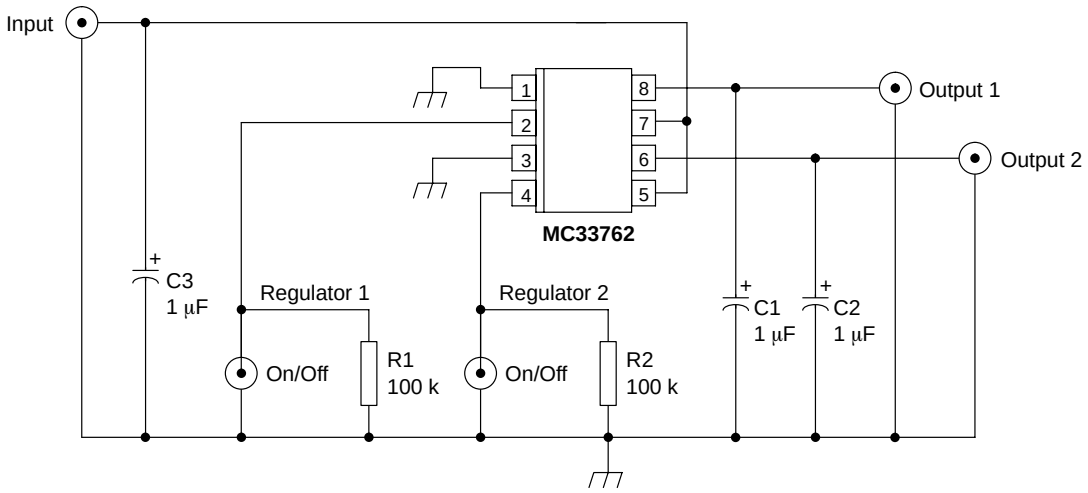



**Figure 6. A Typical Application Schematic**

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. Connections shall be kept short and wide. Layout example as given in the MC33761 application hints can be used as a starting basis.

## Understanding the Load Transient Improvement

The MC33762 features a novel architecture which allows the user to easily implement the regulator in burst systems where the time between two current shots is kept very small.

The quality of the transient response time is related to many parameters, among which the closed–loop bandwidth with the corresponding phase margin plays an important role. However, other characteristics also come into play like the series pass transistor saturation. When a current perturbation suddenly appears on the output, e.g. a load increase, the error amplifier reacts and actively biases the PNP transistor. During this reaction time, the LDO is in open–loop and the output impedance is rather high. As a result, the voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place with a positive overshoot. The problem appears when this overshoot decays down to the LDO steady–state value. During this decreasing phase, the LDO stops the PNP bias and one can consider the LDO asleep (Figure 7). If by misfortune a current shot appears, the reaction time is incredibly lengthened and a strong undershoot takes place. This reaction is clearly not acceptable for line sensitive devices, such as VCOs or other Radio–Frequency parts. This problem is dramatically exacerbated when the output current drops to zero rather than a few mA. In this later case, the internal feedback network is the only discharge path, accordingly lengthening the output voltage decay period (Figure 8).

The MC33762 cures this problem by implementing a clever design where the LDO detects the presence of the overshoot and forces the system to go back to steady–state as soon as possible, ready for the next shot. Figure 9 and 10 show how it positively improves the response time and decreases the negative peak voltage.

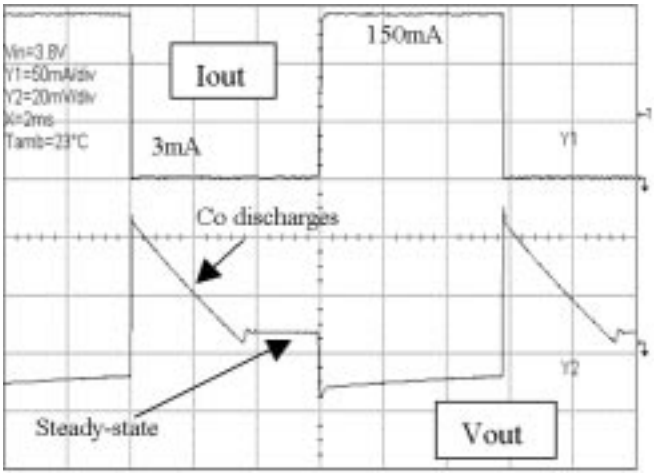



**Figure 7. A standard LDO behavior when the load current disappears**

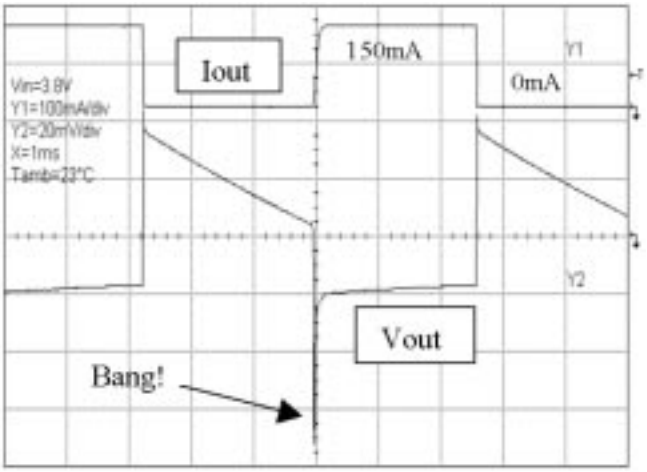



**Figure 8. A standard LDO behavior when the load current appears in the decay zone**

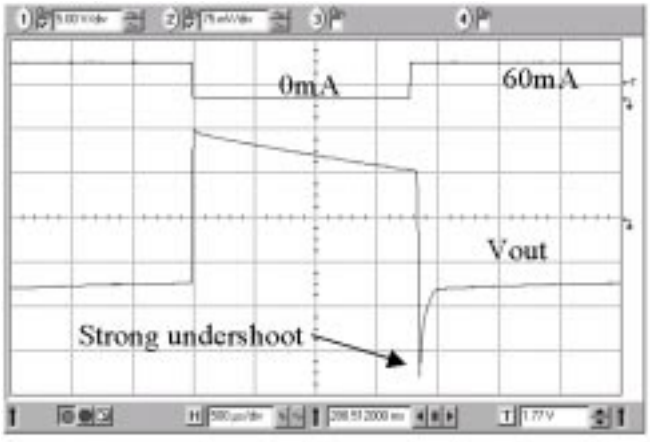



**Figure 9. Without load transient improvement**

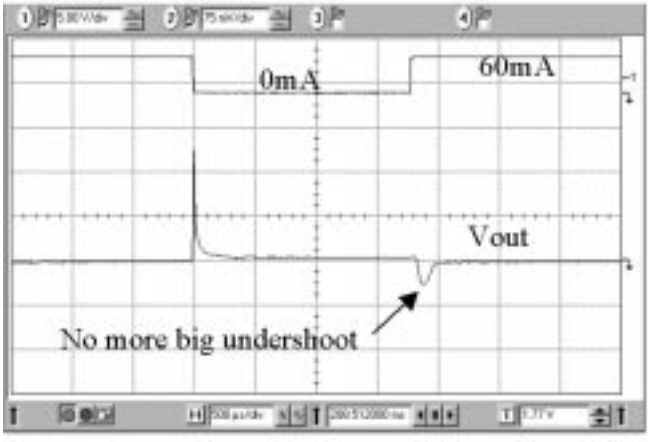



**Figure 10. MC33762 with load transient improvement**

### MC33762 has a fast start–up phase

Thanks to the lack of bypass capacitor the MC33762 is able to supply its downstream circuitry as soon as the OFF to ON signal appears. In a standard LDO, the charging time of the external bypass capacitor hampers the response time. A simple solution consists in suppressing this bypass element but, unfortunately, the noise rises to an unacceptable level. MC33762 offers the best of both worlds since it no longer includes a bypass capacitor and starts in less than 40µs typically (Repetitive at 200Hz). It also ensures an incredible low–noise level of 40µVRMS 100Hz–100kHz. The following picture details the typical 33762 startup phase.

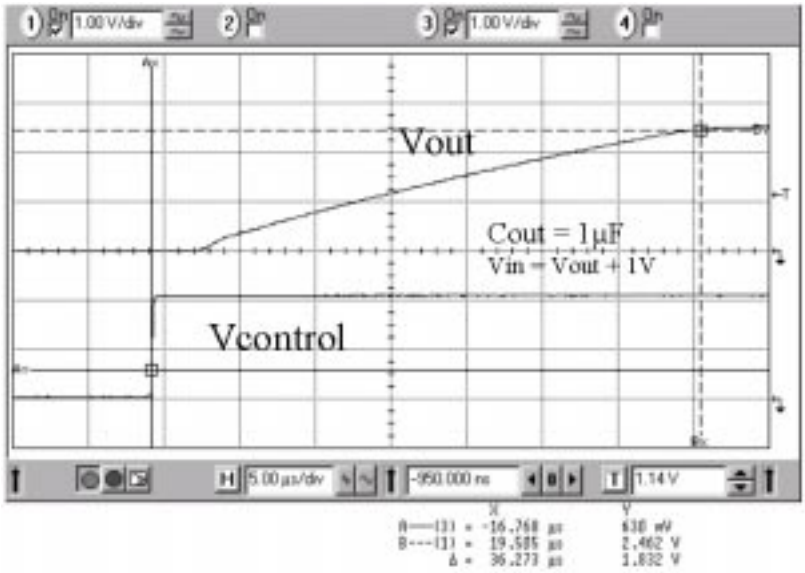



**Figure 11. Repetitive Start–Up Waveforms**

## TYPICAL TRANSIENT RESPONSES

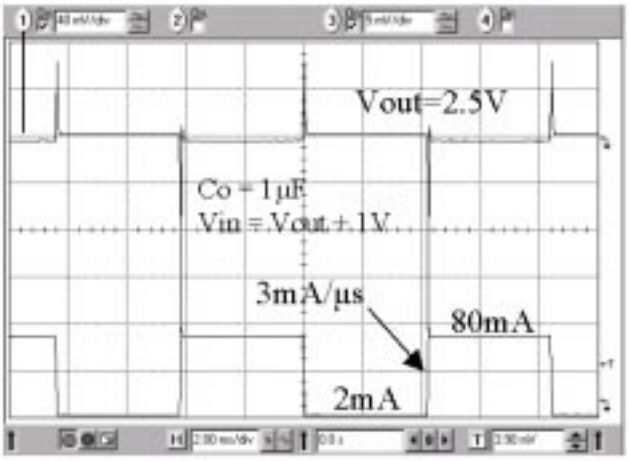



**Figure 12. Output is pulsed from 2mA to 80mA**

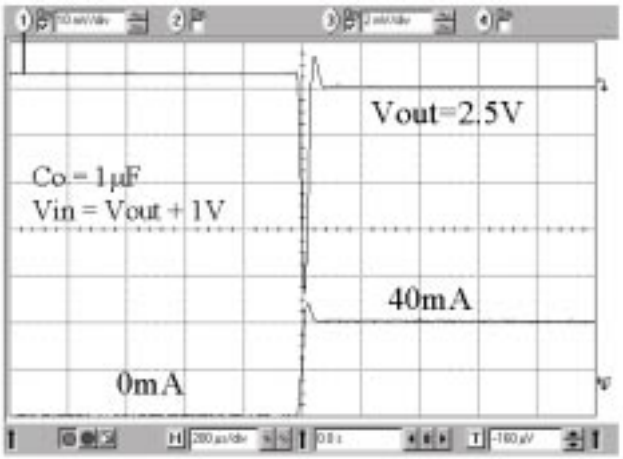



**Figure 13. Discharge effects from 0 to 40mA**

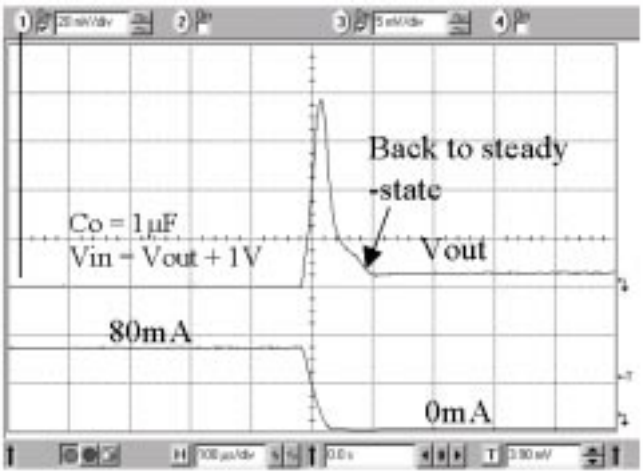



**Figure 14. Load transient improvement effect**

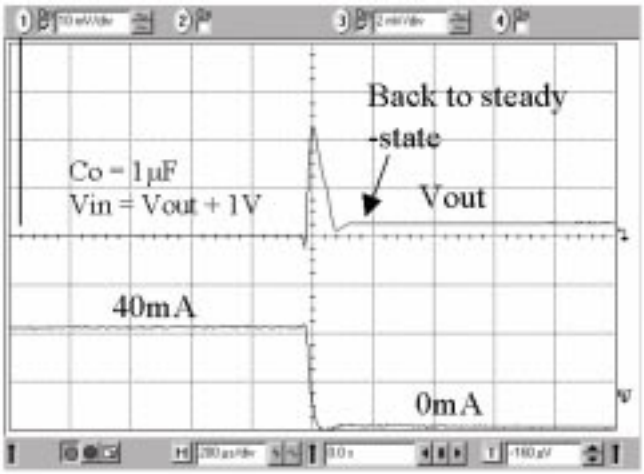



**Figure 15. Load transient improvement effect**

## TYPICAL TRANSIENT RESPONSES

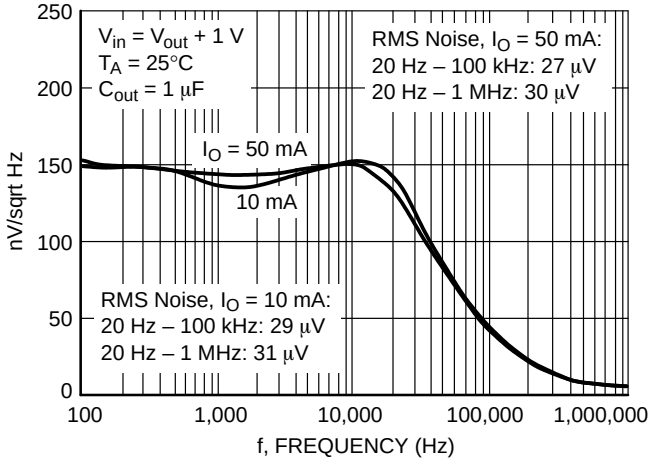



**Figure 16. MC33762 Typical Noise Density Performance**

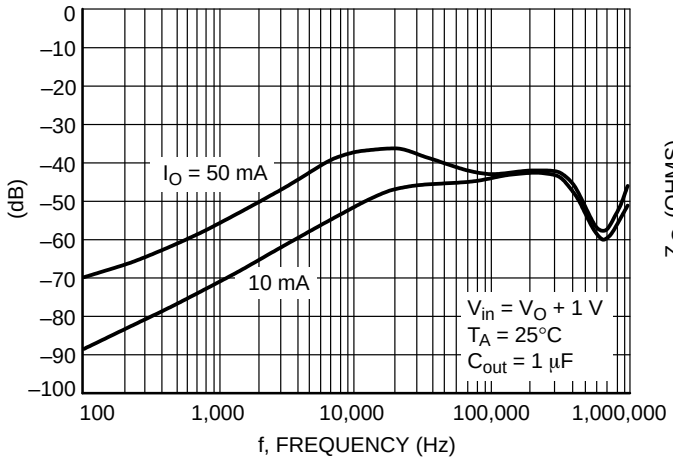



**Figure 17. MC33762 Typical Ripple Rejection Performance**

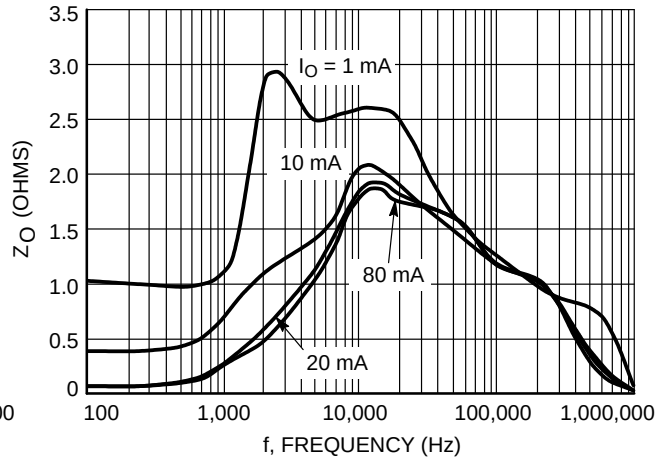
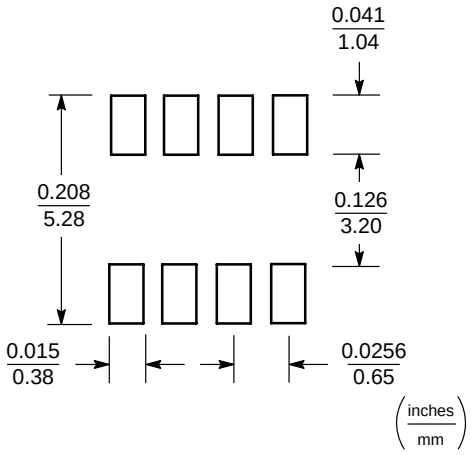



**Figure 18. Output Impedance Plot $C_{out}$ = 1 μF, $V_{in}$ = $V_{out}$ + 1 V**

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.

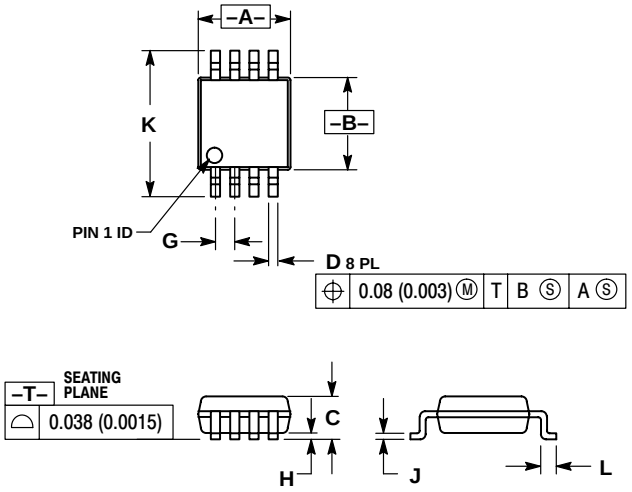


## ORDERING INFORMATION

| Part Number | Voltage Output | Package | Shipping |
|---|---|---|---|
| MC33762DM–2525R2 | 2.5V & 2.5V | Micro–8 | 4000 Units / Tape & Reel |
| MC33762DM–2828R2 | 2.8V & 2.8V | Micro–8 | 4000 Units / Tape & Reel |
| MC33762DM–3030R2 | 3.0V & 3.0V | Micro–8 | 4000 Units / Tape & Reel |

## PACKAGE DIMENSIONS

**Micro8**
PLASTIC PACKAGE
CASE 846A–02
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.25 | 0.40 | 0.010 | 0.016 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.05 | 0.15 | 0.002 | 0.006 |
| J | 0.13 | 0.23 | 0.005 | 0.009 |
| K | 4.75 | 5.05 | 0.187 | 0.199 |
| L | 0.40 | 0.70 | 0.016 | 0.028 |

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