MC33567

Advance Information

Dual Linear Controller for High Current Voltage Regulation

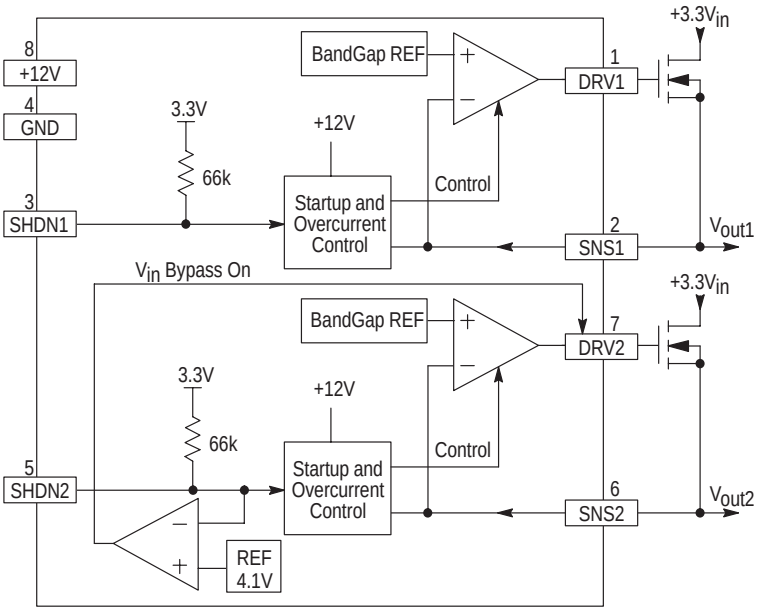
The MC33567 Dual Linear Controller is designed for motherboard/mainboard applications requiring reliable regulation of high current supply planes. This advanced linear IC provides the necessary drive, sense, and control signals to interface two separate N–channel MOSFETs as individual series pass elements regulating two different supply planes.

Use of this device lowers costs as well as ameliorates layout problems on pc motherboard products. Additionally, an under voltage–based short circuit detection and protection feature is provided which places system operation into a protected mode pending removal of the short.

Features

- Detects under voltage condition (short circuit condition) and places regulation into a protective “hiccup” mode, thus preventing damage and permitting recovery after short circuit condition is corrected
- Drive capability for SOT–223, DPAK, and D2PAK MOSFETs
- MC33567–1 controls two separate series pass transistors to provide regulation for separate 1.5V and a 1.8V supply planes. MC33567–2 controls two separate series pass transistors to provide regulation for separate 2.5V supply planes

Simplified Functional Block Diagram



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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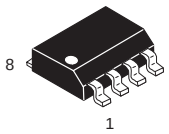
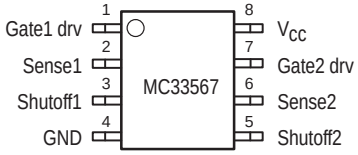


SO–8
D SUFFIX
CASE 751

PIN CONNECTIONS



ORDERING INFORMATION

Device	Output Voltage	Shipping
MC33567D–1	1.8V, 1.5/3.3V	98 Units/Rail
MC33567D–1R2	1.8V, 1.5/3.3V	2500 Tape&Reel
MC33567D–2	2.5V, 2.5V	98 Units/Rail
MC33567D–2R2	2.5V, 2.5V	2500 Tape&Reel

MAXIMUM RATINGS

Parameter	Symbol	Max Value	Unit
Supply Voltage	V_{cc}	12.5	Vdc
Operating Ambient Temperature	T_a	0 to +80	°C
Operating Junction Temperature	T_J	– 5 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$[1]	180	°C/W

DEVICE MARKING

Device	Type	Package	Marking (1st Line)
MC33567–1	1.818 V, 1.515 V	SO–8	M5671
MC33567–2	2.525 V, 2.525 V	SO–8	M5672

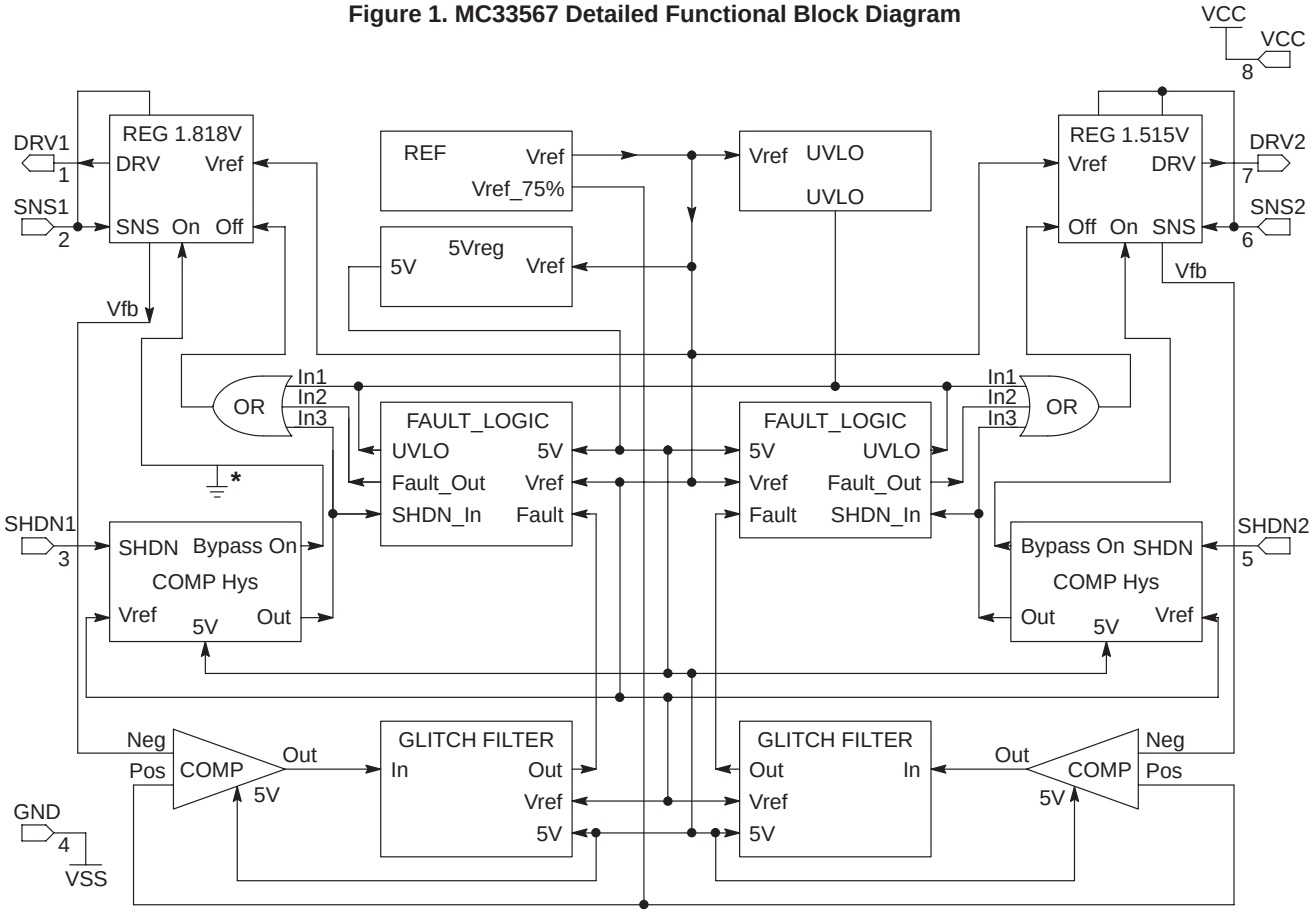
PIN ASSIGNMENTS AND FUNCTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	Gate 1 drive	Drives mosfet in linear region. Is internally clamped to ground in power down mode.
2	Sense 1 line	Returns regulated output from mosfet.
3	Shutoff 1	At TTL high level turns off regulation for gate 1. Effectively grounds gate 1. (Internal pullup to 3.3V)
4	Ground	
5	Shutoff 2	At TTL high level turns off regulation for gate 2. Effectively grounds gate 2. (Internal pullup to 3.3V)
6	Sense 2 line	Returns regulated output from mosfet.
7	Gate 2 drive	Drives mosfet in linear region. Is internally clamped to ground in power down mode.
8	12 volt input	Supply voltage for operation and gate drive output.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Regulation (Full–load to no–load @ 25 – 70°C)	Vreg%	–2.5	—	+2.5	%
Peak Gate Drive Output (pin 1, pin 7)	I_{pkdrv}	10	20	30	mA
Drive Sink Current (steady state)	I_{sink}	5.0	7.0	10	mA
Short Circuit / Undervoltage Detect (load current increased until output drops)	ss/uvd	70	—	80	% Vo
Quiescent Current	I_q	—	7	10	mA
Under Voltage Lock Out	UVLO	7.0	8.5	9.0	V
Hysteresis	hys	0.2	0.5	0.9	V
Shutoff Threshold (Lower)	SHDN	0.8	1.13	1.29	V
Shutoff Hysteresis	$SHDN_{hys}$	—	130	—	mV
Short Circuit Response Time	SC_{td}	—	250	—	μS
Short Circuit Off Time	SC_{toff}	20	40	60	mS
Short Circuit On Time	SC_{ton}	0.5	0.8	1.5	mS
Shutoff Disable Time	$SHDN_{tdis}$	—	0.5	2.0	μS

Figure 1. MC33567 Detailed Functional Block Diagram



* Internal ground disables Bypass On Function on the 1.8V regulator in the MC33567–1 and on the 2.5V regulators of the MC33567–2.

FUNCTIONAL DESCRIPTION

Overcurrent Protection – Hiccup Mode

On detection of overcurrent, output goes into hiccup mode where on period is 40 times shorter than off time. I.e., 1.0 msec ON, 40 msec OFF. When an overcurrent condition exists, the output voltage will drop below the threshold. The output is then turned on and off in a 1:40 duty cycle. Each transition low to high of the enable input restarts the hiccup mode holdoff period.

Shutoff (Shutdown) Function

Each internal regulator has an active high enable input. If the input is held above the minimum threshold, the regulator will operate normally. If the input is held low, the regulator is turned off.

Logic table for Shutoff (Pin 3) on the 1.5V regulator:*

Shutoff Pin	1.5V Regulator Output
No Connect	1.5V
< 0.8V	Shutoff
2.0V < SHDN < 4.2V	1.5V
> 4.1V	3.3V – Full ON

*See Figure 4, 1.5V / 3.3V AGP card detection

NOTE: MC33567–2 does not have full–on bypass feature

Logic table for Shutoff (Pin 3) on the 1.8V regulator:

Shutoff Pin	1.8V Regulator Output
No Connect	1.8V
< 0.8V	Shutoff
> 2.0V	1.8V

This part has under voltage detection that uses the channel resistance of an internal N–channel FET to put the regulator into “hiccup mode” when a short is present on the regulated voltage plane. Under voltage detection is set to ∼75% of regulation set point.

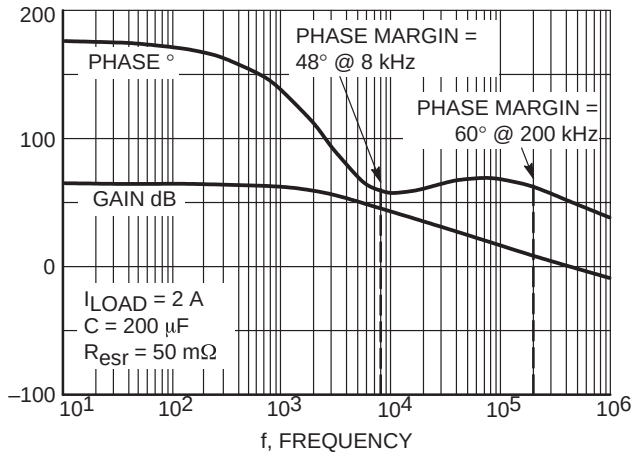


Figure 2. Gain–Phase Plot @ 50 mΩ

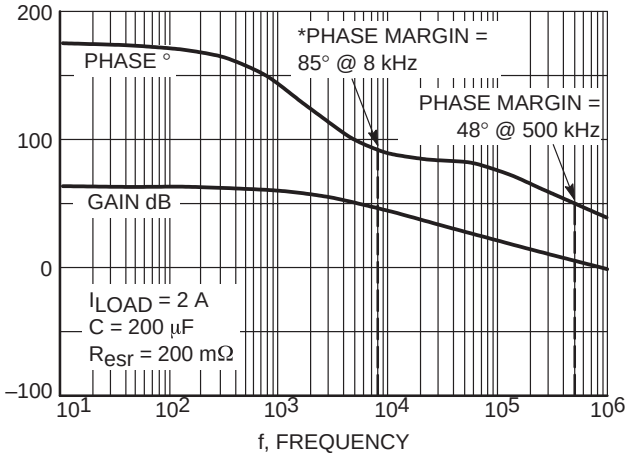


Figure 3. Gain–Phase Plot @ 200 mΩ

*NOTE: For adequate phase margin, C X R ≥ 10 X 10^{-6}.
E.g. 200 μF X 50 mΩ = 10 X 10^{-6},
400 μF X 25 mΩ = 10 X 10^{-6},
800 μF X 12.5 mΩ = 10 X 10^{-6}.

Capacitor Selection Guidelines

The goal here is to preserve adequate phase margin for stable operation. For adequate phase margin, the load capacitance ESR value multiplied by the load capacitance must be greater than 10x10^{-6}. For example, if the load capacitor is 400μF, then the ESR value of the capacitor would need to be no less than 25 milliOhms, (400μF x 25mOhm = 10x10^{-6}). Similarly, if the load capacitance was 200μF, then the ESR value of the capacitance would need to be at least 50 milliOhms, (200μF x 50mOhm = 10x10^{-6}). (**Important Note:** The foregoing rule assumes that all capacitors across the load are of the same type and value. If different types and values of capacitors are used in parallel across the load, then each individual capacitors must meet the C x ESR > 10x10^{-6} rule).

PCB Layout Guidelines

The goal here is to minimize extraneous signals from being either magnetically or electrostatically induced on the sense lines or drive lines. As much as practical, the LDO control ic should be physically close (short traces) to the external series pass transistors; the layout of the sense trace should parallel, go in the same direction, and be on the same plane as the power trace going from the series pass transistor source lead to the load; routing the sense lead near the load current return path should be avoided; unterminated runs of the sense lead should be avoided (if options on sense lead destinations are desired on the board, then use zero ohm resistor jumpers to make the alternate sense lead connections near the sense pin itself).

PIN 5 TRUTH TABLE
Pin 5 No connect = 1.5V LDO drive out active
Pin 5 < 0.8V = shutoff (drive out 0V)
2.5V < pin 5 < 4.1V = 1.5V LDO drive out active
Pin 5 > 4.1V = 3.3V bypass mode (drive out = V_{CC})

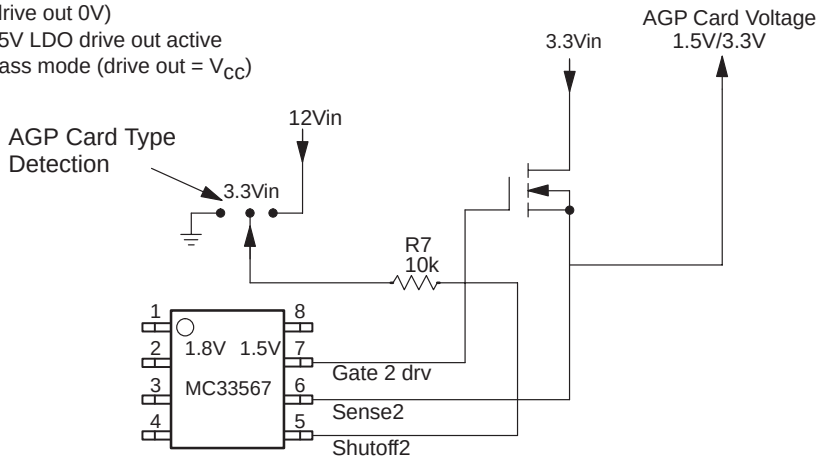
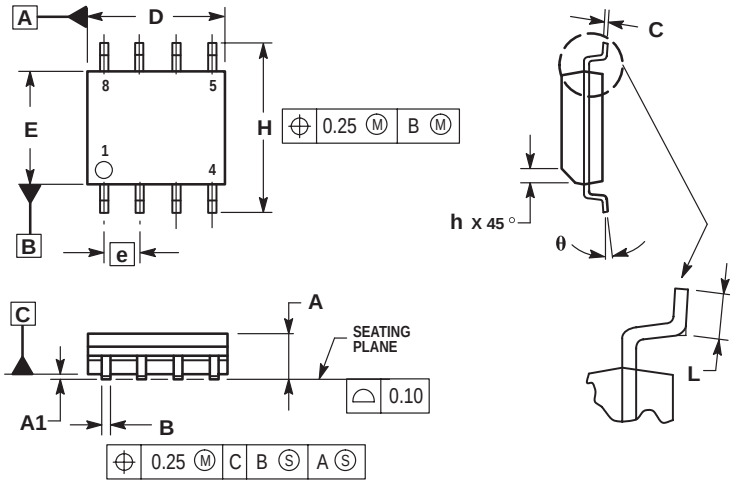


Figure 4. 1.5V/3.3V AGP card detection

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0 °	7 °

Notes

PUBLICATION ORDERING INFORMATION

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Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5740–2745
Email: r14525@onsemi.com

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