MC33565

Smart Voltage Regulator for Peripheral Card Applications

The MC33565 Low Drop Out Voltage Regulator is designed for computer peripheral card applications, allowing glitch–free transitions from “sleep” to “active” system modes. It has internal logic circuitry to detect whether there is a 5 V supply (“active” system mode) or an auxiliary 3.3 V supply (“sleep” system mode). A guaranteed 3.3 V regulated output voltage at 200 mA is always available even if the main 5 V supply drops out.

The regulated 3.3 V output voltage is provided by either an internal dropout 5.0 V–to–3.3 V voltage regulator or an external P–channel MOSFET, depending on the system being in the “active” or “sleep” mode.

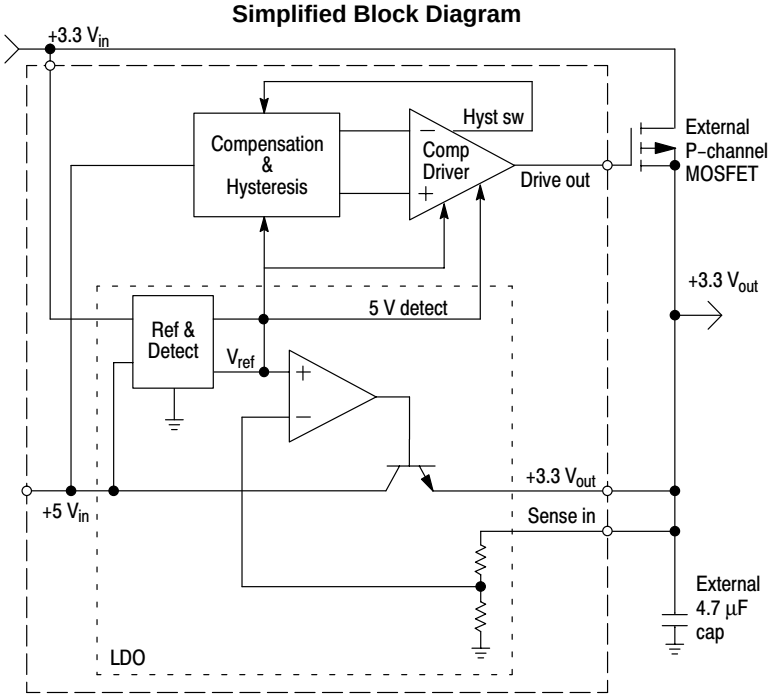
Features

- Glitch–Free Transition from “Sleep” to “Active” Mode
- Compatible with *Instantly Available* PC Systems
- Output Current up to 200 mA
- Output Regulated to 2% over Temperature
- Excellent Line and Load Regulation (0.4%)
- Prevents Reverse Current Flow during Sleep Mode

Applications

- Computer
- Ethernet
- PCI/NIC Cards

Simplified Block Diagram

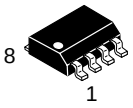


ON Semiconductor

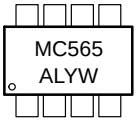
http://onsemi.com

200 mA INTELLIGENT LDO REGULATOR WITH SMART BYPASS CONTROL

MARKING DIAGRAM

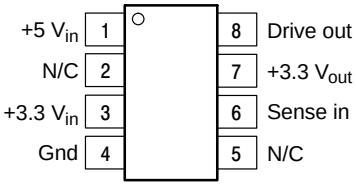


SOIC–8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



Pins 2 and 5 Not Connected

ORDERING INFORMATION

Device	Package	Shipping
MC33565D	SOIC–8	98 Units / Rail
MC33565DR2	SOIC–8	2500 / Tape & Reel

MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted) **(Note 1.)**

Parameter	Symbol	Max Value	Unit
Input Voltage, V_{CC}	V_{max}	7.0	Vdc
	V_{min}	–0.5	Vdc
Operating Ambient Temperature	T_a	–5 to +70	°C
Operating Junction Temperature	T_J	– 5 to +150	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 1.)	171	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	28	°C/W

1. Minimum pad test board with 5 mil wide and 2.8 mil thick copper traces 1 inch long.

AC ELECTRICAL SPECIFICATIONS (Notes 1., 2., 3., and 4.)

Parameter	Symbol	Min	Typ	Max	Unit
Drive High Delay (V_{in} ramping up) C_{Drive} = 1.2 nF, measured from +5 V_{in} = $V_{thresHi}$ to V_{Drive} = 2 V	t_{DH}	—	1.3	3.5	μS
Drive Low Delay (V_{in} ramping down) C_{Drive} = 1.2 nF, measured from +5 V_{in} = $V_{thresLo}$ to V_{Drive} = 2 V	t_{DL}	—	1.2	3.5	μS

1. See 5 V Detect Thresholds Diagram.
2. Recommended source impedance for 5 V supply: ≤ 0.25 Ω. This will ensure that I_o x R_{source} < V_{hyst}, thus avoiding drive out toggling during 5 V detect threshold transitions.
3. See Figure 2. Application Block Diagram.
4. See Timing Diagram.

DC ELECTRICAL CHARACTERISTICS (Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
+5 V_{in} Supply Voltage Range	+5 V_{in}	4.3	5.0	5.5	Vdc
Reverse Leakage Current from Output	$I_{reverse}$	—	—	25	μA
V_{Aux} quiescent current	—	—	—	3.0	mA
+5 V_{in} quiescent current, operating	—	—	—	10	mA
Load Capacitance (Note 2.)	C_{load}	4.7	22	—	μF
REGULATOR OUTPUT					
Output Voltage (4.3 V ≤ V_{in} ≤ 5.5 V, 0 mA ≤ I_o ≤ 200 mA) T_A = 25°C (T_J = –5°C to 150°C)	+3.3 V_{out}	 3.267 3.234	 3.30 3.30	 3.333 3.366	Vdc
In–to–Out Voltage (3.9 V ≤ V_{in} ≤ 4.3 V, V_{aux} = 3.3 V)	V_d	3.0	—	—	Vdc
Voltage Out at Max Voltage In (V_{in} = 7 V)	V_{outmax}	3.1	3.3	3.5	Vdc
Line Regulation (I_o = 200 mA)	—	—	—	0.4	%
Load Regulation (I_o = 0 to 200 mA)	—	—	—	0.4	%
Short Circuit Current	I_{sc}	230	435	—	mA
5 V DETECT					
Low Threshold Voltage (+5 V_{in} falling)	$V_{thresLo}$	3.9	4.02	4.3	Vdc
High Threshold Voltage (+5 V_{in} rising)	$V_{thresHi}$	—	4.17	4.3	Vdc
Hysteresis	V_{Hyst}	0.12	0.15	0.18	Vdc

1. –5°C < T_a < 70°C, 4.3 V < V_{in} < 5.5 V, C_{load} = 4.7 μF unless otherwise noted
2. 4.7 μF minimum over temperature; 22 μF recommended; 500 mΩ ESR maximum.

DC ELECTRICAL CHARACTERISTICS (Note 1.) (continued)

DRIVE OUTPUT

Characteristic	Symbol	Min	Typ	Max	Unit
Output peak source Current (+5 V_{in} > $V_{thresHi}$, Pin 8 current into 1.2 nF)	I_{peak}	15	—	—	mA
Output peak sink Current (+5 V_{in} < $V_{thresLo}$, Pin 8 current into 1.2 nF)	I_{peak}	15	—	—	mA
Low Output Voltage (I_{oL} = 200 μA, V_{in} < $V_{thresLo}$)	V_{oL}	—	145	200	mVdc
High Output Voltage (I_{oH} = 200 μA)	V_{oH}	3.4	V_{in}–0.85	—	Vdc

1. –5°C < T_a < 70°C, 4.3 V < V_{in} < 5.5 V, C_{load} = 4.7 μF unless otherwise noted

DEVICE MARKING

Device	Type	Sub–type	Marking (1st Line)
MC33565D	3.3 V	—	MC565

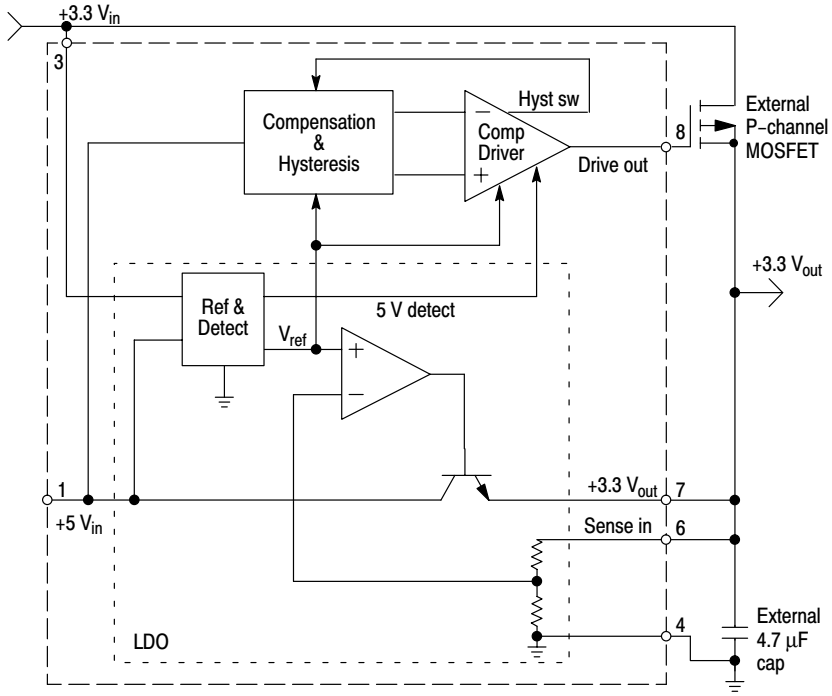


Figure 1. Functional Block Diagram

PIN ASSIGNMENTS AND FUNCTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	+5 V_{in}	This is the input supply for the IC. Typical voltage 5 V.
2, 5	N/C	Reserved
3	+3.3 V_{in}	Auxiliary input. Typical voltage 3.3 V.
4	Gnd	Logic and Power Gnd.
6	Sense in	Load–sense voltage input to internal regulator.
7	+3.3 V_{out}	3.3 V output provided to the application circuit (output current is sourced to this pin from the 5 V input.)
8	Drive out	This output drives a P–channel MOSFET with up to 1.2 nF of “effective” gate capacitance. Recommended device is MGSF1P02ELT MOSFET. Drive out has active internal pull–up and pull–down circuitry to guarantee fast transitions.

OPERATING DESCRIPTION

The MC33565 is designed for power managed computer applications such as peripheral card interface (PCI) and network interface cards (NIC) where glitch–free transition between +3.3 V and +5 V is necessary. In this type of application, the presence of a +5 V supply represents the “active” system mode, while the presence of +3.3 V represents the “sleep” system mode. The MC33565 complies with the *instantly available requirements* as specified by the Advanced Configuration and Power Interface (ACPI) standards set by Intel, Microsoft, and Toshiba. A regulated output voltage of +3.3 V is available even when the +5 V supply has been shut down and only the +3.3 V auxiliary supply is available.

The MC33565 has dual inputs, +5 V_{in} and +3.3 V_{in}. It functions as a linear regulator when V_{in} is greater than 4.02 V. Below this threshold value, the linear regulator turns off and the auxiliary DRIVE OUT feature allows the use of an external P–channel MOSFET to supply power to the output. The MC33565 connects the +3.3 V_{in} auxiliary power supply directly to the output P–channel MOSFET.

5 V Detect

Internal circuitry detects if the system is being powered from a +5 V supply or a 3.3 V auxiliary supply. During normal operating conditions, the MC33565 is powered by the +5 V supply. A regulated output voltage of +3.3 V is provided by an internal low drop out 5.0 V–to–3.3 V voltage regulator. The gate of the P–channel MOSFET is driven high and therefore disabled.

If the +5 V supply is not available or the supply voltage drops below a typical threshold value of 4.02 V, the DRIVE OUT goes low. This enables the external P–channel MOSFET, connecting the +3.3 V auxiliary supply to the load and allowing the load to remain powered even though the +5 V supply is not available.

As the supply voltage begins to rise, the linear regulator output will be disabled until V_{in} reaches a typical threshold voltage of 4.17 V. The load continues to be powered by the auxiliary DRIVE OUT while V_{in} reaches the threshold voltage. When V_{in} reaches the threshold voltage, the gate of the external P–channel MOSFET is driven high and turns off.

The 5 V detect logic is active throughout the entire range of the +5 V supply ramp–up. The DRIVE OUT signal is never turned ON or OFF inappropriately during ramp–up of the +5 V_{in} supply. The +3.3 V output voltage never drops below 3.0 V while the +5 V supply is above the 5 V DETECT minimum threshold of 3.9 V.

Input Blocking

The internal NPN pass transistor of the low drop out regulator (LDO) ensure that no significant reverse current will flow from V_{out} to V_{in} or GND when the +5 V_{in} input is not powered and the +3.3 V_{in} supply is present.

P–Channel MOSFET Polarity

It is imperative that the polarity of the P–channel MOSFET be observed because the P–channel MOSFET body diode will be connected between the auxiliary power supply and the load. The P–channel MOSFET drain is connected to the +3.3 V_{in} auxiliary power supply; source is connected to load; gate is connected to DRIVE OUT. If the polarity is reversed with the drain connected to the load and the source connected to the auxiliary supply, the body diode could be forward biased if the auxiliary supply is not present. Consequently the linear regulator would not turn off and it would supply current to everything on the auxiliary supply rail.

Hysteresis

The internal 5 V DETECT has a typical high threshold voltage of 4.17 V and a typical low threshold voltage of 4.02 V. This results in a typical hysteresis of 150 mV for noise immunity. The input supply voltage, V_{in}, must drop 150 mV while the linear regulator is supplying power to the load before the auxiliary DRIVE OUT is enabled.

External Compensation

An external compensation capacitor with a minimum value of 4.7 μF is required for the linear regulator to be stable. Increasing the capacitance will improve the overall transient response. The equivalent series resistance (ESR) of the capacitor should be less than 1 Ω in order for the output voltage to be maintained within tight tolerance.

Sense

The SENSE IN pin provides tight regulation of the load voltage while the 5 V supply is present even with varying load current. To take advantage of the SENSE PIN, connect pin 6 as close to the load as possible. Use a separate trace to connect the source of the MOSFET to the load. Refer to Figure 2.

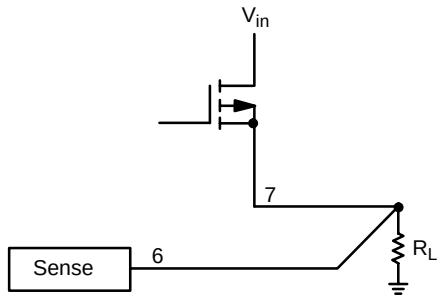


Figure 2.

Board Layout

The PCB component layout shown in Figure 28 is designed for an input range of 4.3 V to 5.5 V; an output voltage range of 3.267 V to 3.333 V; and an output current of 200 mA.

Current Limit and Thermal Shutdown

Full protection with both current limit and thermal shutdown is provided. Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.**

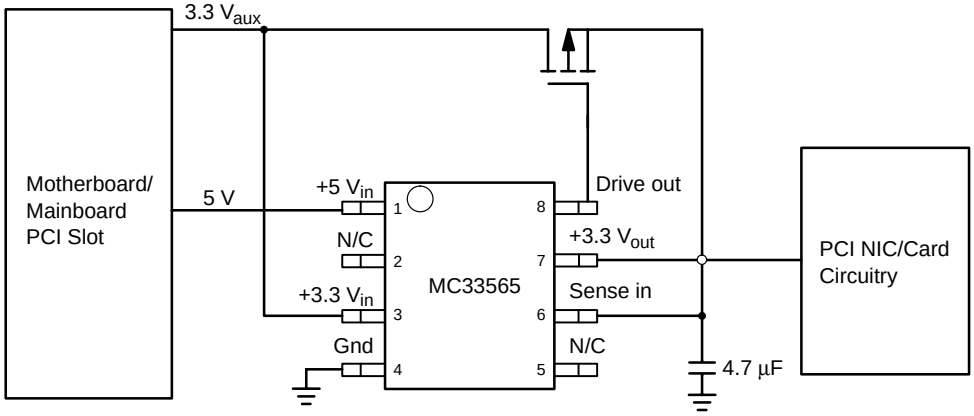


Figure 3. Application Block Diagram

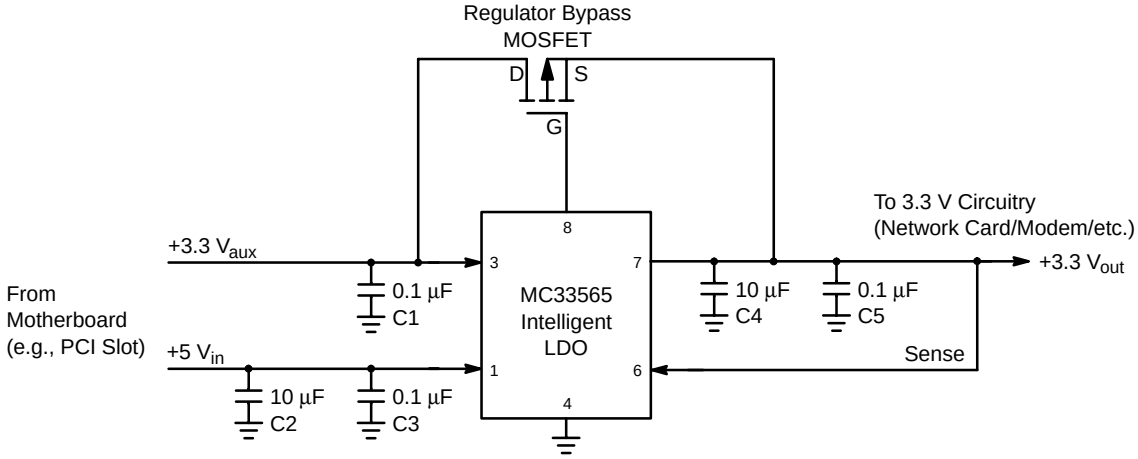


Figure 4. Typical Application Schematic

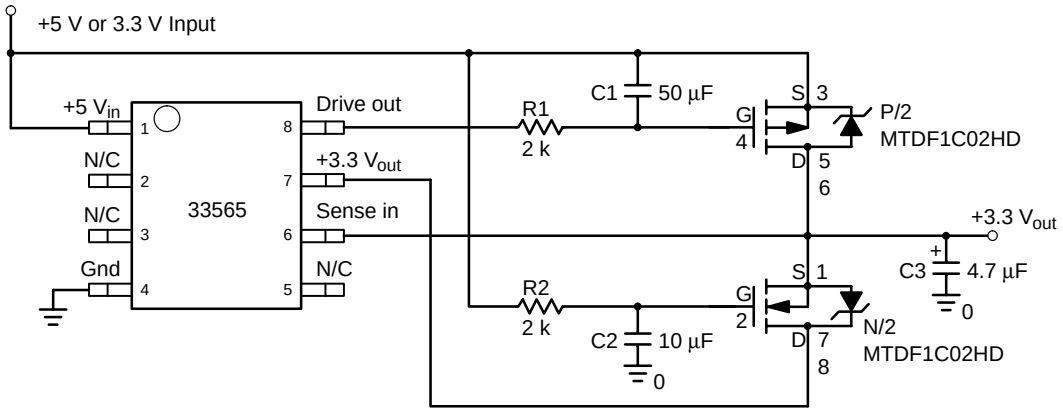
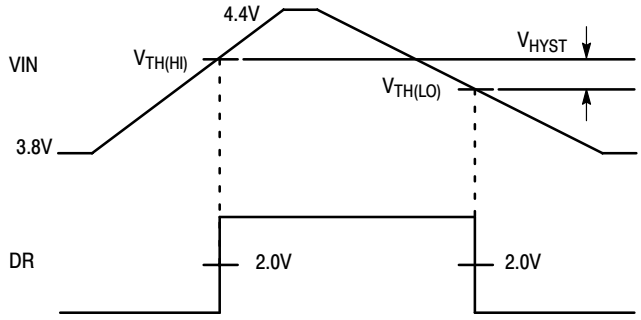


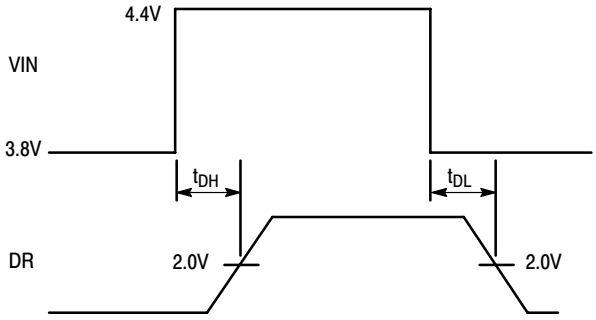
Figure 5. Alternative Application: 5 V or 3.3 V Card Input with Hot Swap Circuitry

TYPICAL CHARACTERISTICS



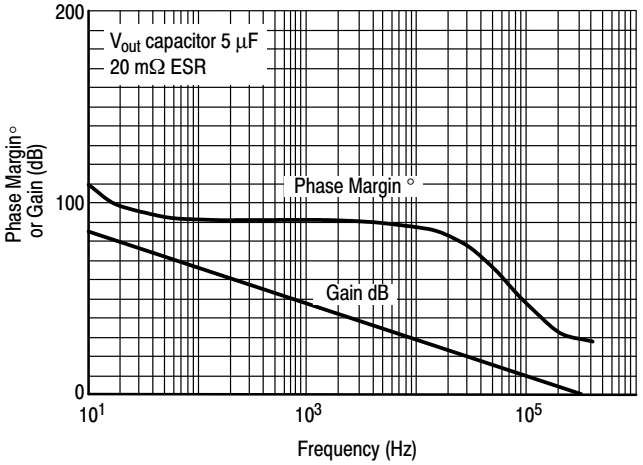
NOTE:
(1) VIN rise and fall times (10% to 90%) to be ≥ 100 μs.

Figure 6. 5V Detect Thresholds Diagram



NOTE:
(1) VIN rise and fall times (10% to 90%) to be ≤ 100 ns.

Figure 7. Timing Diagram



NOTE: V_{out} capacitor ≥ 4.7 μF over operating temperature range.
Maximum ESR permissible = 500 mΩ over operating temperature range.

Figure 8. Predicted Gain and Phase at Zero Load Current

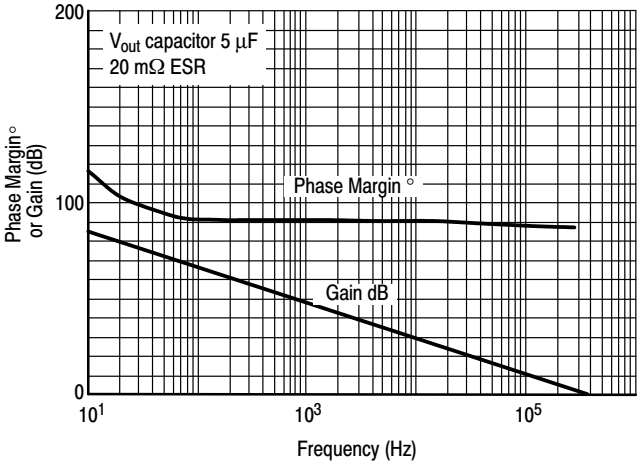


Figure 9. Predicted Gain and Phase at Full Load Current

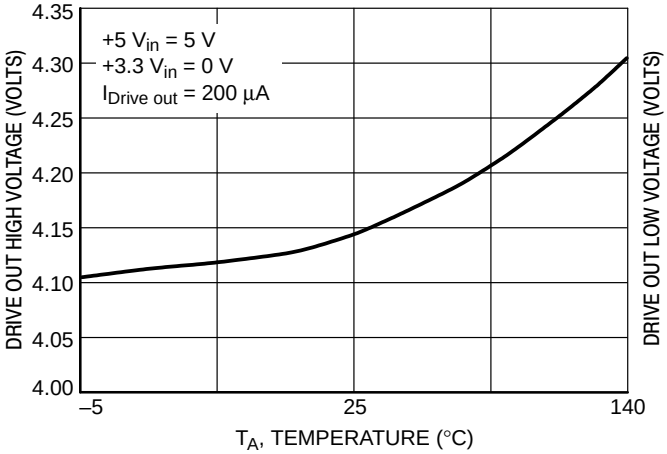


Figure 10. Drive Out High Voltage (external P–channel MOSFET turned off) versus Ambient Temperature

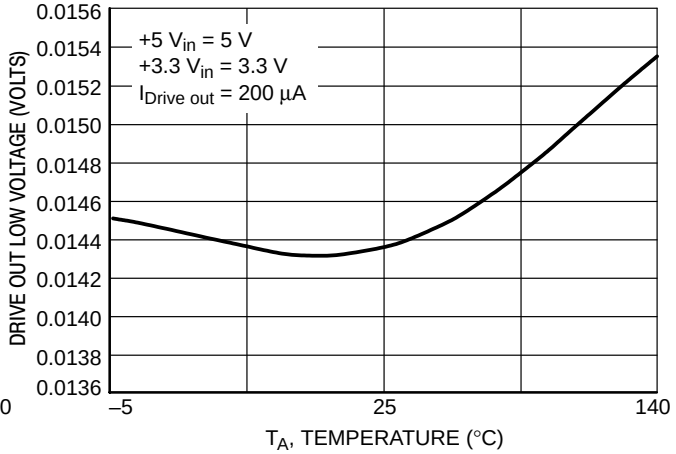


Figure 11. Drive Out Low Voltage (external P–channel MOSFET turned on) versus Ambient Temperature

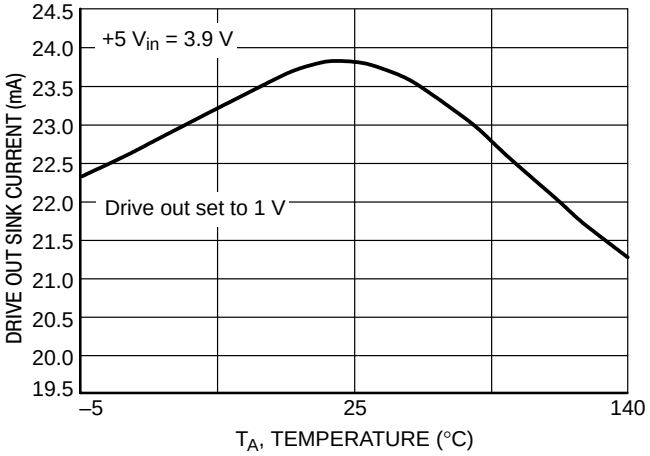


Figure 12. Drive Out Peak Sink Current versus Ambient Temperature

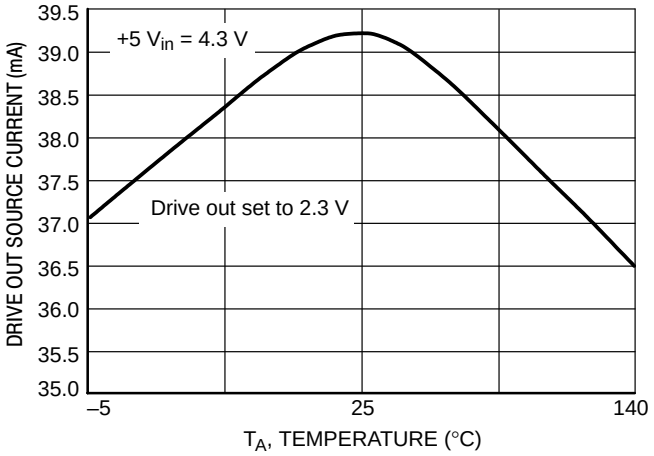


Figure 13. Drive Out Peak Source Current versus Ambient Temperature

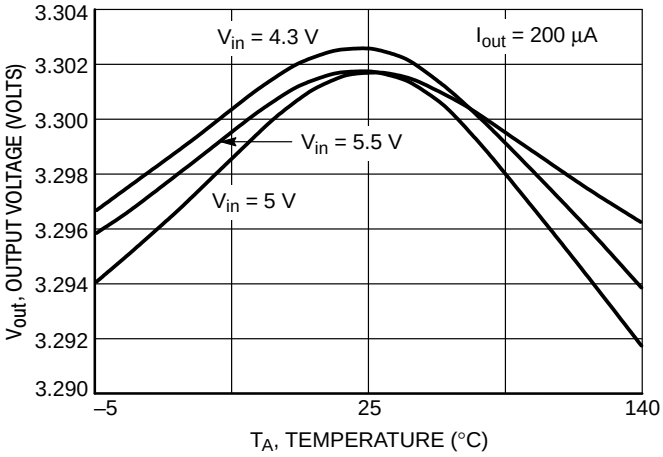


Figure 14. Output Voltage versus Ambient Temperature

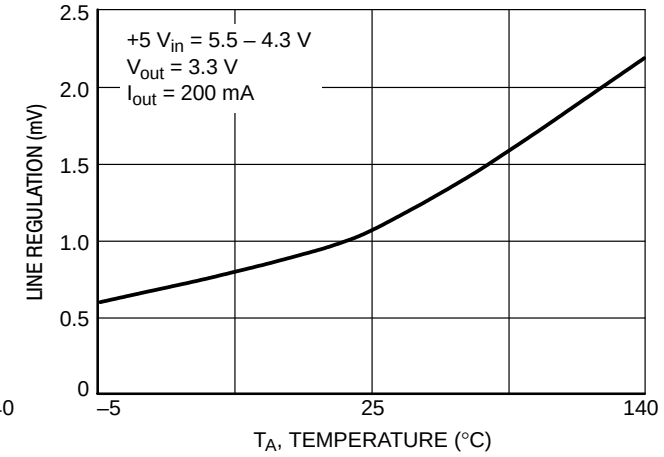


Figure 15. Line Regulation versus Ambient Temperature

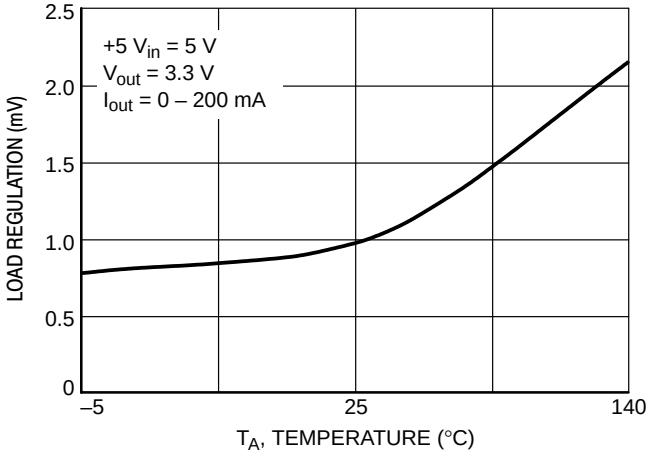


Figure 16. Load Regulation versus Ambient Temperature

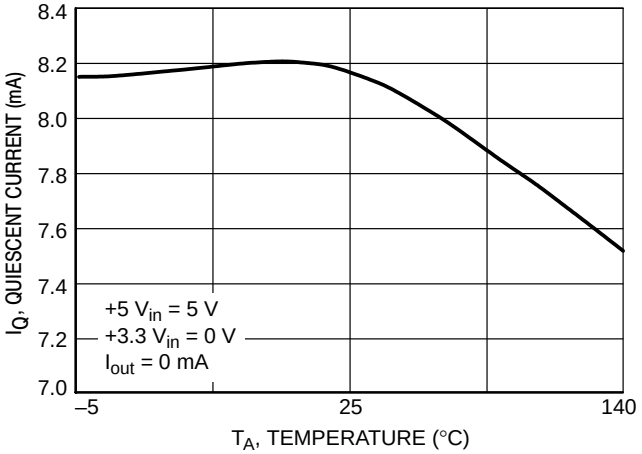


Figure 17. Quiescent Current versus Ambient Temperature (5 V only)

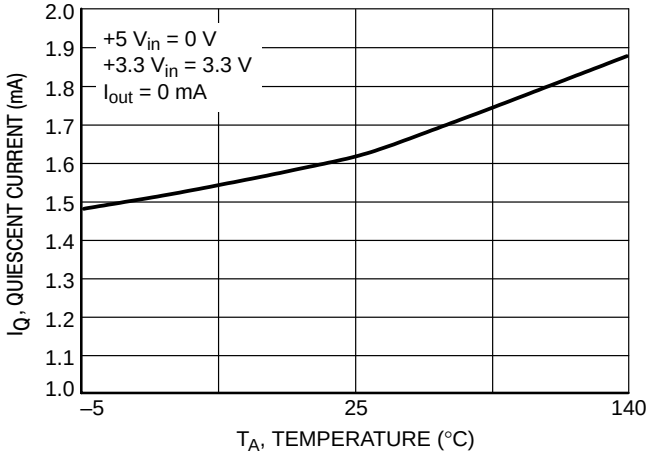


Figure 18. Quiescent Current versus Ambient Temperature (3.3 V aux only)

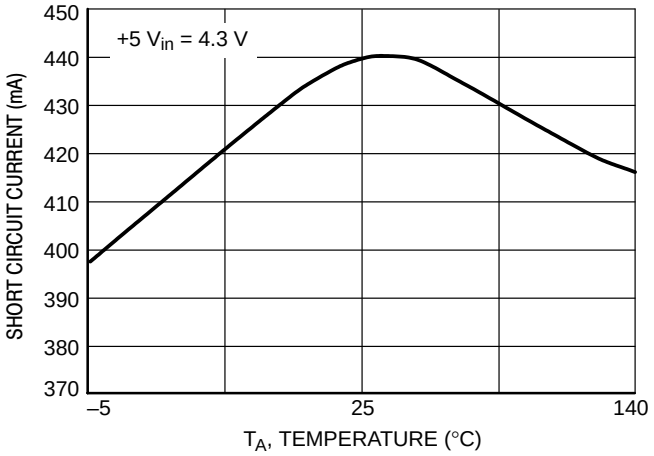


Figure 19. Short Circuit Current versus Ambient Temperature

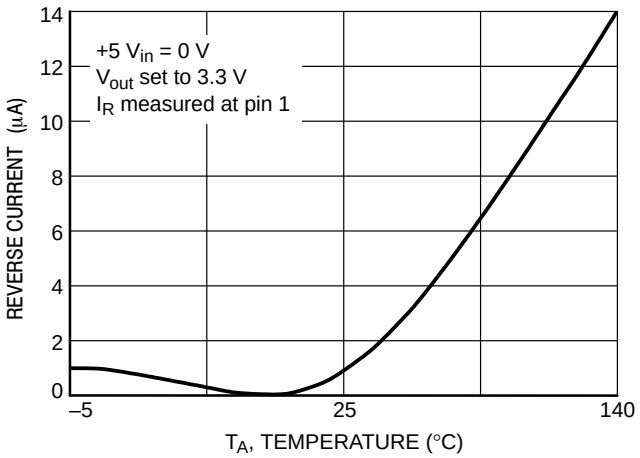


Figure 20. Reverse Leakage Current from Output versus Ambient Temperature

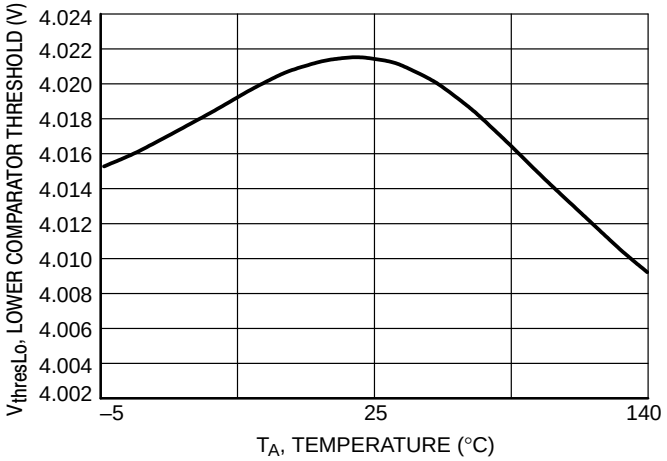


Figure 21. Lower Comparator Threshold versus Ambient Temperature

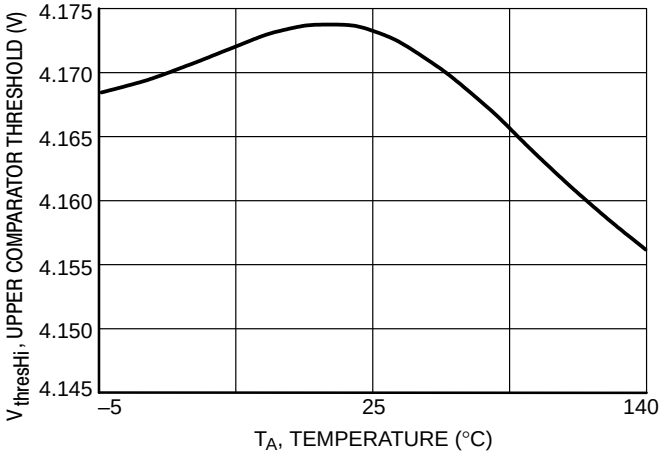


Figure 22. Upper Comparator Threshold versus Ambient Temperature

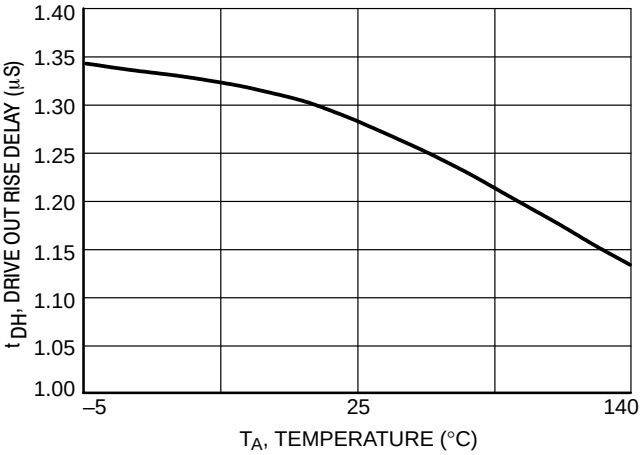


Figure 23. Drive Out Rise Delay (after V_{in} crosses threshold) versus Ambient Temperature

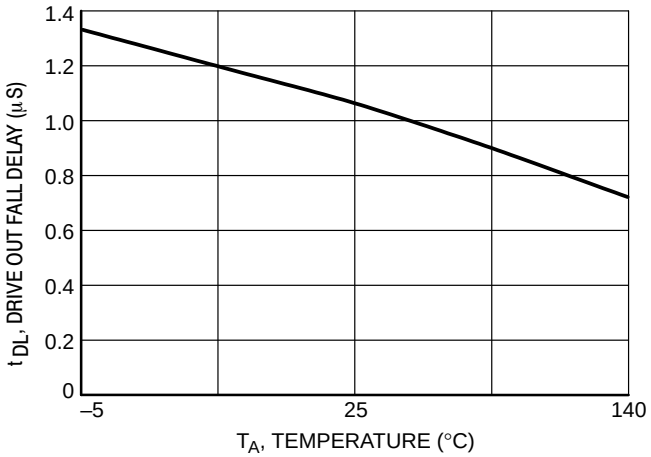
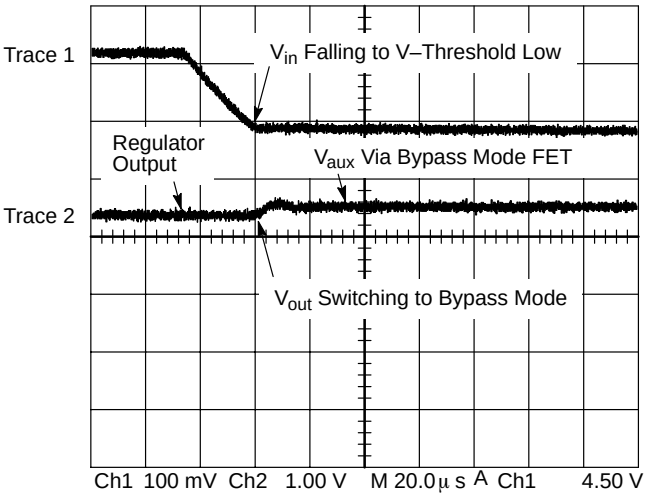
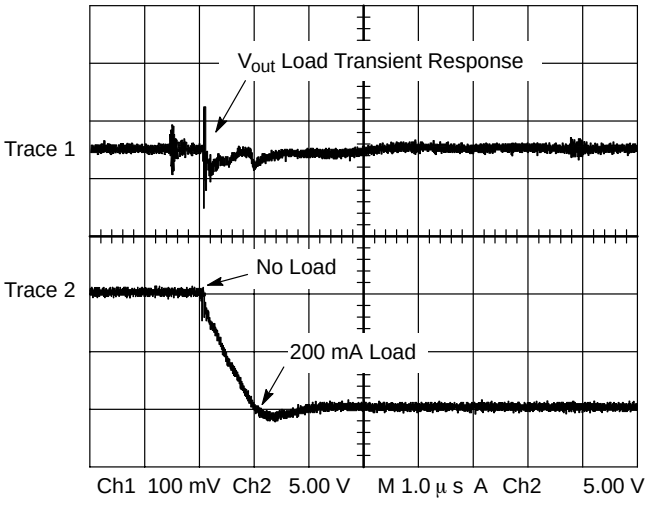


Figure 24. Drive Out Fall Delay (after V_{in} crosses threshold) versus Ambient Temperature



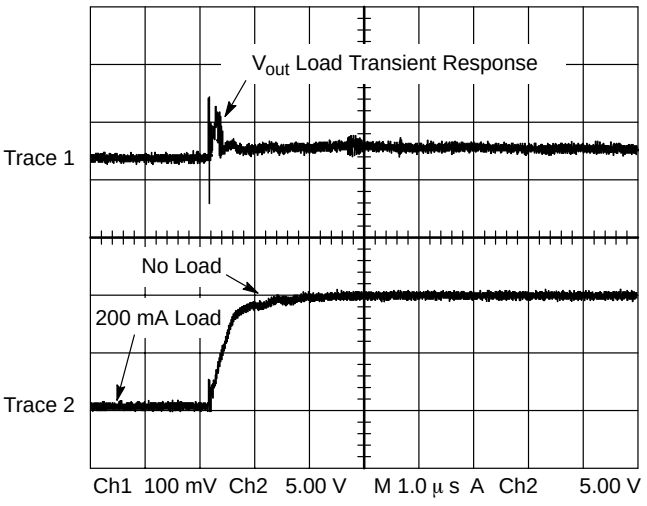
TRACE 1: V_{in} stepping from 5 V to $V_{thresLo}$
TRACE 2: V_{out} switching from regulator output to V_{aux}

Figure 25. Bypass Mode Transition



TRACE 1: V_{out} load transient response
TRACE 2: No load to 200 mA

Figure 26. Load Transient Response: Load Applied



TRACE 1: Regulator 3.3 V_{out}
TRACE 2: I_{out} stepping from 200 mA load to no load

Figure 27. Load Transient Response: Load Removed

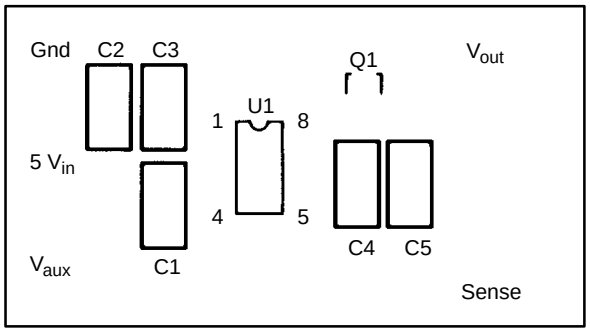


Figure 28. PCB Component Layout

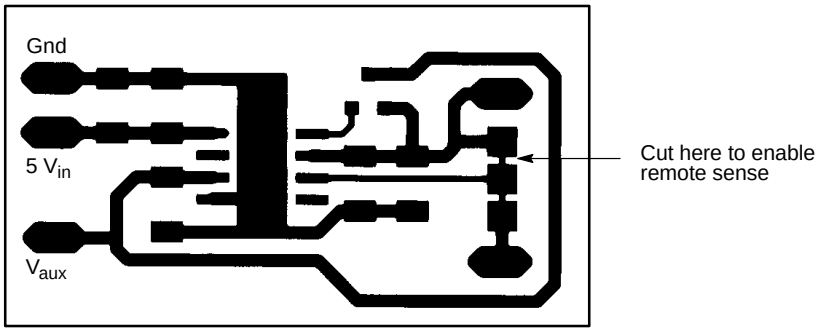


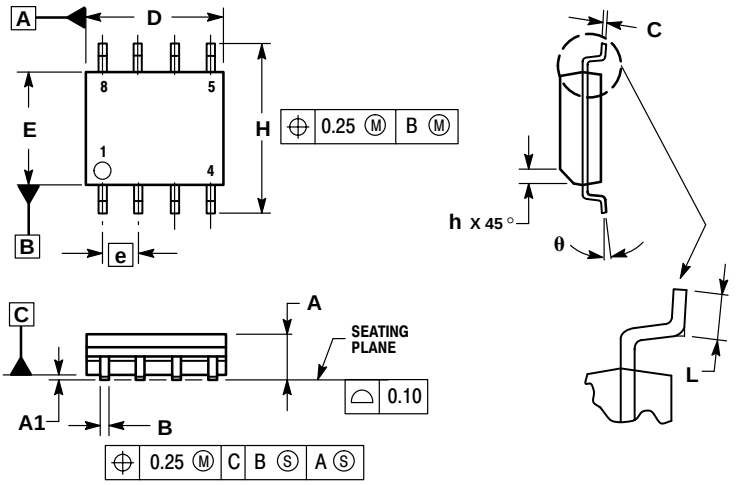
Figure 29. PCB Copper Layout

PARTS LIST

Qty	Reference	Part/Description	Vendor	Notes
3	C1, C3, C5	0.1 μF Ceramic Capacitor	Various	–
2	C2, C4	10 μF Ceramic Capacitor	Various	–
1	U1	MC33565	ON Semiconductor	–
1	Q1	MGSF1P02ELT	ON Semiconductor	P–Channel MOSFET

PACKAGE DIMENSIONS

SOIC–8
D SUFFIX
PLASTIC PACKAGE
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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