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MOTOROLA

MC33349

Product Preview

Lithium Battery Protection Circuit for One Cell Battery Packs

The MC33349 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of a one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, charge and discharge current limit detection, and a virtually zero current sleepmode state when the cell is discharged. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33349 is available in the SOT–23 6 lead surface mount package.

- Internally Trimmed Charge and Discharge Voltage Limits
- Charge and Discharge Current Limit Detection
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in a Low Profile Surface Mount Package

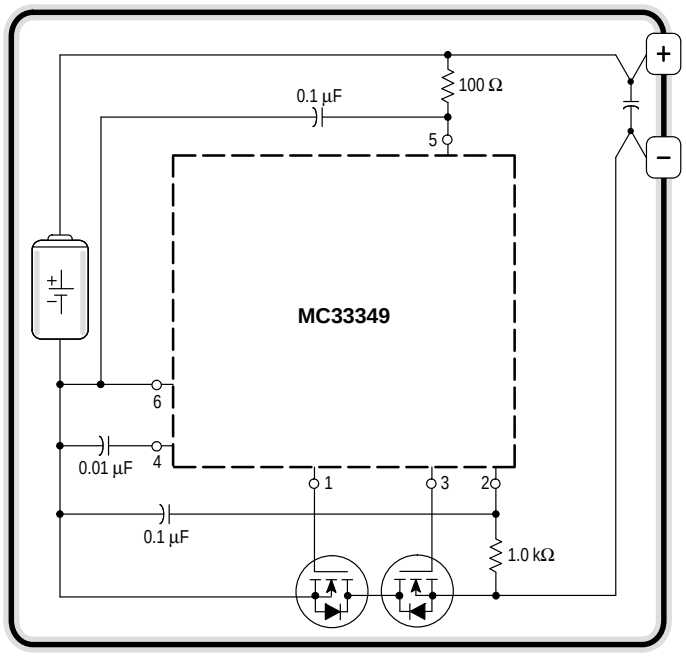
Ordering Information shown on following page.

LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE CELL SMART BATTERY PACKS

SEMICONDUCTOR TECHNICAL DATA

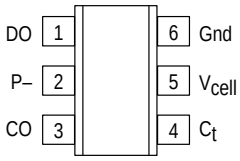
N SUFFIX
PLASTIC PACKAGE
CASE 1262
(SOT–23)

Typical One Cell Smart Battery Pack



This device contains 264 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Charge Overvoltage Threshold (V)	Charge Overvoltage Hysteresis (mV)	Discharge Undervoltage Threshold (V)	Current Limit Threshold (mV)	Operating Temperature Range	Package
MC33349N–1	4.2	200	2.3	150	T_A = –40 to 85°C	SOT–23
MC33349N–2	4.2			75		
MC33349N–3	4.25			150		
MC33349N–4	4.25			75		
MC33349N–5	4.3			150		
MC33349N–6	4.3			75		
MC33349N–7	4.35			150		
MC33349N–8	4.35			75		
MC33349N–9	4.65			150		
MC33349N–10	4.65			75		

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage	V_{IR}		V
Discharge Gate Drive Output (Pin 1) to Gnd (Pin 6)		5.0 to –1.0	
Charge Gate Drive Common/Current Limit (Pin 2) to V_{cell} (Pin 5)		1.0 to –18	
Charge Gate Drive Output (Pin 3) to V_{cell} (Pin 5)		1.0 to –18	
Overvoltage Delay Capacitor (Pin 4) to Gnd (Pin 6)		5.0 to –1.0	
Cell Voltage (Pin 5) to Gnd (Pin 6)		5.0 to –1.0	
Thermal Resistance, Junction–to–Air N Suffix, SOT–23 Plastic Package, Case 1262	$R_{\theta JA}$	TBD	°C/W
Operating Junction Temperature (Note 1)	T_J	–40 to 85	°C
Storage Temperature	T_{stg}	–55 to 125	°C

ELECTRICAL CHARACTERISTICS (C_t = 0.01 µF, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Cell Charging Cutoff (Pin 5 to Pin 6)					
Overvoltage Threshold, V_{Cell} Increasing	$V_{th(OV)}$				V
–1, –3 Suffix		–	4.35	–	
–2, –4 Suffix		–	4.25	–	
Overvoltage Hysteresis V_{Cell} Decreasing	V_H	–	200	–	mV
Cell Discharging Cutoff (Pin 5 to Pin 6)					
Undervoltage Threshold, V_{Cell} Decreasing	$V_{th(UV)}$				V
–1, –3 Suffix		–	2.30	–	
–2, –4 Suffix		–	2.28	–	
Input Bias Current During Cell Voltage Sample (Pin 5)	I_{IIB}	–	20	–	µA
Overvoltage Delay Time (V_{cell} = 4.5 V)	$t_{(ovd)}$	–	75	–	ms
Unervoltage Delay Time (V_{cell} = 2.1 V)	$t_{(uvd)}$	–	13	–	ms
Cell Voltage Sampling Period	$t_{(smpl)}$	–	2.0	–	ms
Cell Voltage Sampling Repitition Period	$t_{(rep)}$	–	26	–	ms
CURRENT SENSING					
Discharge/Charge Current Limit (Pin 2 to Pin 6)					
Discharge Threshold Voltage	$V_{th(dschg)}$				mV
–1, –2 Suffix		–	150	–	
–3, –4 Suffix		–	75	–	
Discharge Current Hysteresis	DCH	–	50	–	%
Charge Threshold Voltage	$V_{th(chg)}$				mV
–1. –2 Suffix		–	–150	–	
–3, –4 Suffix		–	–75	–	
Charge Current Hysteresis	CCH	–	25	–	%
Current Limit Delay Time (1.0 nF load @ CO & DO; to V_{DD}/2)					
Charge Gate Drive Output (Pin 3)	$t_{(ccld)}$	–	10	–	µs
Discharge Gate Drive Output (Pin 1)	$t_{(dcld)}$	–	2.0	–	µs
OUTPUTS					
Charge Gate Drive Output Low (Pin 3 to Pin 2 @ I_O = 50 µA)	V_{olc}	–	0.2	–	V
Charge Gate Drive Output High (Pin 5 to Pin 3 @ I_O = –50 µA)	V_{ohc}	–	0.1	–	V
Discharge Gate Drive Output Low (Pin 1 to Pin 6 @ I_O = 50 µA)	V_{old}	–	0.2	–	V
Discharge Gate Drive Output High (Pin 5 to Pin 1 @ I_O = –50 µA)	V_{ohd}	–	0.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{cell}				
Operating (V_{cell} = 3.9 V)		–	8.5	–	µA
Sleepmode (V_{cell} = 2.0 V)		–	4.0	–	nA
Minimum Operating Cell Voltage	V_{cell}	–	1.5	–	V

PIN FUNCTION DESCRIPTION

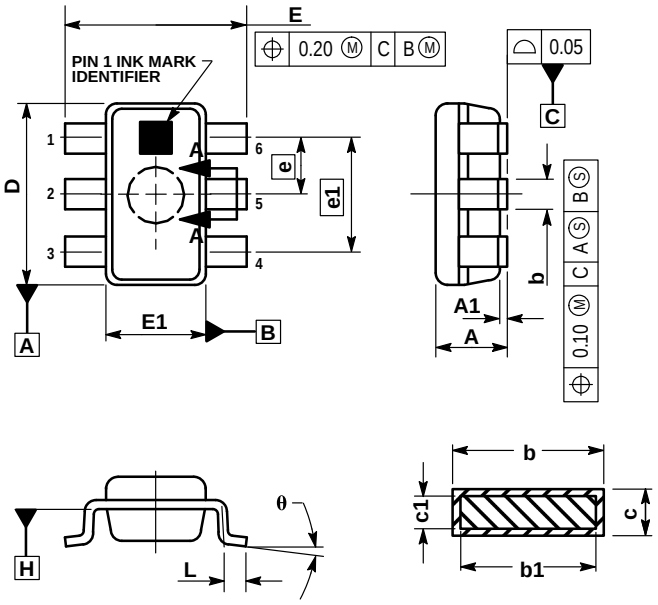
Pin	Symbol	Description
1	DO	This output connects to the gate of discharge MOSFET switch Q2 allowing it to enable or disable battery pack discharging.
2	P–	This is a multifunction pin that is used to monitor cell charge and discharge current and to provide a gate turn–off path for charge switch Q1. A current limit fault is set when the combined voltage drop of charge switch Q1 and discharge switch Q2 exceeds the discharge current limit threshold voltage, $V_{th(dschg)}$ above Pin 6 caused by a load; or charge current limit threshold voltage, $V_{th(chg)}$ below Pin 6 caused by a charger.
3	CO	This output connects to the gate of charge MOSFET switch Q1 allowing it to enable or disable battery pack charging.
4	C_t	An external capacitor connects between this pin and ground (Pin 6) to set the sample timer frequency and overvoltage delay time.
5	V_{cell}	This input connects to the positive terminal of the cell for voltage monitoring and provides operating bias for the integrated circuit. Internally, the Cell Voltage Sample Switch periodically applies this voltage to a resistor divider where it is compared by the Cell Voltage Detector to an internal reference.
6	Gnd	This is the ground pin of the IC.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs MOSFET Switches Charge Q1	Outputs MOSFET Switches Discharge Q2
CELL CHARGING/DISCHARGING			
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On
CELL CHARGING FAULT/RESET			
Charge Voltage Limit Fault: $V_{Pin\ 5} \geq V_{th(OV)}$ for two consecutive samples	Charge MOSFET Q1 is latched off and the cell is disconnected from the charging source. An internal current source pull–up is applied to divider resistors R1 and R2 creating a hysteresis voltage of V_H. The battery pack is available for discharging. Discharge current limit protection is disabled.	On to Off	On
Charge Voltage Limit Reset: $V_{Pin\ 5} < (V_{th(OV)} - V_H)$ for one sample, or $V_{Pin\ 2} > V_{th(dschg)}$	Charge MOSFET Q1 will turn on when the voltage across the cell falls sufficiently to overcome hysteresis voltage V_H, or when a load is applied to the battery pack.	Off to On	On
Charge Current Limit Fault: $V_{Pin\ 2} \leq (V_{Pin\ 6} + V_{th(chg)})$	Charge MOSFET Q1 is latched off and the cell is disconnected from the charger. Q1 will remain in the off state as long as $V_{Pin\ 6}$ exceeds $V_{Pin\ 2}$ by $\approx V_{th(chg)}$. The battery pack is available for discharging. Discharge current limit is disabled.	On to Off	On
Charge Current Limit Reset: $V_{Pin\ 6} - V_{Pin\ 2} < V_{th(chg)}$	The Sense Enable circuit will reset and turn on charge MOSFET Q1 when $V_{Pin\ 6}$ no longer exceeds $V_{Pin\ 2}$ by $\approx V_{th(chg)}$. This can be accomplished by either disconnecting the charger from the battery pack, or by connecting the battery pack to a load.	Off to On	On
CELL DISCHARGING FAULT/RESET			
Discharge Current Limit Fault: $V_{Pin\ 2} \geq (V_{Pin\ 6} + V_{th(dschg)})$	Discharge MOSFET Q2 is latched off and the cell is disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 2}$ exceeds $V_{Pin\ 6}$ by $\approx V_{th(dschg)}$. The battery pack is available for charging. Charge current limit protection is disabled.	On	On to Off
Discharge Current Limit Reset: $V_{Pin\ 2} - V_{Pin\ 6} < V_{th(dschg)}$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 2}$ no longer exceeds $V_{Pin\ 5}$ by $\approx V_{th(dschg)}$. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On
Discharge Voltage Limit Fault: $V_{Pin\ 5} \leq V_{th(UV)}$ for one sample	Discharge MOSFET Q2 is latched off, the cell is disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging. Charge current limit protection is disabled.	On	On to Off
Discharge Voltage Limit Reset: $V_{Pin\ 6} > (V_{Pin\ 2} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 6}$ exceeds $V_{Pin\ 2}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On
TEST MODE – PIN 4/PIN 5 SHORT			
Continuous Charge Voltage Limit Comparator $V_{Pin\ 4} = V_{Pin\ 5} = V_{cell} < V_{th(chg)}$ $V_{Pin\ 4} = V_{Pin\ 5} = V_{cell} > V_{th(chg)}$	This condition occurs if Pin 4 and Pin 5 are accidently shorted together or purposely connected for rapid Charge Voltgae Limit Testing. MOSFET Q1 On to Off is not delayed and no hysteresis is required for reset.	 On Off	 On On
FAULTY CELL			
Discharge Voltage Limit Fault: $V_{Pin\ 5} \leq 1.5\ V$	This condition can happen if the cell is defective (<1.5 V) or if a momentary discharge current causes the cell voltage to fall below $V_{th(UV)}$ before a sample is taken.	Off	Off

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 1262–01
(SOT–23)
ISSUE O



SECTION A–A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE FLASH OR PROTRUSIONS. FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.23 PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
b	0.35	0.50
b1	0.35	0.45
c	0.09	0.20
c1	0.09	0.15
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95	
e1	1.90	
L	0.25	0.55
θ	0 °	10 °

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