MOTOROLA

MC33347A

Product Preview

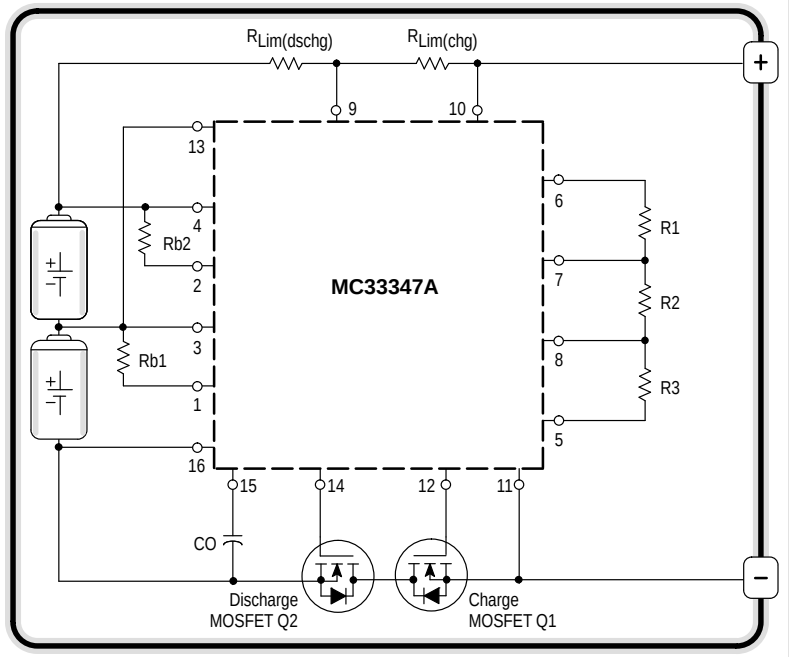
Lithium Battery Protection Circuit for One or Two Cell Battery Packs

The MC33347A is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one or two cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current, a delayed current shutdown, continuous cell voltage balancing with the choice of on–chip or external balancing resistors, and a virtually zero current sleepmode state when the cells are discharged.

Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33347A is available in standard and low profile 16 lead surface mount packages.

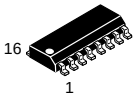
- Programmable for One or Two Cell Applications
- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Continuous Cell Voltage Balancing
- On–Chip and External (optional) Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Two Cell Smart Battery Pack

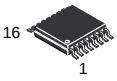


LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE OR TWO CELL SMART BATTERY PACKS

SEMICONDUCTOR TECHNICAL DATA

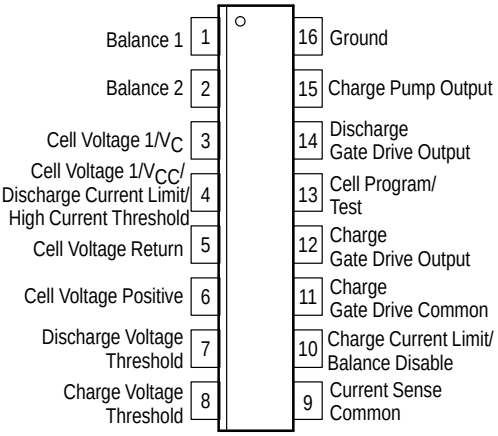


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33347AD	T_A = –40° to +85°C	SO–16
MC33347ADTB		TSSOP–16

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 16)	V_{IR}		V
Balance 1, 2 (Pins 1, 2)		10	
Cell 1 (Pin 3)		7.5	
Cell 2 (Pin 4)		10	
Cell Voltage Divider (Pins 5, 6, 7 and 8)		10	
Current Sense Common (Pin 9)		10	
Charge Current Limit (Pin 10)		10	
Charge Gate Drive Common (Pin 11)		±13	
Charge Gate Drive Output (Pin 12)		–14 to +12	
Cell Program/Test (Pin 13)		10	
Discharge Gate Drive Output (Pin 14)		10	
Charge Pump Output (Pin 15)		10	
External Cell Balancing Current (Pin 1, 2, Note 1)	I_{bal}	1.0	A
Cell Voltage Divider Current	I_{div}		mA
Source Current (Pin 4 to 6) or (Pin 3 to 6)		0.5	
Sink Current (Pin 3 to 5) or (Pin 16 to 5)		0.5	
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$		°C/W
DTB Suffix, TSSOP–16 Plastic Package, Case 948F		176	
D Suffix, SO–16 Plastic Package, Case 751B		145	
Operating Junction Temperature (Notes 1, 2 and 3)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Charge or Discharge Voltage Inputs (Pin 7 or 8 to Pin 5)					
Threshold Voltage	V_{th}				V
T_A = 25°C		–	1.230	–	
$T_A = T_{low}$ to T_{high}		–	–	–	
Input Bias Current	I_{IB}	–	20	–	nA
Input Hysteresis Source Current (Pin 8)	I_H	–	2.0	–	μA
Cell Charge or Discharge Programmable Input Voltage Range (Pin 7 or 8)	$V_{IR(pgm)}$	–	V_{th} to 7.5	–	V
Cell Selector Series Resistance					Ω
Cell Positive to Top of Divider (Pin 3 or 4 to Pin 6)	R_{S+}	–	50	–	
Cell Negative to Bottom of Divider (Pin 3 or 16 to Pin 5)	$R_{S–}$	–	50	–	
Cell Voltage Sampling Rate	$t_{(smpl)}$				s
$V_{Pin\ 9} < V_{Pin\ 4}$ + 10mV		–	1.0	–	
$V_{Pin\ 9} > V_{Pin\ 4}$ + 10mV		–	0.004	–	
Cell Program/ Test Input Threshold Voltage (Pin 13)	V_{th}	–	$V_{Cell\ 1}$/2.0	–	V
CELL VOLTAGE BALANCING					
Cell Voltage Balancing Accuracy (Note 4)	V_{bal}	–	1.0	–	Δ%
Internal Balancing Resistance (Pin 3, 4)	R_{bal}	–	100	–	Ω
Balancing MOSFET On Resistance (Pin 1, 2)	$R_{DS(on)}$	–	1.0	–	Ω

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33347A:
T_{low} = –25°C T_{high} = +85°C
4. Cell balancing is active when the percent change in voltage exceeds the typical limit specified. This parameter is measured by holding one cell at a fixed voltage while the other is varied so that balancing is activated. It is defined by:

$$\Delta\% = \left(\frac{\text{Variable Cell Voltage} - \text{Fixed Cell Voltage}}{\text{Fixed Cell Voltage}}\right) \times 100$$

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING					
Charge Current Limit (Pin 10 to Pin 9, T_A = 25°C)					
Threshold Voltage	$V_{th(chg)}$	–	18	–	mV
Input Bias Current	$I_{IB(chg)}$	–	200	–	nA
Delay	$I_{dly(chg)}$	–	3.0	–	ms
Discharge Current Limit (Pin 4 to Pin 9, T_A = 25°C)					
Threshold Voltage	$V_{th(dschg)}$	–	70	–	mV
Input Bias Current	$I_{IB(dschg)}$	–	200	–	nA
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 15, $R_L \geq 10^{10}\ \Omega$)	V_O	–	9.2	–	V
TOTAL DEVICE					
Average Cell Current (T_A = 25°C, Battery Pack Unloaded and without Current Limit Fault)	I_{CC}				μA
Operating with Soft Short ($V_{Pin\ 4} - V_{Pin\ 9} > 10mV$)		–	19	–	
Operating (V_{CC} = 8.0 V)		–	12.5	–	
Sleepmode (V_{CC} = 5.0 V)		–	0.015	–	
Minimum Operating Cell Voltage	V_{CC}				V
Programmed for Two Cell Operation					
Cell 1 Voltage		–	1.5	–	
Cell 2 Voltage		–	0	–	
Programmed for One Cell Operation					
Cell 1 Voltage		–	1.5	–	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33347A:
T_{low} = –25°C T_{high} = +85°C
4. Cell balancing is active when the percent change in voltage exceeds the typical limit specified. This parameter is measured by holding one cell at a fixed voltage while the other is varied so that balancing is activated. It is defined by:

$$\Delta\% = \left(\frac{\text{Variable Cell Voltage} - \text{Fixed Cell Voltage}}{\text{Fixed Cell Voltage}}\right) \times 100$$

PIN FUNCTION DESCRIPTION

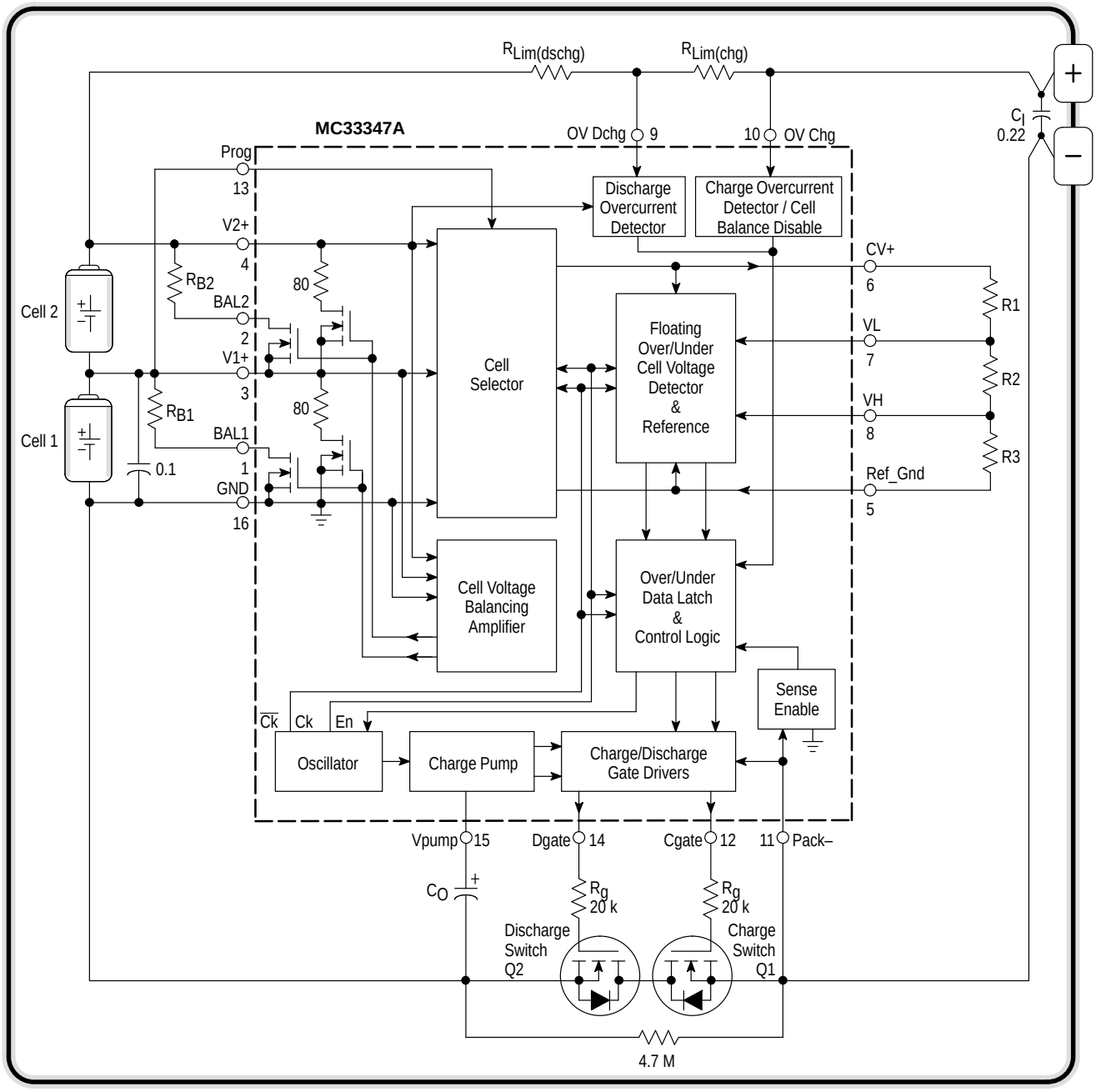
Pin	Pin Name	Function	Description
1	BAL1	Balance 1	This is the drain connection to an internal MOSFET. An external resistor is placed from this pin to the positive terminal of Cell 1 for increased cell balancing capability. This allows most of the additional power to be dissipated off–chip.
2	BAL2	Balance 2	This is the drain connection to an internal MOSFET. An external resistor is placed from this pin to the positive terminal of Cell 2 for increased cell balancing capability. This allows most of the additional power to be dissipated off–chip.
3	V1+	Cell Voltage 1/V_C	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2. This pin also provides logic biasing and a discharge path for the internal balancing of Cell 1.
4	V2+	Cell Voltage 2 /V_{CC}/Discharge Current Limit/ High Current Threshold	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and to provide positive supply voltage for the protection IC. This pin is also used to monitor the voltage drop across the discharge current limit resistor to detect a discharge current or a high current threshold to trigger fast sampling. It also provides a discharge path for the internal balancing of Cell 2.
5	Ref_Gnd	Cell Voltage Return	The bottom side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the negative terminal of the cell that is to be monitored.
6	CV+	Cell Voltage Positive	The top side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the positive terminal of the cell that is to be monitored.
7	VL	Discharge Voltage Threshold	The upper tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has fallen below the programmed level for three consecutive samples, discharge switch Q2 is disabled, and the protection circuit enters into a low current sleepmode state. This prevents further discharging of the battery pack.
8	VH	Charge Voltage Threshold	The lower tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has risen above the programmed level, charge switch Q1 is disabled, preventing further charging of the battery pack. A 2.0 μA current source pull–up is internally applied to this pin creating input hysteresis.
9	OV Dchg	Current Sense Common	This pin is a common point that is used to monitor the voltage drop across the charge and discharge current limit resistors.
10	OV Chg	Charge Current Limit/Cell Balance Disable	This pin is used to monitor the voltage drop across the charge current limit resistor or if connected to Pin 16, prevents cell balancing from occuring.
11	Pack–	Charge Gate Drive Common	This pin provides a gate turn–off path for charge switch Q1. The charge switch source and the battery pack negative terminal connect to this point.
12	Cgate	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
13	Prog	Cell Program /Test	This is a multifunction input that is used to program the number of cells and to facilitate circuit testing. This input is connected to Pin 3 for two cell operation, and to Pin 16 for one cell operation.
14	Dgate	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
15	Vpump	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.
16	GND	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs			
		MOSFET Switches		Function	
		Charge Q1	Discharge Q2	Charge Pump	Cell Balancing (See Note)
CELL CHARGING/DISCHARGING					
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active	Active
CELL CHARGING FAULT/RESET					
Charge Current Limit Fault: $V_{Pin\ 10} \geq (V_{Pin\ 9} + 18\ mV)$ for 3.0 ms	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. Q1 will remain in the off state as long as $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Current Limit Reset: $V_{Pin\ 16} - V_{Pin\ 11} < 2.0\ V$	The Sense Enable circuit will reset and turn on charge MOSFET Q1 when $V_{Pin\ 16}$ no longer exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the charger from the battery pack, or by connecting a load to the battery pack.	Off to On	On	Active	Active
Charge Voltage Limit Fault: $V_{Pin\ 8} \geq 1.23\ V$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal current source pull–up of 2.0 μA is applied to Pin 8 creating an input hysteresis voltage of V_H with divider resistors R1 and R2. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Voltage Limit Reset: $V_{Pin\ 8} < 1.23\ V$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across each cell falls sufficiently to overcome the input hysteresis voltage. This can be accomplished by applying a load to the battery pack.	Off to On	On	Active	Active
CELL DISCHARGING FAULT/RESET					
Discharge Current Limit Fault: $V_{Pin\ 4} \leq (V_{Pin\ 9} - 50\ mV)$ for 3.0 ms	Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 11}$ exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active	Active
Discharge Current Limit Reset: $V_{Pin\ 11} - V_{Pin\ 16} < 2.0\ V$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 11}$ no longer exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active	Active
Discharge Voltage Limit Fault: $V_{Pin\ 7} \leq 1.23\ V$ for three consecutive 1.0 s samples	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 16} > (V_{Pin\ 11} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active	Active
FAULTY CELL (ONE CELL OVERVOLTAGE, ONE CELL UNDERVOLTAGE)					
Simultaneous Charge and Discharge Voltage Limit Faults: $V_{Pin\ 8} \geq 1.23\ V$ for 1 cell and $V_{Pin\ 7} \leq 1.23\ V$ for three consecutive 1.0 s samples	This condition can happen if there is a defective cell in the battery pack such as one of the cells is shorted. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty (<1.5 V), the protection circuit logic will not function and the battery pack cannot be charged.	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty

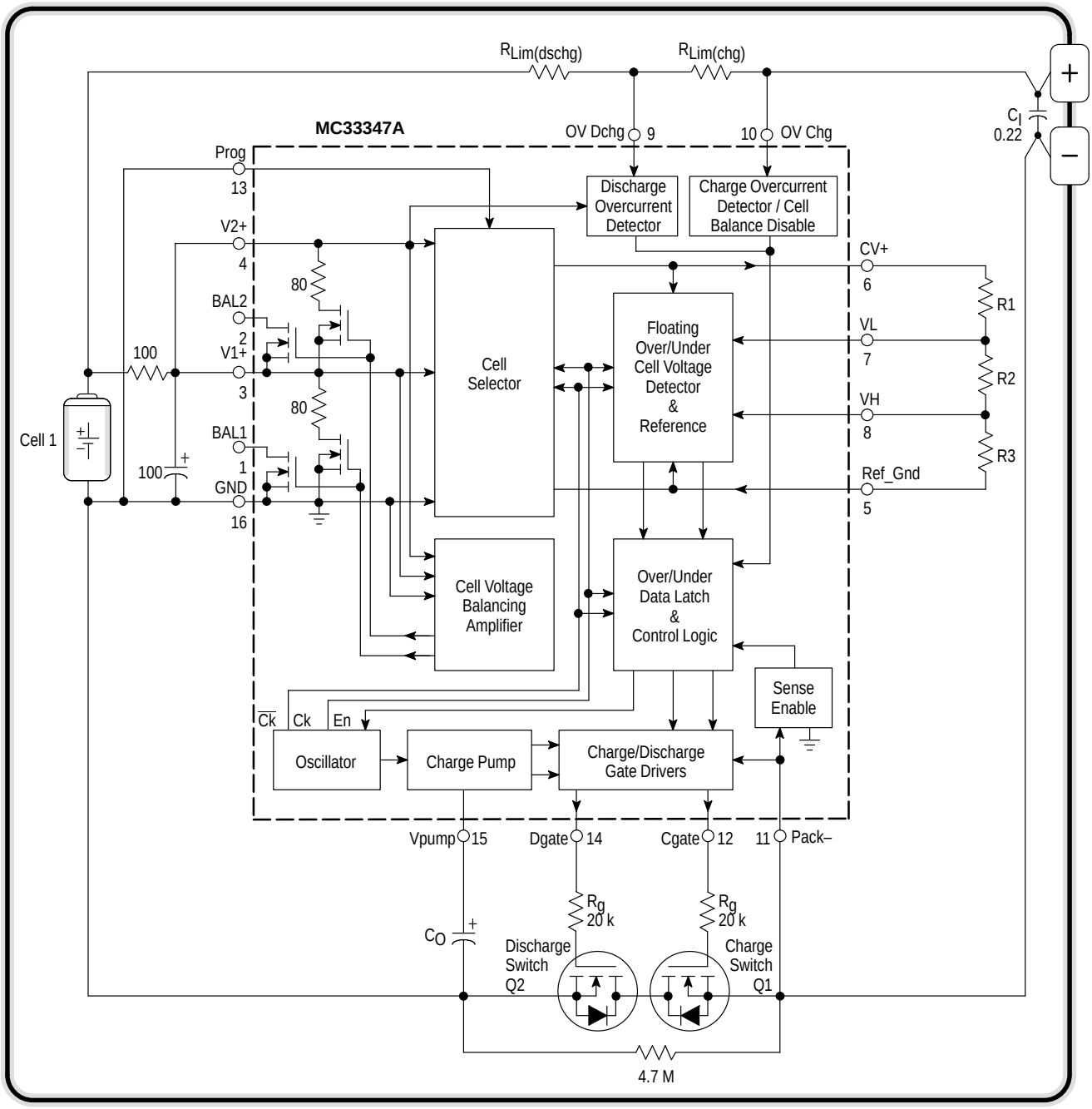
NOTE: Cell balancing is not active when programmed for one cell operation.

Figure 1. Two Cell Smart Battery Pack



Components C_I and R_g are mandatory. Refer to the Battery Pack Application text. The 100 nF capacitor that connects across Cell 1 provides high frequency bypassing of the V_C pin which powers the internal logic. This capacitor is desireable in applications that have high load current spikes when used with high impedance type cells.

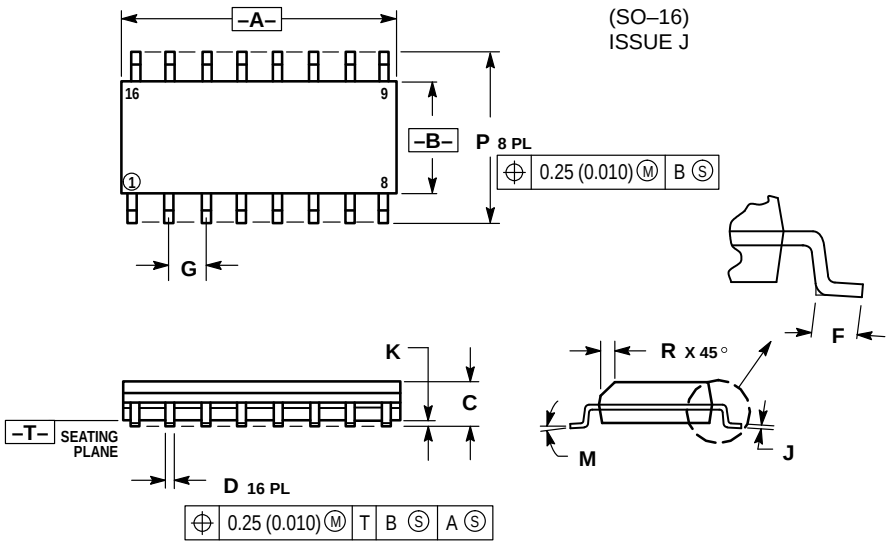
Figure 2. One Cell Smart Battery Pack



Components C_I and R_g are mandatory. Refer to the Battery Pack Application text. In order to guarantee proper discharge current limit operation when the battery pack output is shorted, power must be made available to the MC33347. An artifical power source with a 10 ms time constant is required, and is provided by the 100 Ω resistor and 100 µF capacitor that connects to the V_{CC} and V_C inputs. These components are only required in single cell battery pack applications.

OUTLINE DIMENSIONS

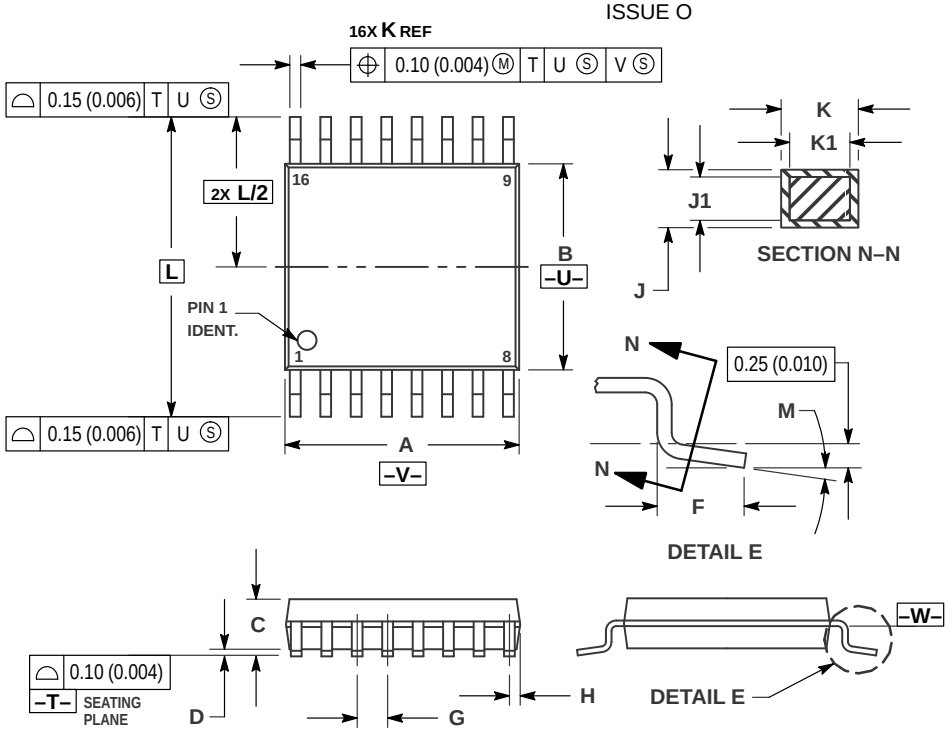
D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DTB SUFFIX
PLASTIC PACKAGE
CASE 948F–01
(TSSOP–16)
ISSUE O



NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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