MC33263

Ultra Low Noise 150 mA Low Dropout Voltage Regulator with ON/OFF Control

Housed in a SOT23–L package, the MC33263 delivers up to 150 mA where it exhibits a typical 180 mV dropout. With an incredible noise level of 25 μVRMS (over 100 Hz to 100 kHz, with a 10 nF bypass capacitor), the MC33263 represents the ideal choice for sensitive circuits, especially in portable applications where noise performance and space are premium. The MC33263 also excels in response time and reacts in less than 25 μs when receiving an OFF to ON signal (with no bypass capacitor).

Thanks to a novel concept, the MC33263 accepts output capacitors without any restrictions regarding their Equivalent Series Resistance (ESR) thus offering an obvious versatility for immediate implementation.

With a typical DC ripple rejection better than –90 dB (–70 dB @ 1 kHz), it naturally shields the downstream electronics against choppy power lines.

Additionally, thermal shutdown and short–circuit protection provide the final product with a high degree of ruggedness.

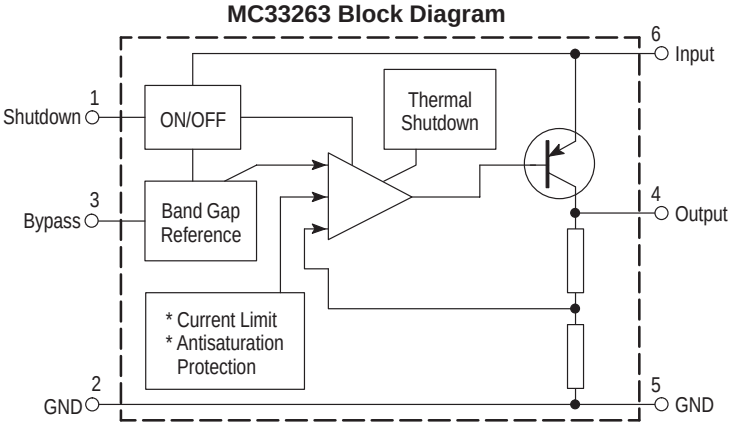
Features:

- Very Low Quiescent Current 170 μA (ON, no load), 100 nA (OFF, no load)
- Very Low Dropout Voltage, typical value is 137 mV at an output current of 100 mA
- Very Low Noise with external bypass capacitor (10 nF), typically 25 μVrms over 100 Hz to 100 kHz
- Internal Thermal Shutdown
- Extremely Tight Line Regulation typically –90 dB
- Ripple Rejection –70 dB @ 1 kHz
- Line Transient Response: 1 mV for ΔV_{in} = 3 V
- Extremely Tight Load Regulation, typically 20 mV at ΔI_{out} = 150 mA
- Multiple Output Voltages Available
- Logic Level ON/OFF Control (TTL–CMOS Compatible)
- ESR can vary from 0 to 3Ω
- Functionally and Pin Compatible with TK112xxA/B Series

Applications:

- All Portable Systems, Battery Powered Systems, Cellular Telephones, Radio Control Systems, Toys and Low Voltage Systems

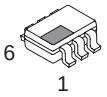
MC33263 Block Diagram



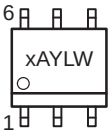
ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS

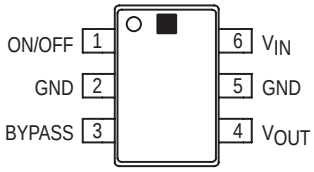


SOT–23L
NW SUFFIX
CASE 318J



x = Voltage Option Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



(Top View)

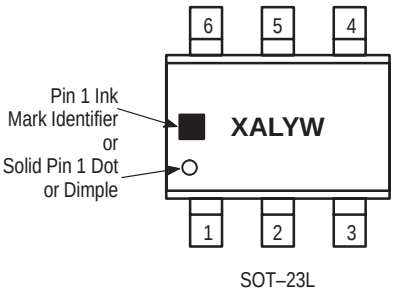
ORDERING INFORMATION

Device	Version	Shipping
MC33263NW–28R2	2.8 V	2500 Tape & Reel
MC33263NW–30R2	3.0 V	2500 Tape & Reel
MC33263NW–32R2	3.2 V	2500 Tape & Reel
MC33263NW–33R2	3.3 V	2500 Tape & Reel
MC33263NW–38R2	3.8 V	2500 Tape & Reel
MC33263NW–40R2	4.0 V	2500 Tape & Reel
MC33263NW–47R2	4.75 V	2500 Tape & Reel
MC33263NW–50R2	5.0 V	2500 Tape & Reel

All Devices Available in SOT–23L 6 Lead Package

DEVICE MARKING

XALYW	Marking	Version
1st Digit	A	2.8 V
	B	3.0 V
	C	3.2 V
	D	3.3 V
	E	3.8 V
	F	4.0 V
	G	4.75 V
	H	5.0 V
2nd Digit	A	Location Code
3rd Digit	L	Wafer Lot Traceability
4th/5th Digits	YW	Date Code



SOT–23L

MAXIMUM RATINGS

Rating	Symbol	Pin #	Value	Unit
Power Supply Voltage	V_{in}	6	12	V
Power Dissipation and Thermal Resistance Maximum Power Dissipation NW Suffix, Plastic Package Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$		 Internally Limited 210 	 W °C/W °C/W
Operating Ambient Temperature Maximum Junction Temperature	T_A T_{Jmax}		–40 to +85 150	°C °C
Storage Temperature Range	T_{stg}		–60 to +150	°C

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 150°C)

Characteristics	Symbol	Pin #	Min	Typ	Max	Unit
CONTROL ELECTRICAL CHARACTERISTICS						
Input Voltage Range	$V_{ON/OFF}$	1	0	–	V_{in}	V
ON/OFF Input Current (All versions) $V_{ON/OFF}$ = 2.4 V	$I_{ON/OFF}$	1	 –	 2.5	 –	μA
ON/OFF Input Voltages (All versions) Logic “0”, i.e. OFF State Logic “1”, i.e. ON State	$V_{ON/OFF}$	1	 – 2.2	 – –	 0.3 –	V
CURRENTS PARAMETERS						
Current Consumption in OFF State (All versions) OFF Mode Current: V_{in} = V_{out} + 1.0 V, I_{out} = 0 mA	IQ_{OFF}		–	0.1	2.0	μA
Current Consumption in ON State (All versions) ON Mode Sat Current: V_{in} = V_{out} + 1.0 V, I_{out} = 0 mA	IQ_{ON}		–	170	200	μA
Current Consumption in Saturation ON State (All versions) ON Mode Sat Current: V_{in} = V_{out} – 0.5 V, I_{out} = 0 mA	IQ_{SAT}		–	900	1400	μA
Current Limit V_{in} = V_{out} + 1.0 V, (All versions) Output Short–circuited (Note 1.)	I_{MAX}		175	210	–	mA

1. I_{out} (Output Current) is the measured current when the output voltage drops below 0.3 V with respect to V_{out} at I_{out} = 30 mA.

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 150°C)

Characteristics	Symbol	Pin #	Min	Typ	Max	Unit
V_{in} = V_{out} + 1.0 V, T_A = 25°C, 1.0 mA < I_{out} < 150 mA	V_{out}	4				V
2.8 Suffix			2.74	2.8	2.86	
3.0 Suffix			2.94	3.0	3.06	
3.2 Suffix			3.13	3.2	3.27	
3.3 Suffix			3.23	3.3	3.37	
3.8 Suffix			3.72	3.8	3.88	
4.0 Suffix			3.92	4.0	4.08	
4.75 Suffix			4.66	4.75	4.85	
5.0 Suffix			4.90	5.0	5.1	
V_{in} = V_{out} + 1.0 V, –40°C < T_A < 80°C, 1.0 mA < I_{out} < 150 mA	V_{out}	4				V
2.8 Suffix			2.7	2.8	2.9	
3.0 Suffix			2.9	3.0	3.1	
3.2 Suffix			3.09	3.2	3.31	
3.3 Suffix			3.18	3.3	3.42	
3.8 Suffix			3.67	3.8	3.93	
4.0 Suffix			3.86	4.0	4.14	
4.75 Suffix			4.58	4.75	4.92	
5.0 Suffix			4.83	5.0	5.17	
LINE AND LOAD REGULATION, DROPOUT VOLTAGES						
Line Regulation (All versions)	Reg_{line}	4/6				mV
V_{out} + 1.0 V < V_{in} < 12 V, I_{out} = 60 mA			–	2.0	10	
Load Regulation (All versions) V_{in} = V_{out} + 1.0 V	Reg_{load}	1				mV
I_{out} = 1.0 to 60 mA			–	8.0	25	
I_{out} = 1.0 to 100 mA			–	15	35	
I_{out} = 1.0 to 150 mA			–	20	45	
Dropout Voltage (All versions)	V_{in} – V_{out}	4, 6				mV
I_{out} = 10 mA			–	30	90	
I_{out} = 100 mA			–	137	230	
I_{out} = 150 mA			–	180	260	
DYNAMIC PARAMETERS						
Ripple Rejection (All versions)		4, 6				dB
V_{in} = V_{out} + 1.0 V, V_{pp} = 1.0 V, f = 1.0 kHz, I_{out} = 60 mA			60	70	–	
Line Transient Response		4, 6				mV
V_{in} = V_{out} + 1.0 V to V_{out} + 4.0 V, I_{out} = 60 mA, $d(V_{in})/dt$ = 15 mV/μs			–	1.0	–	
Output Noise Voltage (All versions)	V_{RMS}	4, 6				μVrms
C_{out} = 1.0 μF, I_{out} = 60 mA, f = 100 Hz to 100 kHz						
C_{bypass} = 10 nF			–	25	–	
C_{bypass} = 1.0 nF			–	40	–	
C_{bypass} = 0 nF			–	65	–	
Output Noise Density	V_N	4				nV/ $\sqrt{Hz}$
C_{out} = 1.0 μF, I_{out} = 60 mA, f = 1.0 kHz			–	230	–	
Output Rise Time (All versions)	t_r	4				
C_{out} = 1.0 μF, I_{out} = 30 mA, $V_{ON/OFF}$ = 0 to 2.4 V, 1% of ON/OFF Signal to 99% of Nominal Output Voltage						
Without Bypass Capacitor			–	40	–	μs
With C_{bypass} = 10 nF			–	1.1	–	ms
THERMAL SHUTDOWN						
Thermal Shutdown (All versions)			–	150	–	°C

DEFINITIONS

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage – The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage – The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.

Maximum Power Dissipation – The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current – Current which is used to operate the regulator chip and is not delivered to the load.

Line Regulation – The change in input voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Line Transient Response – Typical over– and undershoot response when input voltage is excited with a given slope.

Thermal Protection – Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically 150°C, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

Maximum Package Power Dissipation – The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. 125°C. The junction temperature is rising while the difference between the input power (V_{CC} X I_{CC}) and the output power (V_{out} X I_{out}) is increasing.

Depending on ambient temperature, it is possible to calculate the maximum power dissipation, maximum load current or maximum input voltage (see Application Hints: Protection).

The maximum power dissipation supported by the device is a lot increased when using appropriate application design. Mounting pad configuration on the PCB, the board material and also the ambient temperature are affected the rate of temperature rise. It means that when the I_C has good thermal conductivity through PCB, the junction temperature will be “low” even if the power dissipation is great.

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature (150°C for MC33263) and ambient temperature.

APPLICATION HINTS

Input Decoupling – As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A 1 μF capacitor either ceramic or tantalum is recommended and should be connected close to the MC33263 package. Higher values will correspondingly improve the overall line transient response.

Output Decoupling – Thanks to a novel concept, the MC33263 is a stable component and does not require any Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3Ω can thus safely be used. The minimum decoupling value is 1 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

Noise Performances – Unlike other LDOs, the MC33263 is a true low–noise regulator. With a 10 nF bypass capacitor, it typically reaches the incredible level of 25 μVRMS overall noise between 100 Hz and 100 kHz. To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics as well as noise dependency versus bypass capacitor.

The bypass capacitor impacts the start–up phase of the MC33263 as depicted by the data–sheet curves. A typical 1 ms settling time is achieved with a 10 nF bypass capacitor. However, thanks to its low–noise architecture, the MC33263 can operate without bypass and thus offers a typical 20 μs start–up phase. In that case, the typical output noise stays lower than 65 μVRMS between 100 Hz – 100 kHz.

Protections – The MC33263 hosts several protections, conferring natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a minimum of 175 mA while temperature shutdown occurs if the die heats up beyond 150°C. These value lets you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$P_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

If T_{Jmax} is internally limited to 150°C, then the MC33263 can dissipate up to 595 mW @ 25°C.

The power dissipated by the MC33263 can be calculated from the following formula:

$$Ptot = \langle V_{in} \cdot I_{gnd}(I_{out}) \rangle + \langle V_{in} - V_{out} \rangle \cdot I_{out}$$

or

$$Vin_{max} = \frac{Ptot + V_{out} \cdot I_{out}}{I_{gnd} + I_{out}}$$

If a 150 mA output current is needed, the ground current is extracted from the data–sheet curves: 6.5 mA @ 150 mA. For a MC33263NW28R2 (2.8 V), the maximum input voltage will then be 6.48 V, a rather comfortable margin.

Typical Application – The following figure portraits the typical application for the MC33263 where both input/output decoupling capacitors appear.

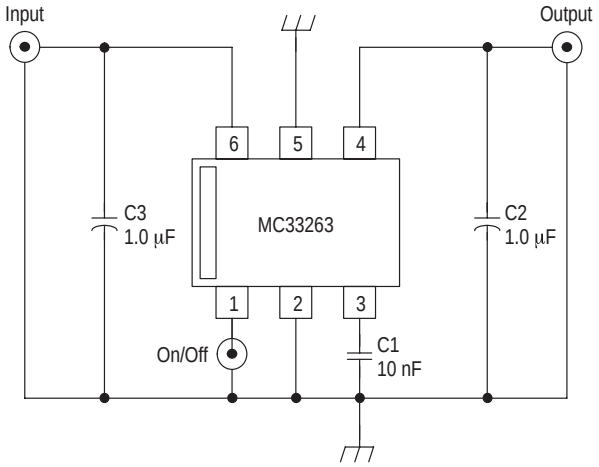


Figure 1. A Typical MC33263 Application with Recommended Capacitor Values

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. The following figure gives an example of a layout where stray inductances/capacitances are minimized.

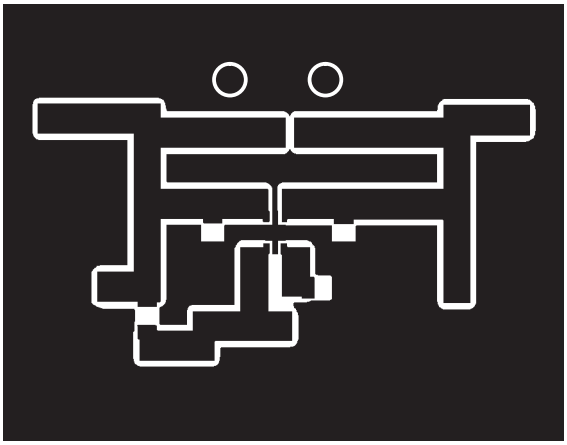


Figure 2. Printed Circuit Board

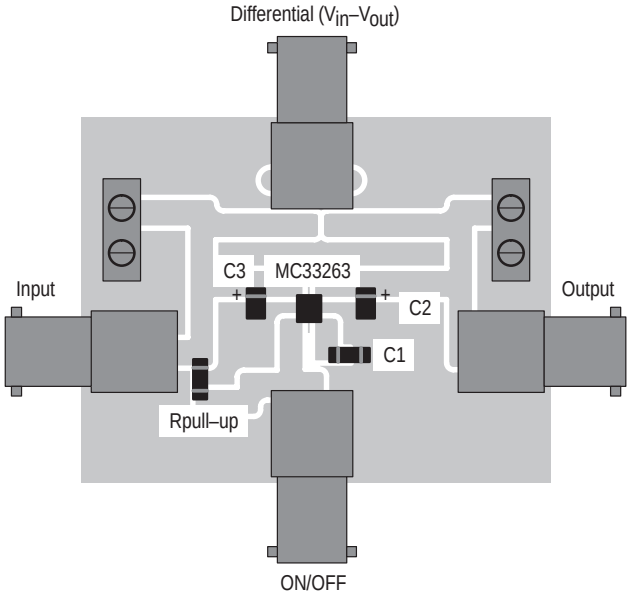


Figure 3. Copper Side Component Layout

This layout is the basis for an MC33263 performance evaluation board where the BNC connectors give the user an easy and quick evaluation mean.

MC33263 Wake–up Improvement – In portable applications, an immediate response to an enable signal is vital. If noise is not of concern, the MC33263 without a bypass capacitor settles in nearly 20 μs and typically delivers 65 μVRMS between 100 Hz and 100 kHz.

In ultra low–noise systems, the designer needs a 10 nF bypass capacitor to decrease the noise down to 25 μVRMS between 100 Hz and 100 kHz. With the adjunction of the 10 nF capacitor, the wake–up time expands up to 1 ms as shown on the data–sheet curves. If an immediate response is wanted, following figure's circuit gives a solution to charge the bypass capacitor with the enable signal without degrading the noise response of the MC33263.

At power–on, C4 is discharged. When the control logic sends its wake–up signal by going to a high level, the PNP base is momentarily tight to ground. The PNP switch closes and immediately charges the bypass capacitor C1 toward its operating value. After a few μs, the PNP opens and becomes totally transparent to the regulator.

This circuit improves the response time of the regulator which drops from 1 ms down to 30 μs. The value of C4 needs to be tweaked in order to avoid any bypass capacitor overload during the wake–up transient.

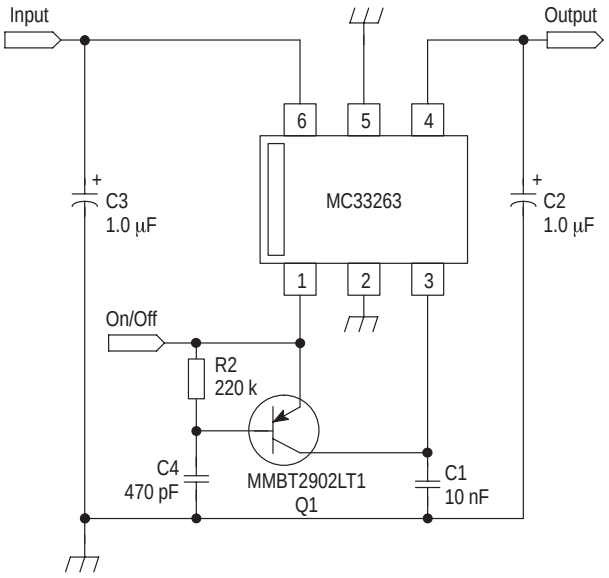


Figure 4. A PNP Transistor Drives the Bypass Pin when Enable Goes High

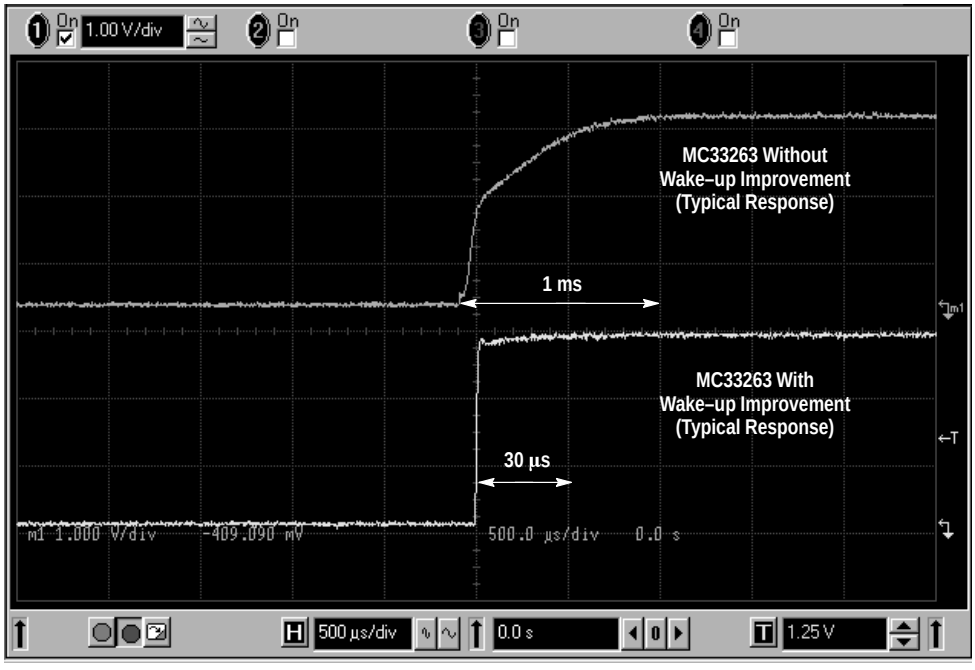


Figure 5. MC33263 Wake–up Improvement with Small PNP Transistor

The PNP being wired upon the bypass pin, it shall not degrade the noise response of the MC33263. Figure 6 confirms the good behavior of the integrated circuit in this area which reaches a typical noise level of 26 μVRMS (100 Hz to 100 kHz) at I_{out} = 60 mA.

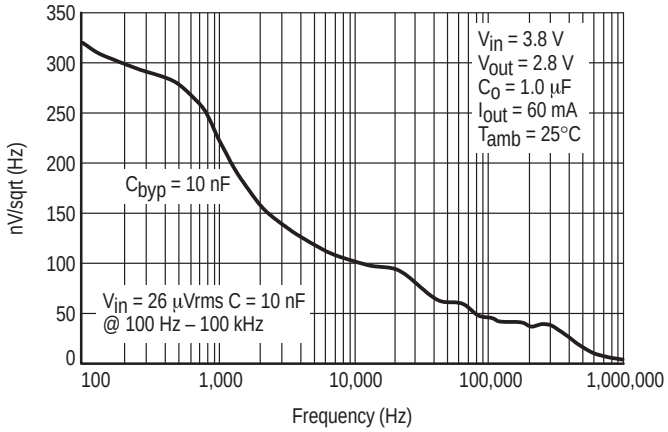


Figure 6. Noise Density of the MC33263 with a 10 nF Bypass Capacitor and a Wake–up Improvement Network

TYPICAL PERFORMANCE CHARACTERISTICS

Ground Current Performances

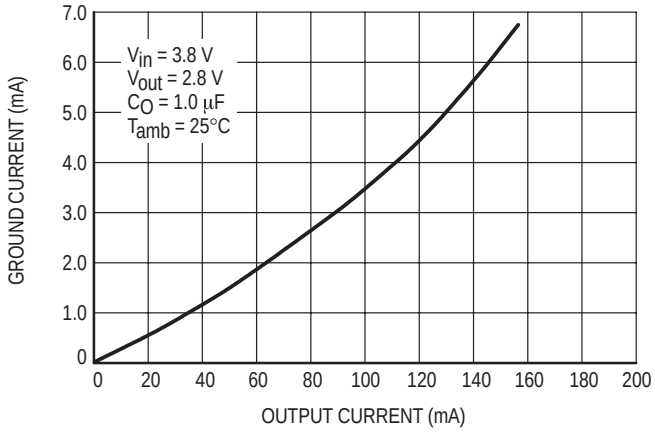


Figure 7. Ground Current versus Output Current

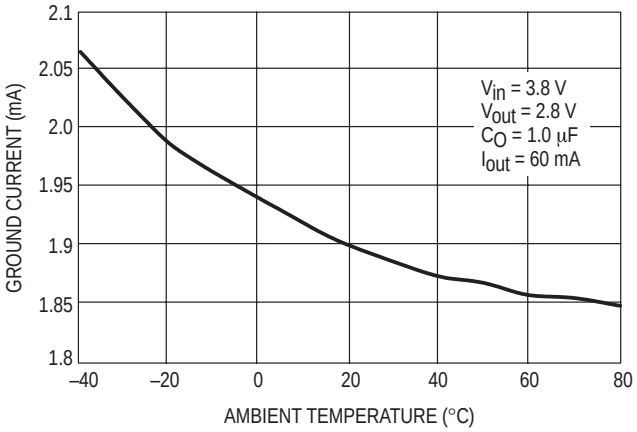


Figure 8. Ground Current versus Ambient Temperature

Line Transient Response and Output Voltage

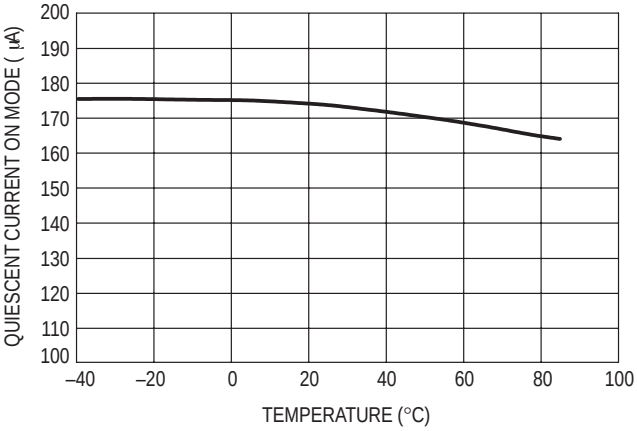


Figure 9. Quiescent Current versus Temperature

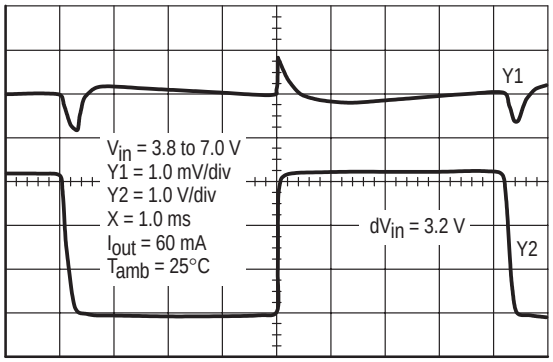
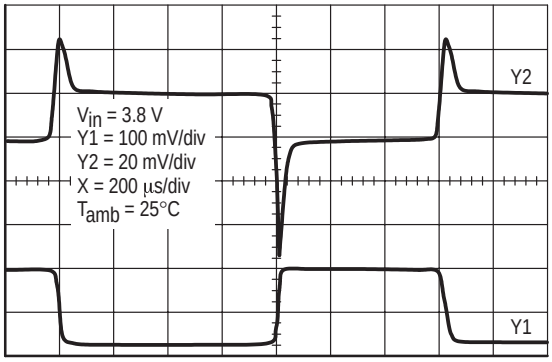


Figure 10. Line Transient Response

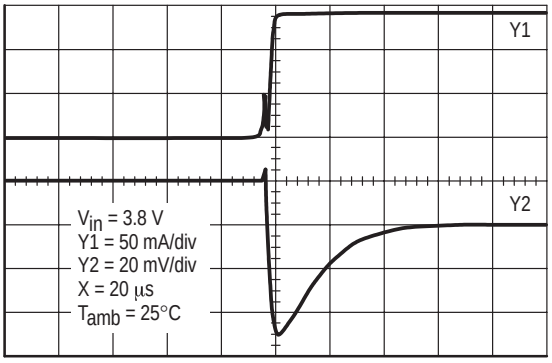
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response versus Load Current Slope



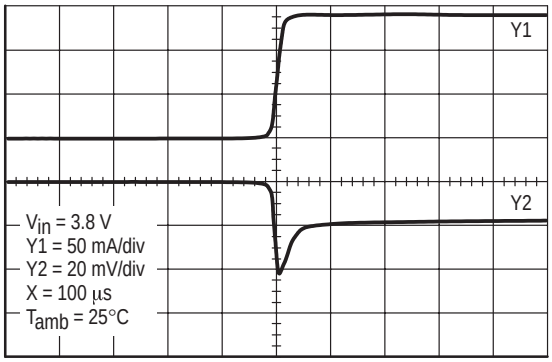
Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 11. I_{out} = 3.0 mA to 150 mA



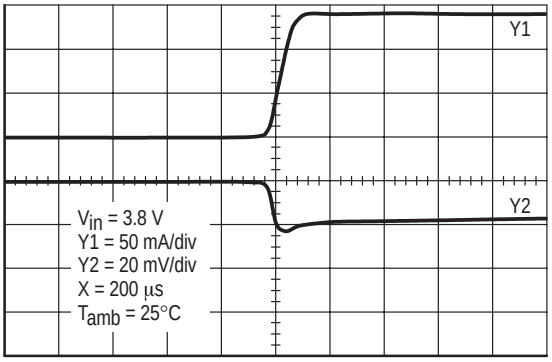
Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 12. I_{Slope} = 100 mA/μs (Large Scale) I_{out} = 3.0 mA to 150 mA



Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 13. I_{Slope} = 6.0 mA/μs (Large Scale) I_{out} = 3.0 mA to 150 mA



Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 14. I_{Slope} = 2.0 mA/μs (Large Scale) I_{out} = 3.0 mA to 150 mA

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Performances

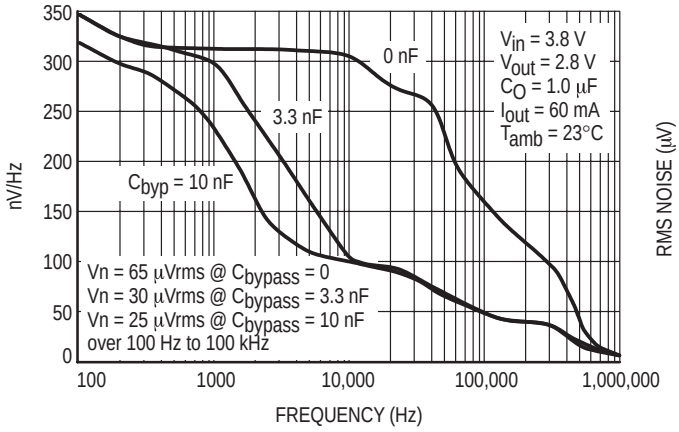


Figure 15. Noise Density versus Bypass Capacitor

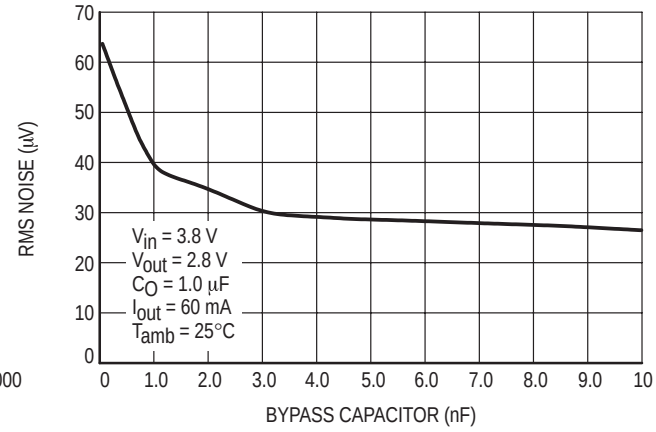


Figure 16. RMS Noise versus Bypass Capacitor (100 Hz – 100 kHz)

Settling Time Performances

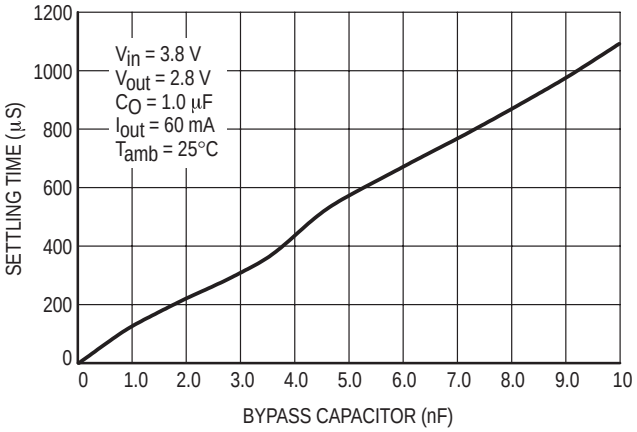


Figure 17. Output Voltage Settling Time versus Bypass Capacitor

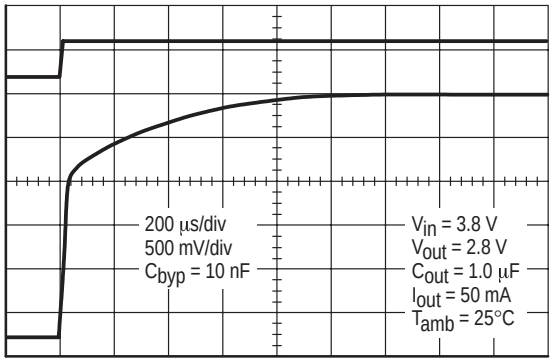


Figure 18. Output Voltage Settling Shape C_{bypass} = 10 nF

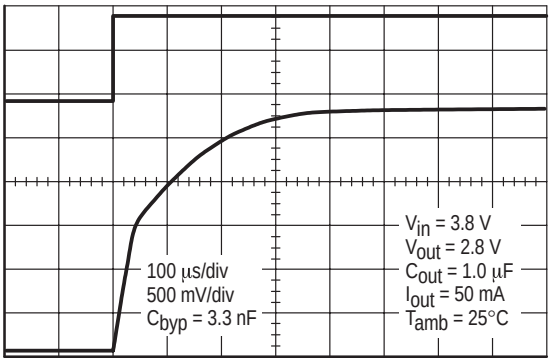


Figure 19. Output Voltage Settling Shape C_{bypass} = 3.3 nF

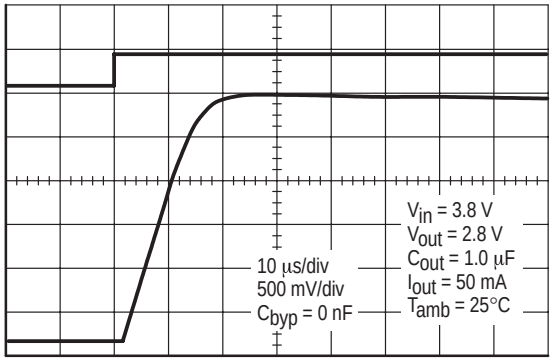


Figure 20. Output Voltage Settling Shape without Bypass Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Voltage

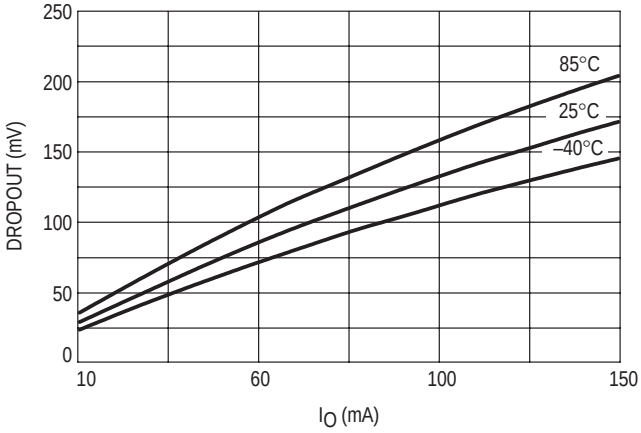


Figure 21. Dropout Voltage versus I_{out}

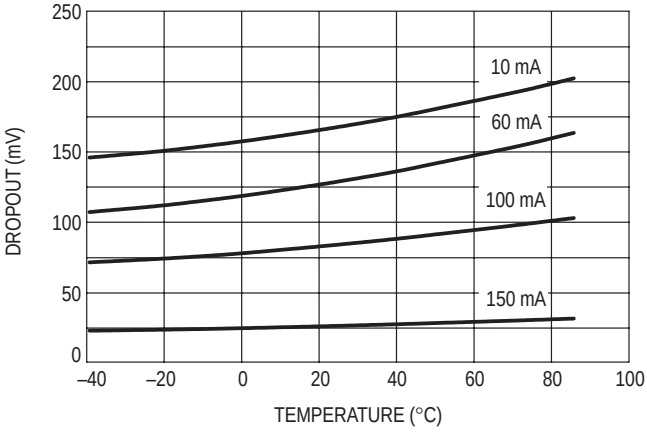


Figure 22. Dropout Voltage versus Temperature

Output Voltage

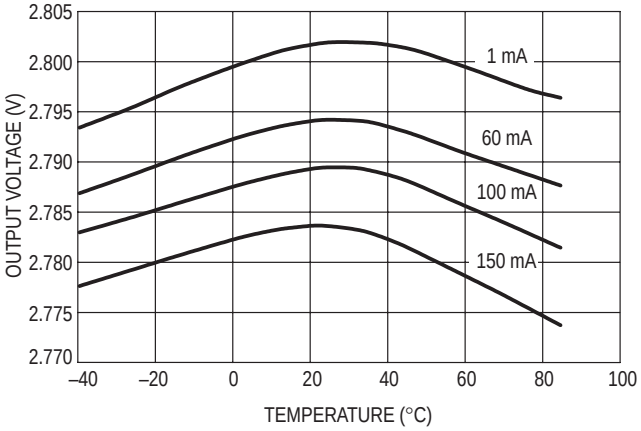


Figure 23. Output Voltage versus Temperature

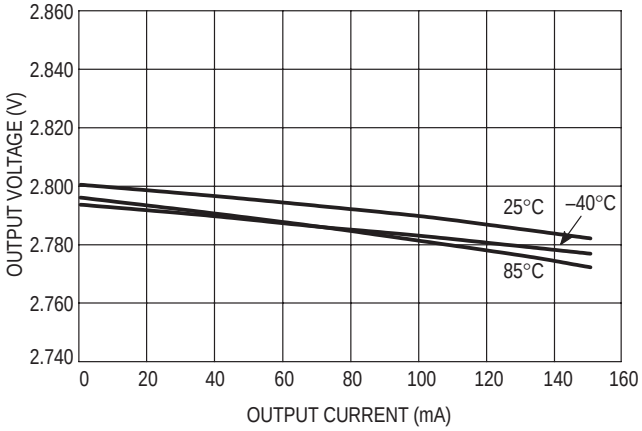


Figure 24. Output Voltage versus I_{out}

Ripple Rejection Performances

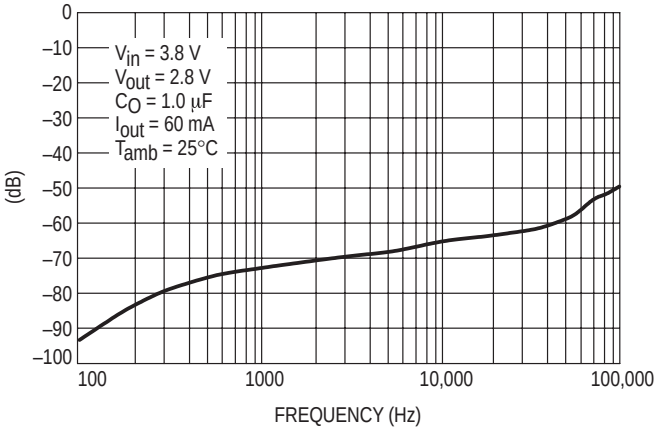


Figure 25. Ripple Rejection versus Frequency with 10 nF Bypass Capacitor

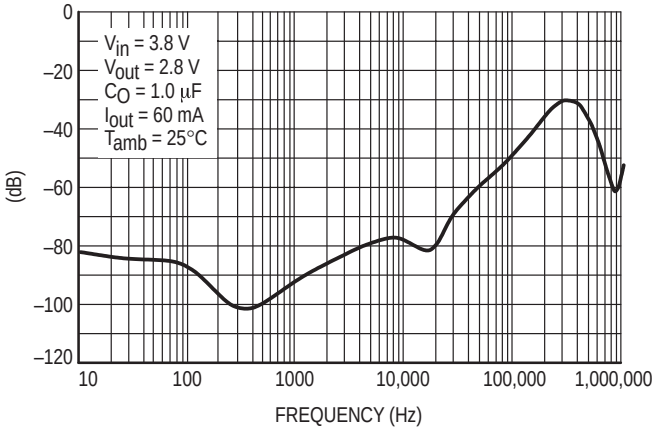
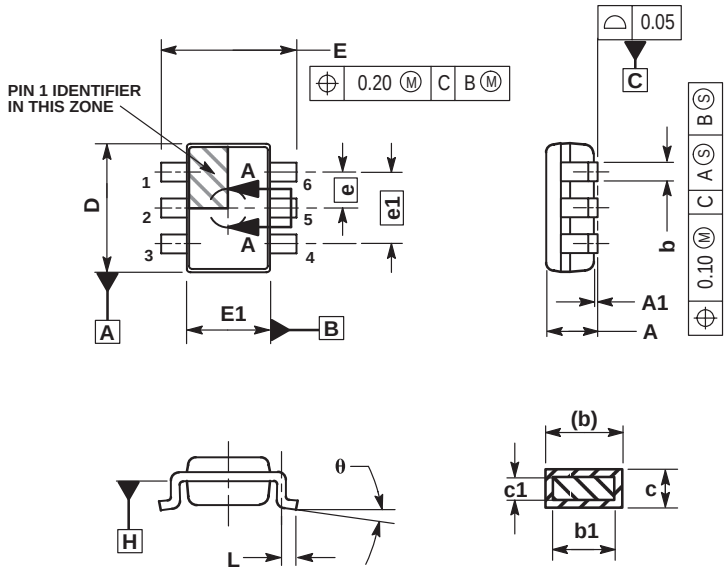


Figure 26. Ripple Rejection versus Frequency without Bypass Capacitor

PACKAGE DIMENSIONS

SOT–23L
NW SUFFIX
CASE 318J–01
ISSUE B



SECTION A–A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.23 PER SIDE.
4. DIMENSIONS b AND b2 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.40
A1	0.00	0.10
b	0.35	0.50
b1	0.35	0.45
c	0.10	0.25
c1	0.10	0.20
D	3.20	3.60
E	3.00	3.60
E1	2.00	2.40
e	0.95	
e1	1.90	
L	0.25	0.55
θ	0 °	10 °

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