MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33188

Prototype Information

BUS INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

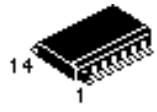
Bus Interface IC for Automotive Application

The MC33188D is a bus interface circuit especially designed to operate in the harsh automotive environment. It can be directly connected to a microcontroller and to the bus line. It is capable of interfacing several bus types, with single and multi wire configurations, including MIBus.

The bus line is internally short-circuit protected. The circuit has an automatic standby mode to minimize the current consumption. Receiving path remains active during sleep mode.

Several MC33188D can be connected to the same bus line and the device also includes a transmission monitoring circuit.

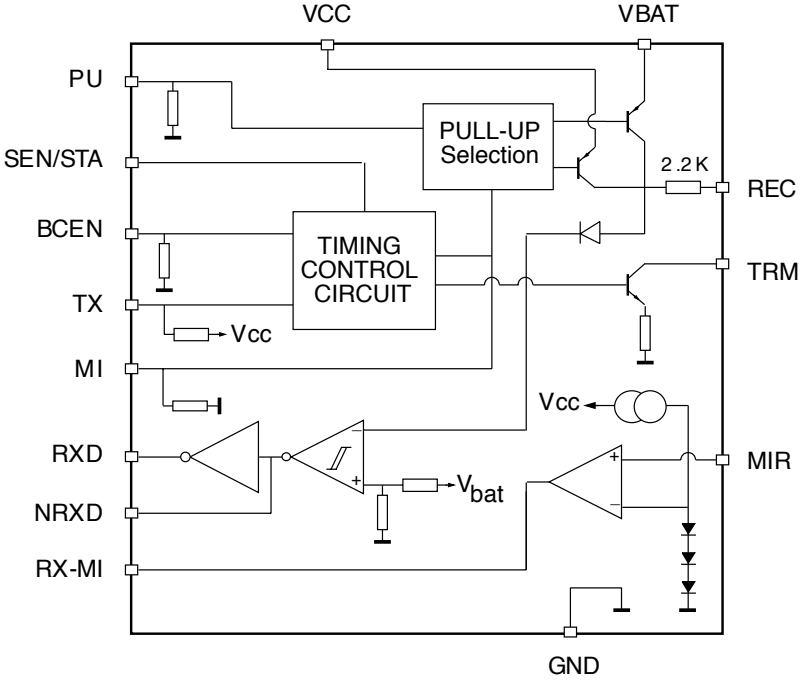
- Large Vbat Operating Range from 6 to 16 Volts
- Automatic Sleep Mode with Low Standby Current
- .Load Dump and Jump Start Protected
- MIBus Application
- Single, Multi wires and Full Duplex Operation Allowed
- 5V or 12V Bus High Voltage Level
- 2.2KΩ Bus Pull up Resistor
- Bus Line Short-circuit Protected
- -40°C to +85°C Operating Temperature Range
- CMOS Compatible Levels for Direct Microprocessor Interface
- Bus Line Thresholds Dependent on Vbat



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

ORDERING INFORMATION		
Device	Temperature Range	Package
XC33188D	-40°C to +85°C	SO14

Simplified Application Schematic



PIN CONNECTIONS

Pin 1: RX-MI
Pin 2 : MIR
Pin 3 : GND
Pin 4 : VCC
Pin 5 : TRM
Pin 6 : REC
Pin 7 : VBAT
Pin 8 : PU
Pin 9 : MI
Pin 10 : SEN/STA
Pin 11 : TX
Pin 12 : BCEN
Pin 13 : RXD
Pin 14 : NRXD

10/12/98
Rev 1.0

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Continuous Supply Voltage on Vcc	Vcc	5.5	V
Power Supply Voltage on Vbat - Continuous - During 15 seconds (jump start) - During 0.4 second (load dump)	Vbat	 16 25 40	V
REC, TRM, MIR Voltage - Continuous - During 15 seconds (jump start) - During 0.4 second (load dump)	Vmax	 -0.5 to 16 25 40	V
ESD Voltage : Human Body Model - All pins except pins 2 and 6 - Pins 2 and 6	Vesd	 2000 1500	V
Storage Temperature	Tstg	-55 to 150	°C
Operating Junction Temperature	Tj	-40 to 150	°C
Operating Ambient Temperature	Tamb	-40 to 85	°C

ELECTRICAL CHARACTERISTICS Vcc from 4.75 to 5.25V, Vbat from 6 to 16V, Tamb from -40°C to 85°C unless otherwise noted

Description	Symbol	Min	Typ	Max	Unit
RX-MI					
RX-MI Low Voltage at I = 5μA	VOL rxmi	-0.3		0.2 * Vcc	V
RX-MI High Voltage at I = -70μA	VOH rxmi	0.7 * Vcc		Vcc + 0.3	V
MIR					
MIR Threshold	THmir	1.5	2	3	V
MIR Input Current - Vmir = 0V - Vmir = 14.8V	Imir	 -200 -20	 -100 0	 0 20	μA
Vcc					
Vcc Supply Current : Vcc = 5V	Icc	0		1	mA
Vbat and Vcc Supply Current in Sleep Mode at Vcc = 5V and Vbat = 12V	Ism	50	100	135	μA
TRM					
TRM Saturation Voltage - At Vbat = 12V and I = 20mA - At Vbat = 16V and I = 25mA	SAT trm	 0 0	 0.3 0.36	 0.7 1	V
TRM Current Limit at Vtrm = 16V, Vtx = 0V	ICCtrm	25	50	100	mA
TRM Leakage Current at Vtrm = 16V, Vtx = 5V	ILtrm	0	_	100	μA
REC					
REC Pull Up Resistor	Rrec	1400	2200	3000	Ohms
REC Input Current - Vrec = 4.2V, Vbat = 12V - Vrec = Vbat = 12V - Vrec = 14.8V, Vbat = 1V	Irec	 0 0 0	 _ _ _	 60 10 10	μA
REC High Threshold: - Vbat = 6V - Vbat = 12V - Vbat = 16V	HTH rec	 2 6	 3.6 6.6 8.6	 4 9.5	V

ELECTRICAL CHARACTERISTICS Vcc from 4.75 to 5.25V, Vbat from 6 to 16V, Tamb from -40°C to 85°C unless otherwise noted

Description	Symbol	Min	Typ	Max	Unit
REC Low Threshold: - Vbat = 6V - Vbat = 12V - Vbat = 16V	LTH rec	 2.7 6.1	 2.9 5.8 7.1	 4 9	V
REC Hysteresis: - Vbat = 6V - Vbat = 12V - Vbat = 16V	HYS rec	 0.3 1	 0.6 0.8 1.5	 1.5 2.2	V
REC Output Level High Vbat = 12V, I = -100µA, TX = 5V	HLrec	10.8	11.6	12	V
REC Output Level High in MIBus mode Vbat = 12V, I = -50µA, MIsel = 1, PU = 0	HLrecmi	4.5	4.8	_	V
Vbat					
Vbat Supply Current Pull up OFF	Ibat			1	mA
Vbat Supply Current Pull up ON	Ibat			15	mA
PU					
PU Pull Down Resistor	Rpu	10	20	30	K
PU Input Voltage High	VIHpu	0.7 * Vcc		Vcc + 0.3	V
PU Input Voltage Low	VILpu	-0.3		0.3 * Vcc	V
PU Hysteresis	HYSpu	0.3	1	1.5	V
MI					
MI Pull Down Resistor	Rmi	10	20	30	K
MI Input Voltage High	VIHmis	0.7 * Vcc		Vcc + 0.3	V
MI Input Voltage Low	VILmis	-0.3		0.3 * Vcc	V
MI Hysteresis	HYSmis	0.3	1	1.5	V
SEN/STA					
SEN/STA Input Voltage High	VIHss	0.7 * Vcc		Vcc + 0.3	V
SEN/STA Input Voltage Low	VILss	-0.3		0.3 * Vcc	V
SEN/STA Hysteresis	HYSss	0.3	1	1.5	V
SEN/STA Output Voltage High at I = -20µA	VOHss	0.7 * Vcc			V
SEN/STA Output Voltage Low at I = 10µA	VOLss			0.2 * Vcc	V
SEN/STA Input Current. Vcc = 5.5V - At VSEN/STA = 1.65V - At VSEN/STA = 5.5V	Isen/sta	 -400 -200	 -160 0	 200 400	uA
TX					
TX Input Voltage High	VIHtx	0.7 * Vcc		Vcc + 0.3	V
TX Input Voltage Low	VILtx	-0.3		0.3 * Vcc	V
TX Hysteresis	HYStx	0.3	1	1.5	V

ELECTRICAL CHARACTERISTICS Vcc from 4.75 to 5.25V, Vbat from 6 to 16V, Tamb from -40°C to 85°C unless otherwise noted

Description	Symbol	Min	Typ	Max	Unit
BCEN					
BCEN Pull Down Resistor	Rbcen	10	20	30	K
BCEN Input Voltage High	VIHbcen	0.7 * Vcc		Vcc + 0.3	V
BCEN Input voltage Low	VILbcen	-0.3		0.3 * Vcc	V
BCEN Hysteresis	HYSbcen	0.3	1	1.5	V
RXD and NRXD					
RXD Low Voltage at I = 220μA (note 1)	VOLrxd	-0.3		0.3 * Vcc	V
RXD High Voltage at I = -220μA (note 1)	VOHrxd	0.7 * Vcc		Vcc + 0.3	V
NRXD Low Voltage at I = 220μA (note 1)	VOL nrxd	-0.3		0.3 * Vcc	V
NRXD High Voltage at I = -220μA (note 1)	VOH nrxd	0.7 * Vcc		Vcc + 0.3	V

NOTE 1 : These values are not affected even if REC Voltage is down to -10V.

DYNMIC CHARACTERISTICS (AT V_{BAT} = 12V and T_A = 25°C)

Ratings	Symbol	Min	Typ	Max	Unit
T Sleep	Tsl	10	40	200	ms
T Low	Tl	3	6	12	ms
T Bit_compare	Tbc	25	40	60	μs
TSperr	Tsp	0.9	1.36	1.8	ms
TRecovery	Tr	30	50	75	μs
Twake	Tw	_	_	2	μs
TRM time. C=40pF. REC&TRM connected. Pu=1 - Rise Time - Fall Time	TRMt	 1 1	 1.6 1.6	 2 2	V/μs
Delay time. C = 12pF - TX rise time to RXD rise time - TX fall time to RXD fall time - TX rise time to RXMI rise time - TX fall time to RXMI fall time	TD	 5 5 0.5 0.5	 10 8 3 1.3	 20 20 4 2.5	μs

PIN DESCRIPTION

Pin Number	Pin Name	Description
1	RXMI	This pin reflects the logical value of the MIR input pin.
2	MIR	This pin receives the data from the MIBus single line wire when the interface is in MIBus mode configuration.
3	GND	Gnd pin.
4	Vcc	5V typical power supply pin. Supply current is 0.8mA typical and down to 135μA in sleep mode.
5	TRM	Bus line transmission pin. It has the same phase as the input TX, it is an open collector structure, short-circuit protected.
6	REC	Bus line reception pin. The voltage level of the bus is determined through a selectable pull-up resistor connected to either Vcc or Vbat. Soothed depends on Vbat voltage, it is approximately : K x Vbat + Vbe.
7	Vbat	12V typical power supply pin. It supplies REC pull-up resistors and comparators.
8	PU	Pull-up selection for REC output. - PU = 0, pull-up resistor OFF - PU=1, pull-up resistor ON In the MIBus mode (MI=1), the bus line REC can be supplied at 5 or 12V, with pull-up resistor ON : - PU = 0 and MI = 1, REC is supplied at 5V (normal MIBus mode) - PU = 1 and MI = 1, REC is supplied at 12V (MIBus programming mode)
9	MI	MIBus selection. - MI = 1, the circuit is configured in the MIBus mode. - MI = 0, the circuit is configured for other bus applications. This pin has an internal pull down resistor. When MIBus is selected, the internal timing control circuit is disabled. MIBus = 1 switches on the pull-up resitor.
10	SEN/STA	Sender status pin is an input/output pin. As an input, if SEN/STA is forced at 0, the timing control circuit is disabled : output cannot be blocked, sending path is always free. If SEN/STA is forced at 1, output TRM and the sending path are blocked. As an output : the MCU can read back the status of the timing control circuit by reading the SEN/STA voltage level. - SEN/STA = 0 means that the sending path is free. - SEN/STA = 1 means that the sending path is blocked. In the MIBus mode (MI=1) the timing control circuit status is reported on SEN/STA but the sending path is always free.
11	TX	Transmission input. The logical state of TX is transmitted to output TRM. The logical state 1 forces the output transistor OFF and the logical state 0 forces the output transistor ON. It has an internal pull-up resistor.
12	BCEN	Bit Compare Enable. When BCEN = 1 the compare circuit for TX and REC is disabled. This pin has an internal pull down resistor.
13	RXD	Receive output. The logical state of REC is transmitted to RXD and NRXD. The input comparator threshold are adapted to Vbat voltage.
14	NRXD	This pin exhibit the complemented value of the data presented at RXD.

Timing Control Circuit

The purpose of this portion of the circuit is to monitor the transmission and to report the status to the microcontroller. If a special condition occurs, the timing control circuit will block the output and set the SEN/STA pin to 1.

Four special conditions exist :

1) TX = 0 for a time greater than Tlow (Tlow = 6 ms typical). In this case the control circuit blocks TRM output and set SEN/STA to 1.

2) TX = 1 and REC = 0 for a time greater than Tbit-compare (Tbit-compare = 40 μs typical). In this case, the control circuit blocks TRM output and set SEN/STA to 1.

3) TX = 1 and REC = 1 for a time greater than Tsperr (Tsperr = 1.36 ms typical). In this case, if the output has been previously blocked by one of the above condition, the sending path will be set free and SEN/STA set back to 0.

4) If condition TX = 0 less than Tlow with output not blocked by the timing control circuit is followed by condition TX = 1 and REC = 1 during min. Trecovery (Trecovery = 50 μs typical), then the timing control circuit is totally reseted (internal capacitor discharged). The sending path stays free and SEN/STA remains at 0.

When condition 1 or 2 occurs, the timing control circuit switches OFF the output transistor and set SEN/STA to 1. If BCEN = 1, the bit compare function condition 2 is disabled.

When MIBus is selected (MIsel = 1), the timing control circuit action is disabled. This means that the circuit operates and report its status on SEN/STA but doesn't block TRM ouput.

Sleep Mode Function

If TXD = 1 and no transition occurs on REC for a time greater than Tsleep (Tsleep = 40 ms typical) and if the circuit is not in MIBus mode (MI = 0), the circuit will be switched into the sleep mode.

In this mode the Vcc current is reduced to 135μA maximum, the receiving path from REC to RXD and NRXD remains active.

A transition on REC or a high to low transition on TXD will wake up the circuit within Twake.

TRUTH TABLE for PULL-UP and BUS MODE

MI	PU	Effect On Bus
Open or Low	Open or Low	No pull-up active
Open or Low	High	12V pull-up active
High	Open or Low	5V pull-up active - MIBus mode
High	High	12V pull-up active - MIBus programming mode

Figure 1. Single Wire MIBus Configuration

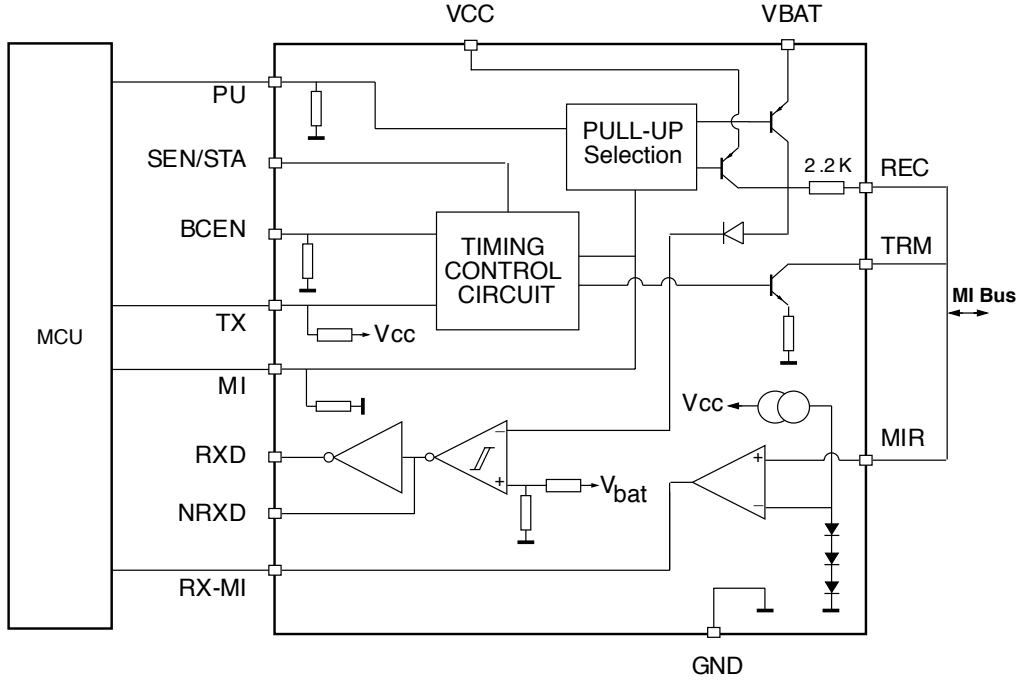


Figure 2. Single Wire Configuration

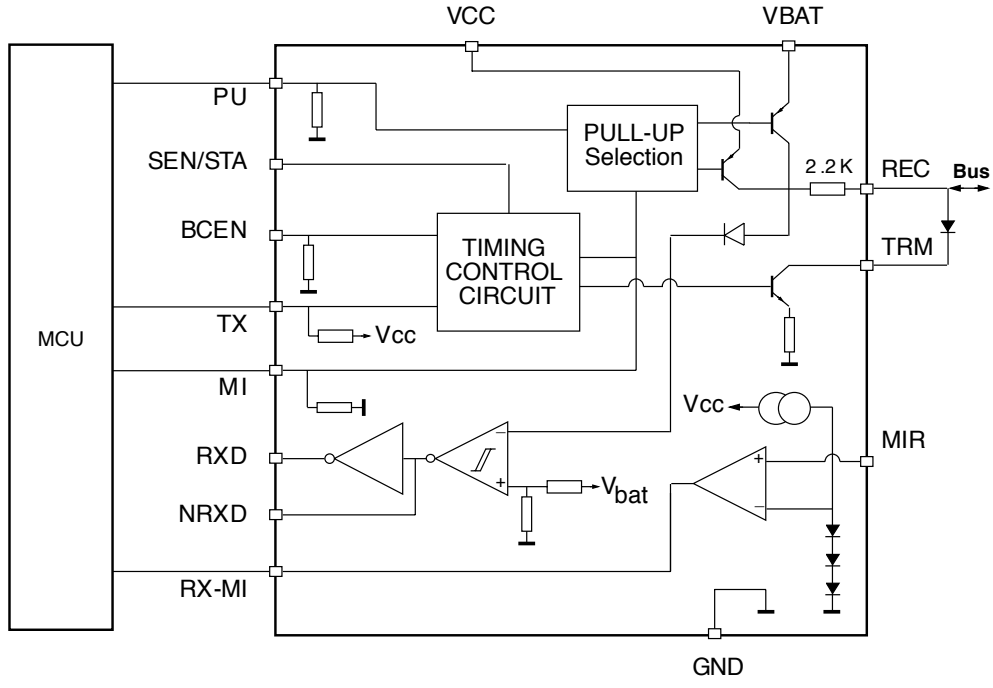


Figure 3. Full Duplex Configuration