MC33157

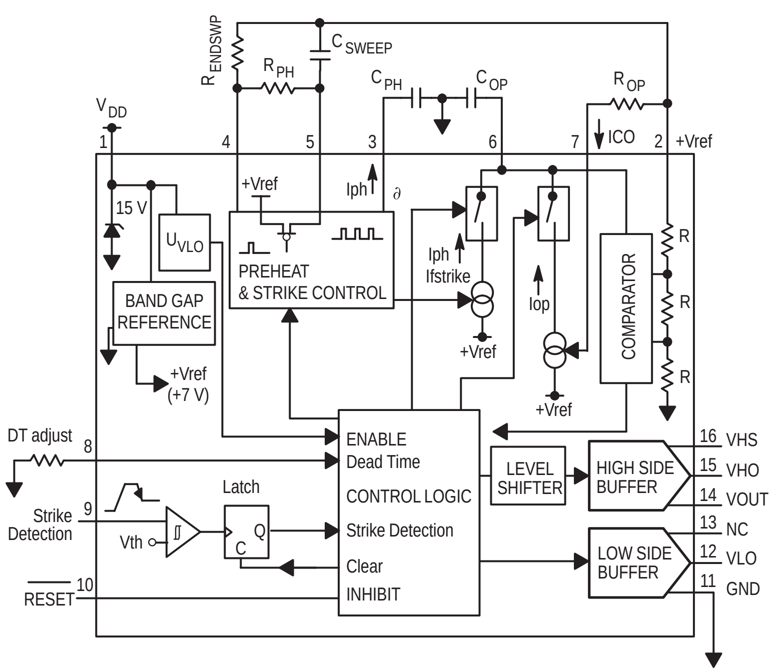
Half Bridge Controller and Driver for Industrial Linear Tubes

The MC33157 includes the oscillator circuit and two output channels to control a half–bridge power stage.

One of the channels is ground–referenced. The second one is floating to provide a bootstrap operation for the high side switch.

Dedicated Driver for Industrial Linear Tubes

- Main oscillator is current controlled, making it easy to set up by a single external resistor. On top of that, such a feature is useful to implement a dimming function by frequency shift.
- Filament pre–heating time control built–in.
- The strike sequence is controllable by external passive components, the resonnant frequency being independently adjustable. This frequency can be made different from the pre–heating and the steady state values. A frequency sweep between two defined values makes this IC suitable for any series resonnant topologies.
- Dedicated internal comparator provides an easy lamp strike detection implementation.
- Digital $\overline{\text{RESET}}$ pin provides a fast reset of the system (less than 10µs). Both output MOSFET are set to “OFF” state when $\overline{\text{RESET}}$ is zero.
- Adjustable dead time makes the product suitable for any snubber capacitor and size of MOSFET used as power switches.
- Designed to be used with standard setting capacitors ≤ 470nF.
- A voltage reference, derived from the internal bandgap, is provided for external usage. This voltage is 100% trimmed at probe level yielding a 2% tolerance over the temperature range.



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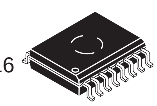
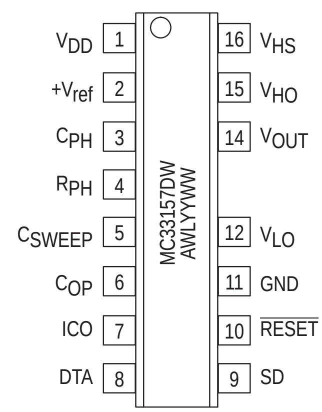


SO–16L
DW SUFFIX
CASE 751G

PIN CONNECTIONS AND MARKING DIAGRAM



AWL = Manufacturing Code
YYWW = Date Code

(Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC33157DW	Plastic SO–16L	47 Units / Rail

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Side Max Voltage	V_{HS}	600	V
Differential Max Voltage $V_{HS} – V_{OUT}$	ΔV_{HS}	16	V
High Side Output Voltage Range	V_{HO}	V_{OUT}–0.3 to V_{HS}+0.3	V
Low Side Output Voltage Range	V_{LO}	–0.3 to +16	V
Max V_{HS} Allowable Slew Rate	dV_{HS}/dt	±10	V/ns
Max V_{HO}/V_{LO} Allowable Slew Rate	dV_{HO}/dt, dV_{LO}/dt	±10	V/ns
Supply Voltage (Note 1) Maximum Power Dissipation @ T_A = 50°C Thermal Resistance Junction–to–Air Operating Junction Temperature	V_{DD} P_D $R_{\theta JA}$ T_J	16 600 140 –40 to +150	V mW °C/W °C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Electrostatic Discharge [HBMI]	ESD	2.0	kV

ELECTRICAL CHARACTERISTICS

(V_{DD} = 14V. All parameters are specified for –20°C to 85°C ambient temperature unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Input Threshold Voltage Turn–On Turn–Off	 UV_{ON} UV_{OFF}	 11 8.0	 12 8.5	 12.8 9.0	 V V
Clamp Voltage @ I_{CLAMP} = 10 mA	V_{CLAMP}	15	16	16.5	V
Supply Current (Note 2)	I_S		12		mA
Standby Current at No Load @ $V_{DD} < UV_{OFF}$	I_{STDBY}		1.5		mA
Quiescent Current at No Load @ $V_{DD} > UV_{ON}$	I_Q		2.5		mA
OUTPUT DRIVERS (V_{LO}, V_{HO})					
High Side VDS_{ON} @ Source current = 250 mA	$V_{DS}(P)$	–	880	1500	mV
Low Side VDS_{ON} @ Sink current = 300 mA	$V_{DS}(N)$	–	880	1500	mV
High Side / Low Side rise time @ C_{OUT} = 2 nF	t_r		40		ns
High Side / Low Side fall time @ C_{OUT} = 2 nF	t_f		35		ns
OSCILLATOR					
Output Max Frequency	f_{OSC}			250	kHz
Internal Master Clock Duty Cycle	DC	–	50	–	%
System operation programming recommended values	R_{OP} R_{PH} $R_{ENDSWEEP}$ R_{DTA} C_{OP}	68 68 68 10 100		560 560 2200 250 560	kΩ kΩ kΩ kΩ pF
V_{COP} High threshold		–	4.2	–	V
V_{COP} Low threshold		–	2.8	–	V
I_{COP} discharging current		–	400	–	µA
I_{COP} over I_{ROP} current ratio		–	2.0	–	

ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 14V. All parameters are specified for –20°C to 85°C ambient temperature unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING					
Preheat timing capacitor pulsed charging current (Duty Cycle=1/16)	It_{PH}	14	16	17	μA
Filament preheat time with C_{PH} = 0.47 μF	t_{PH}	–	2.0	–	s
Strike sequence recycling time with C_{PH} = 0.47 μF	t_{SK}	–	125	–	ms
C_{PH} charging current ratio	∂	–	1/16	–	
Strike sequence restart blanking time with C_{PH} = 470nF	t_{bk}	–	10	–	ms
Dead time: externally adjustable by Rdt	dt	0.3	–	2.5	μs
Dead time adjust resistance (Recommended range)	Rdt	10	–	220	kΩ
Dead time tolerance	dt_{Tol}		±10		%
VOLTAGE REFERENCE					
Voltage reference @ I_{LOAD} = 500 μA, T_J = 25°C	V_{REF}	–	7.0	–	V
Line regulation @ I_{LOAD} = 500 μA, T_J = 25°C	ΔV_{REF}	–	10	–	mV
Load regulation @ I_{LOAD} = 500 μA to 5 mA	ΔV_{REF}	–	10	–	mV
Maximum load current	I_{REFMAX}	–	–	25	mA
Total V_{REF} variation over Line, Temperature, Load	V_{REF}	6.85	7.0	7.15	V
INPUT					
Strike detect high voltage threshold	$VTH_{SD}HI$	–	4.0	–	V
Strike detect low voltage threshold	$VTH_{SD}LO$	–	3.75	–	V
Maximum current on strike detect input @ Regulation level	$I_{SD}HI$	–	–	10	nA
Maximum voltage on strike detect @ Regulation level	$V_{SD}HI$	–	–	7.0	V
Maximum current on strike detect input @ Low level	$I_{SD}LO$	–	–	10	nA
Maximum strike detect voltage negative input	$V_{SD}NEG$	–	–	–0.3	V
Strike detect minimum pulse width	SDPW	50	100	–	ns
$\overline{RESET}$ high voltage	$\overline{RST}HI$	–	1.8	2.2	V
$\overline{RESET}$ low voltage	$\overline{RST}LO$	1.6	1.8	–	V
$\overline{RESET}$ input current @ high voltage		–	–20	–	μA
$\overline{RESET}$ input current @ low voltage		–	–20	–	μA
$\overline{RESET}$ maximum voltage		–	–	7.0	V
$\overline{RESET}$ maximum negative voltage		–	–	–0.3	V

NOTES:
(1) Since this device has a built–in zener, one cannot use a low impedance supply to drive this pin. Having a current limit mode by external means is mandatory.
(2) Test Conditions: C_{OUT} = 2.2 nF, f = 100 kHz, V_{DD} = 15V.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Function	Description
1	V_{DD}	Supply voltage input	This pin provides the DC supply to the circuit. The voltage is internally clamped by a zener connected to the ground. It is NOT allowed to use a DC low impedance power supply to feed this pin, but limiting the current by an external resistor is mandatory. It is recommended to damp this pin to ground by an electrolytic capacitor connected close to pin 1.
2	$+V_{ref}$	Voltage reference output	This pin provides a +7V voltage reference derived from the internal bandgap. The +Vref can supply up to 25 mA and shall be decoupled to ground by a 220nF ceramic capacitor
3	C_{PH}	Preheat timing capacitor	This capacitor sets two timings: filaments preheat time (t_{PH}) and strike sequence recycle time (t_{SK}). It is charged with a constant current and cares must be observed to minimize the leakage current at this pin to get the expected timing. Typically, a 0.47 μF capacitor will give a 2 seconds pre–heating time and a 125 ms strike sequence recycle time. (See details given by figure 9)
4	R_{PH}	Preheat and Strike frequencies adjustment resistors	The R_{PH} resistor together with $R_{ENDSWEEP}$ and C_{OP} defines the frequency used to preheat the filaments ($f_{PH} = f_1$). $R_{ENDSWEEP}$ defines the strike frequency ($f_{ENDSWEEP} = f_2$). During the sweep timing, the frequency will sweep from the high pre–heating f_1 to the low strike f_2 values. Normally, f_1 is far from the LC resonance but f_2 is close enough to generate the high voltage across the fluorescent tube. (See details given by figure 9)
5	C_{SWEEP}	Frequency sweep timing capacitor	This timing define the sweep time from f_1 to f_2. Since the timing capacitor is charged with a low constant current, cares must be observed to minimize the leakage current at this pin to get the expected timing. Since this capacitor is charged through resistor R_{PH}, the voltage rises according to an exponential and the frequency shifts with the same law.
6	C_{OP}	Oscillator capacitor	This pin defines the steady state operation frequency ($f_3 = f_{OP}$) of the controller. Since this timing capacitor is charged with a low constant current, cares must be observed to minimize the leakage current at this pin to get the expected frequency. Film type capacitor are recommended (polycarbonate).
7	ICO	Steady state operating frequency adjustment current input	Since the circuit uses a Current Controlled Oscillator (ICO), the current forced into this pin will control the operating frequency. The allowable current range is from 1 μA to 500 μA. The +Vref output can be used to provide the voltage across R_{OP}. An auxiliary voltage source can be used to implement a dimming function.
8	DTA	Dead Time Adjust	This pin provides an access to the internal timing system to adjust the dead time between the gate drive of the High and Low power switches connected, respectively, to pin V_{HO} and V_{LO}.
9	SD	Strike detection input	This pin drives a comparator, with an internal fixed reference, and acknowledges the tube strike. When a negative going slope (across the internal reference) is detected, the system considers the lamp has struck and the oscillator jumps from the present frequency value, which is within the window defined by R_{PH} and $R_{ENDSWEEP}$ to the steady state value defined by R_{OP}. If no negative going slope is detected on this pin, the system will repeat the sweep and strike sequence four times, then stops. The circuit will re–start from either a RESET, or by pulling $+V_{DD}$ to ground. The input signal can be either a logic level or an analog voltage ramping up from zero to +Vref followed by a negative going slope to zero. In any case, the positive pulse width must be 1 μs minimum. The pcb layout must be designed to minimize the noise at this pin. (See details given by figures 8, 9, & 10)
10	$\overline{RESET}$	Master reset input	Forcing a logic zero to this pin (HCMOS low level) will reset the circuit, initializing a frequency sweep and lamp strike sequence. The master reset does not include the pre–heating timing. The minimum pulse width requested is 10μs to guarantee a reset state. However, this pin has no built in filtering and a shorter pulse may initialize a reset sequence: it is the responsibility of the designer to make sure that no noise or parasitic pulse are developed at the RESET input. A full re–start of the sequence, including the pre–heating time, can be initialized by pulling the $+V_{DD}$ pin to ground. In this case, $+V_{DD}$ and $\overline{RESET}$ must be simultaneously released to a high state. When RESET is asserted low (active) both outputs MOS are biased in the off condition. An internal 20μA pull up current forces the pin to logic one, allowing the designer to left this pin open if the RESET function is not used. In order to avoid any uncontrolled state of the output drivers, it is recommended to set up a 10ms low level at pin 10. The reset is activated in less than 10 microsecond, but releasing this pin while the Vcc supply is high (above 300V) can generate a random operation, depending upon the dv/dt coming from the power supply.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Function	Description
11	GND	Ground (zero voltage reference)	Since high and fast currents circulate in the circuit, it is mandatory to build a single ground point in the system.
12	V_{LO}	Low side driver output	This pin provides the V_{GS} to drive the Low side power MOSFET.
13	NC	Not Connected	
14	V_{OUT}	High side common point / Half bridge output	This pin is connected to the output of the half bridge and is referenced for the High side switch.
15	V_{HO}	High side driver output	This pin provides the V_{GS} to drive the High side power MOSFET.
16	V_{HS}	High voltage boost supply	The gate drive of the High side switch is derived from this voltage.

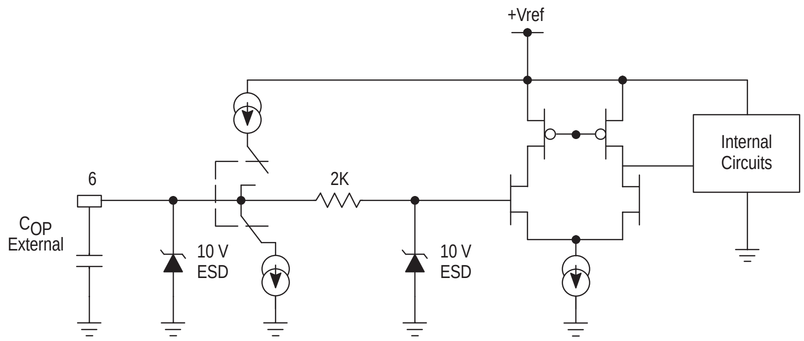


Figure 1. PIN 6 C_{OP} INPUT

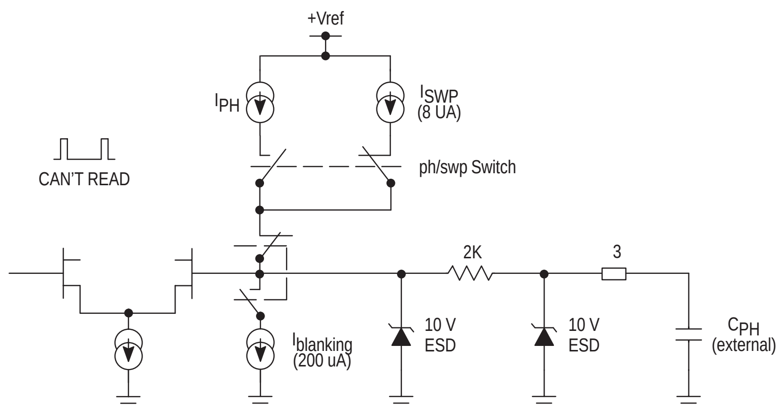


Figure 2. PIN 3 C_{PH} INPUT

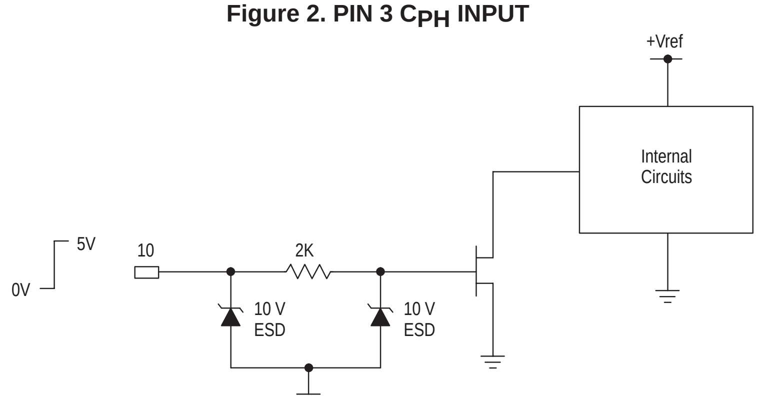


Figure 3. PIN 10 $\overline{\text{RESET}}$

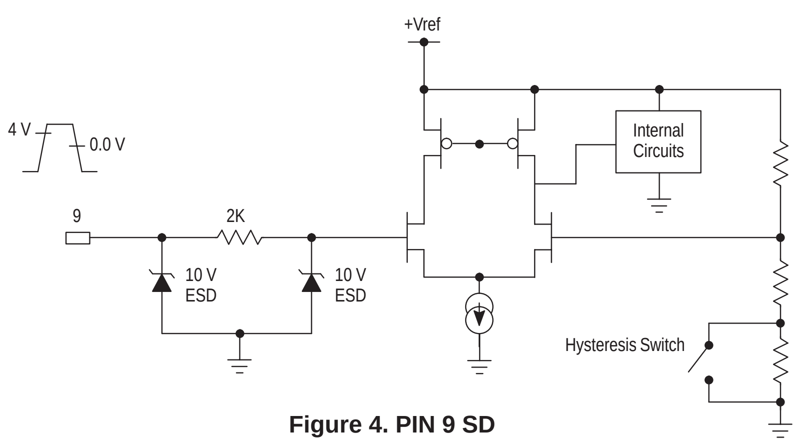


Figure 4. PIN 9 SD

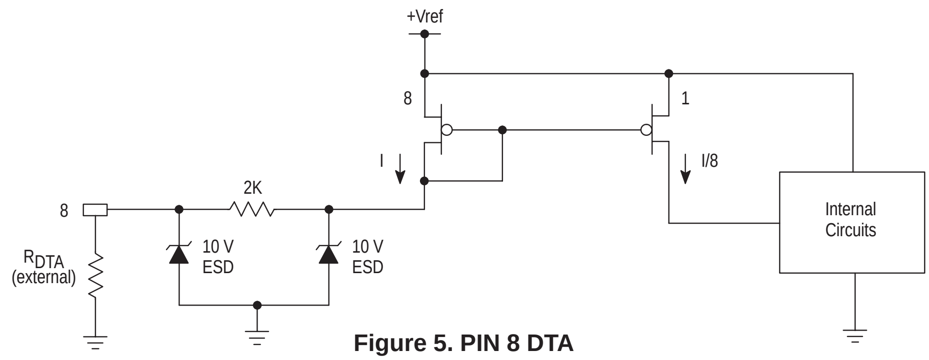


Figure 5. PIN 8 DTA

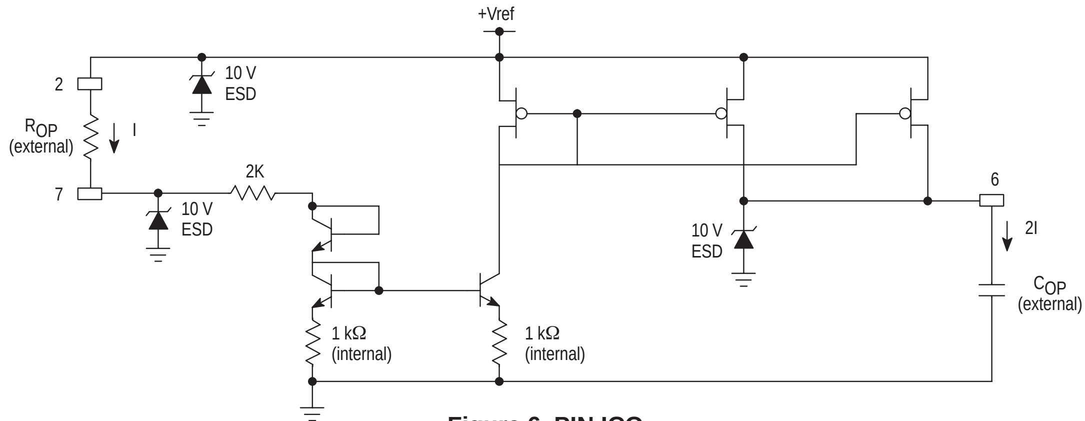


Figure 6. PIN ICO

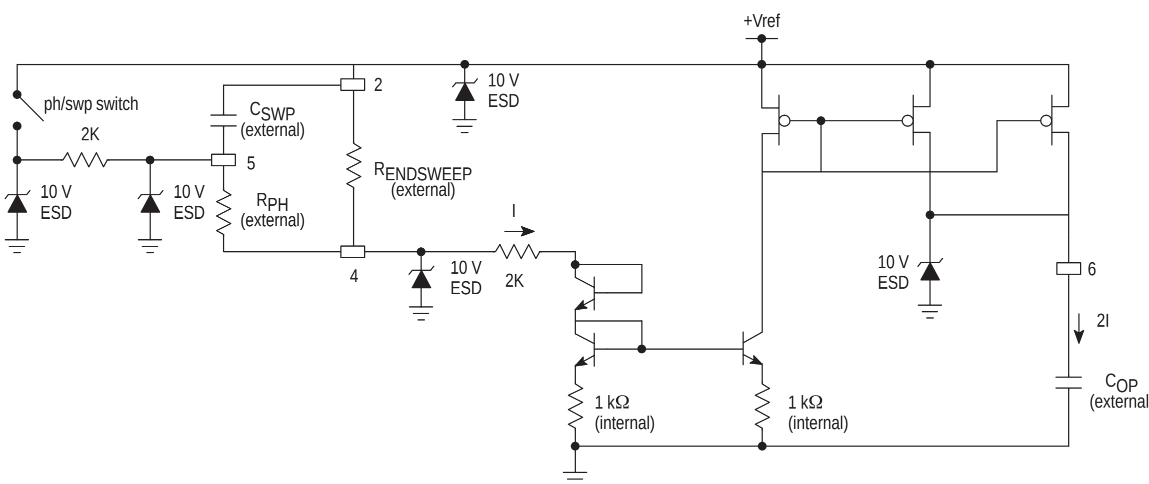


Figure 7. PIN 2, 4 & 5 V_{ref}, R_{PH} & C_{SWP}

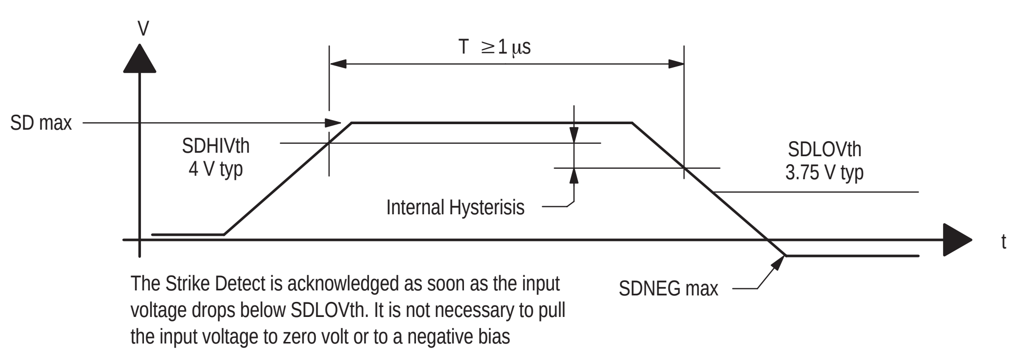
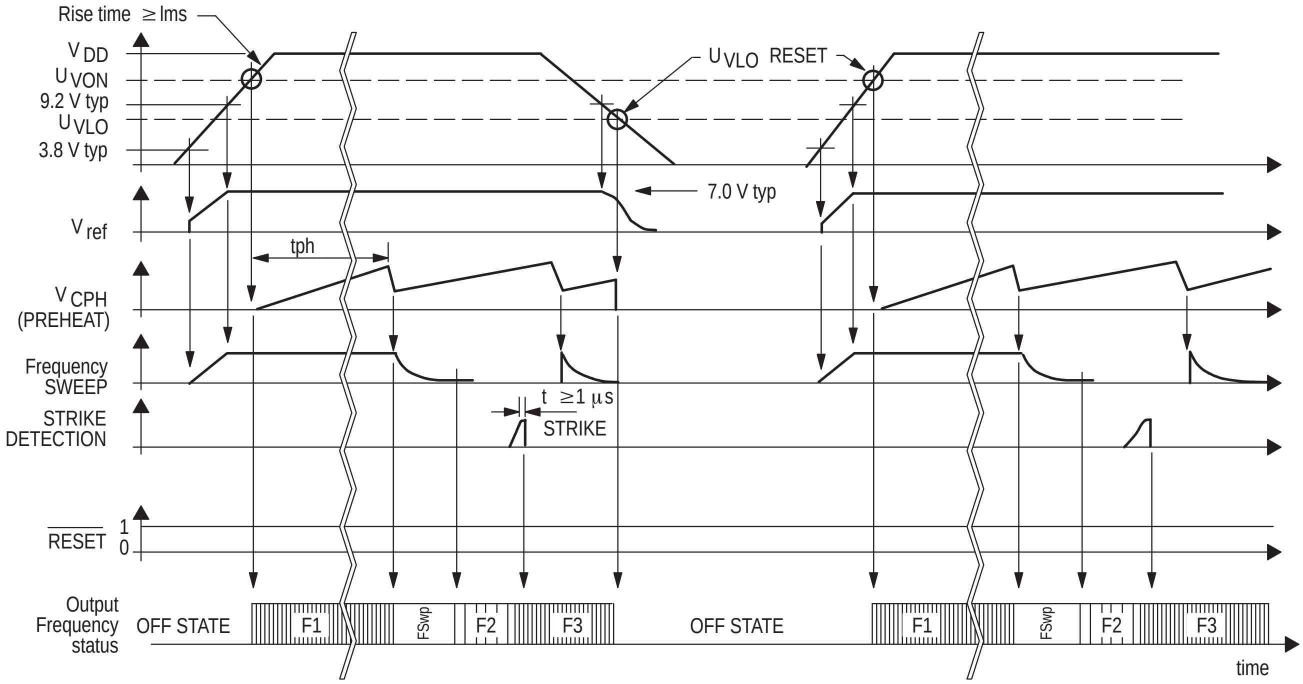


Figure 8. STRIKE DETECTION



$f_1 = f_{PH}$, preheating frequency adjusted by R_{PH} and $R_{ENDSWEEP}$

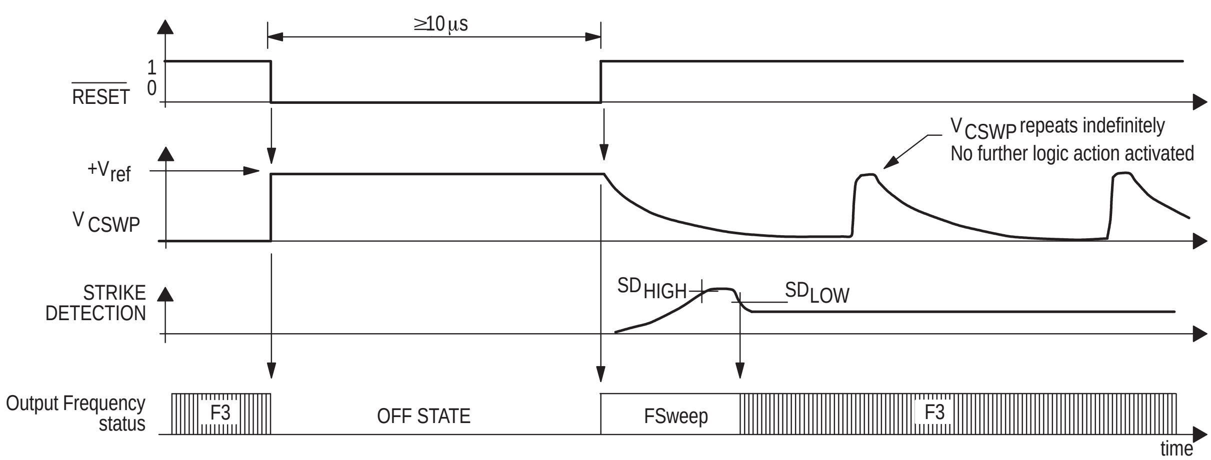
$f_2 = f_{ENDSWEEP}$, end of sweep frequency, adjusted by $R_{ENDSWEEP}$ (pin 2). In any case $f_1 \geq f_2$

$f_3 = f_{OP}$, operating frequency controlled by the I_{CO} current (pin 7) and capacitor C_{OP}

$t_{PH} = (C_{PH} * 2/3 * Vref) / (\partial * I_{tPH})$

"OFF" state: High side switch OFF, Low side switch ON

Figure 9. TIMING DIAGRAM (Normal startup sequence and U_{VLO} reset)



Previous On state

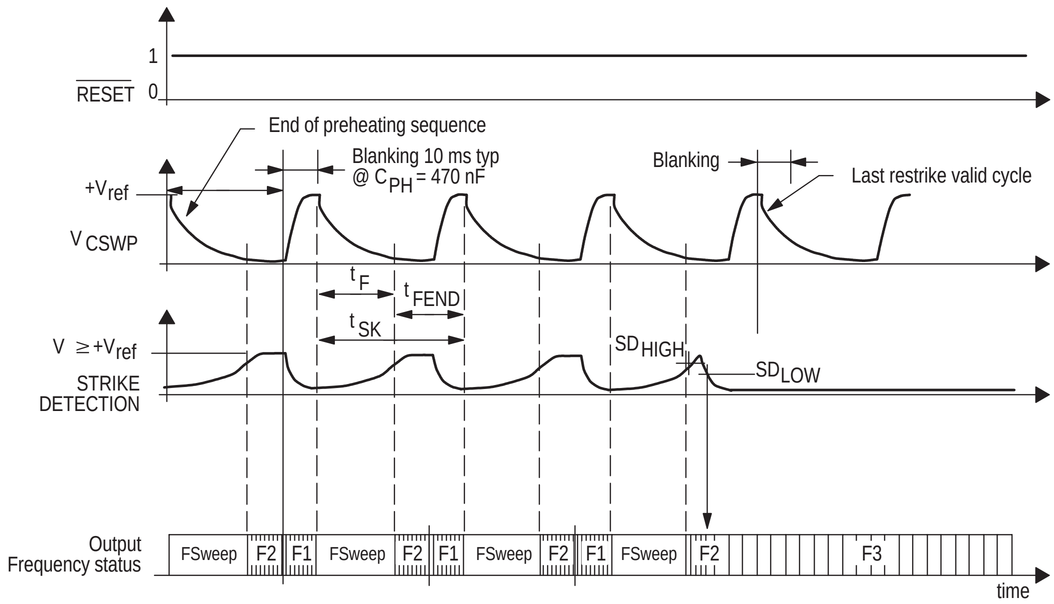
When RESET pin is released to a logic one, the system jumps to the preheat frequency as defined by RPH, then executes a frequency sweep down to $f_{ENDSWEEP}$, as defined by $R_{ENDSWEEP}$, and waits until a strike detection signal is applied to pin 9. There is no preheating timing performed after a reset coming from pin 10.

RESET logic level is CMOS compatible.

Note: Strike detection lever can be either digital – CMOS or analog as depicted here above, as long as the signal fulfills the SD_{HIGH} and SD_{LOW} values and timing.

OFF STATE: both output MOSFET are biased in the off condition.

Figure 10. TIMING DIAGRAM (External reset)



t_{SF}: Sweep Frequency time. This time is given by the RC network built with C_{SWEEP} and R_{PH}.
t_{SK}: Sweep sequence recycle time. This time is derived by integrating a constant DC current in capacitor C_{PH}. There is a fixed ratio (∂) between the preheating time t_{PH} and strike sequence recycle time t_{SK}.
t_{fEND}: Time during which f = (f_{ENDSWP}). This time is equal to $t_{SK} - t_{SF}$.

The controller repeats the f_{SWEEP} and the strike sequence until there is a STRIKE signal coming from the external circuit, or until FOUR sequences have been counted. Following a non strike situation, the controller goes in a full STOP and can be reinitialized by either pulling the V_{DD} pin 1 to ground or by forcing a low to the RESET pin 9. The controller assumes the lamp has struck when a negative going transient is applied on the STRIKE detection pin 10. On the other hand, in order to avoid false strike information, the controller force a blank time between the end of t_{SWEEP} and the start of the next sequence.

Figure 11. TIMING DIAGRAM (no strike conditions)

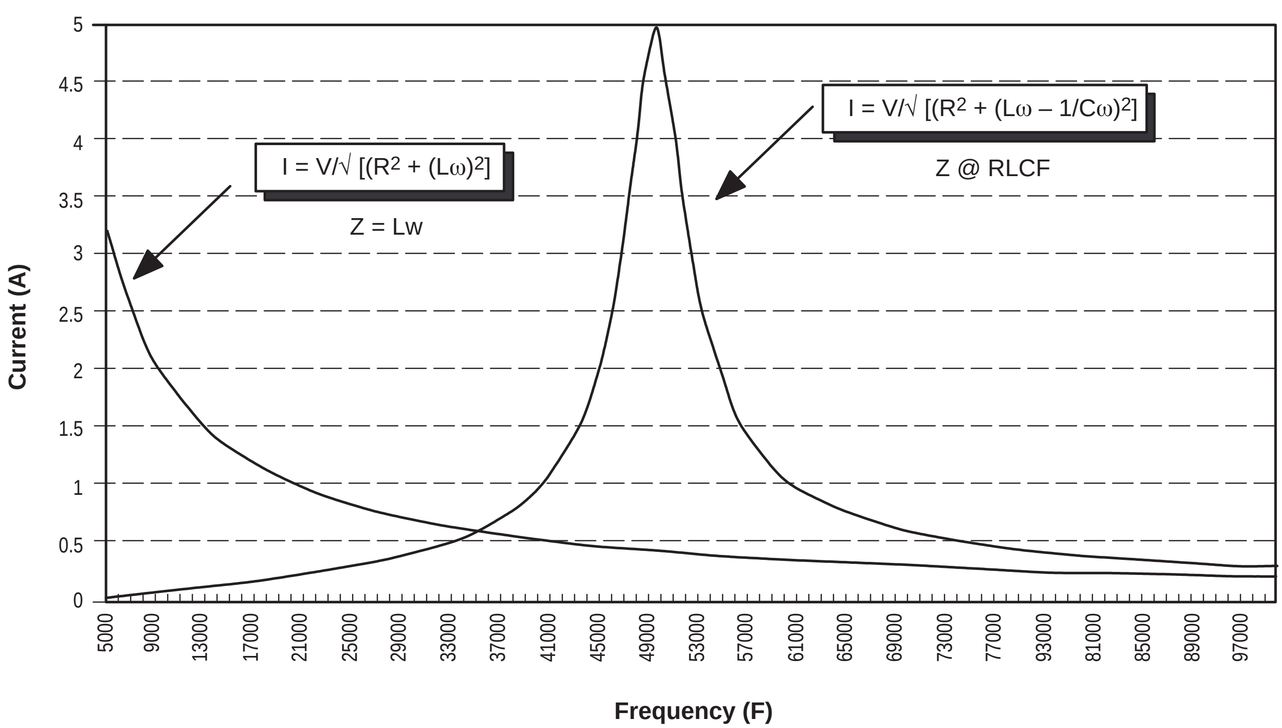
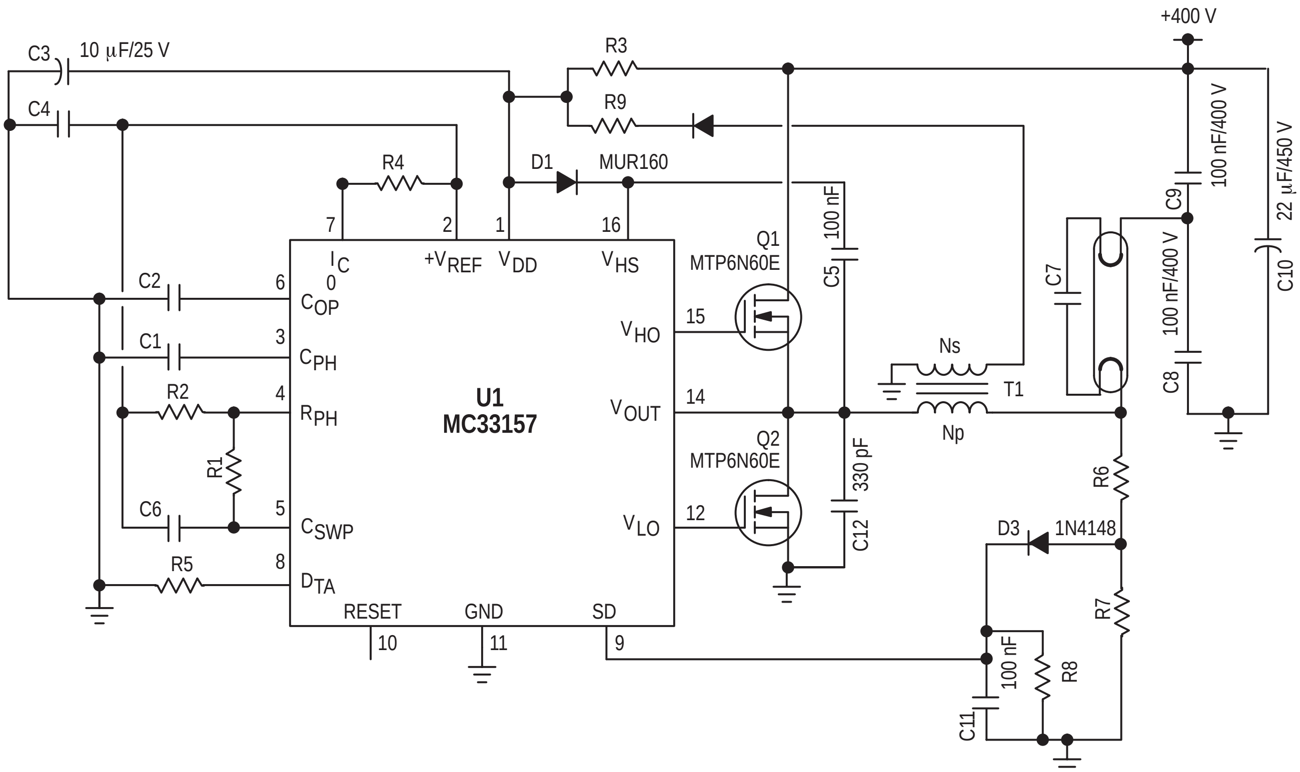


Figure 12. OUTPUT = f (freq) @ Lc = 1.5 mH, Cs = 6.8 nF



Typical Values for F_{PH} = 70 kHz, F_{OP} = 45 kHz, t_{PH} = 2 s, t_{SWEEP} = 125 ms

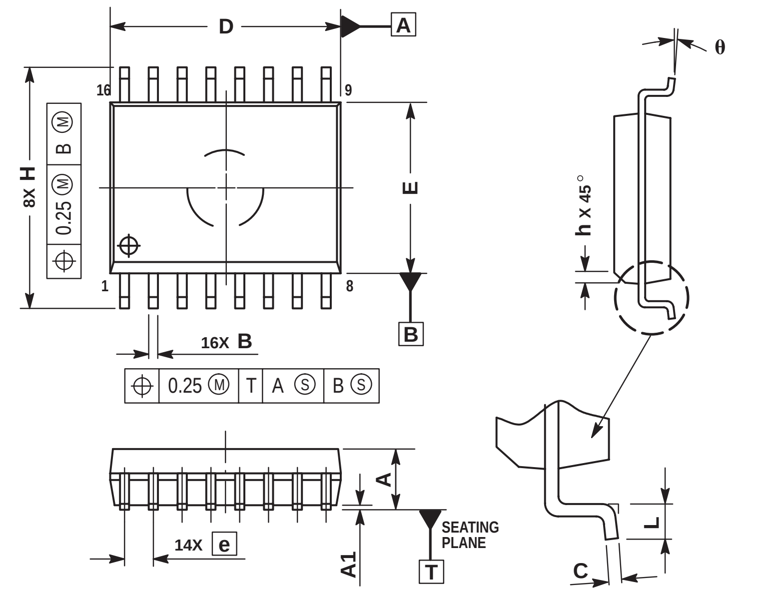
T1	Np =	R1	390 kΩ	C1	470 nF/25 V/Polyester
	Ns =	R2	62 kΩ	C2	470 pF/2%/50 ppm
	Lp = 150 mH	R3	100 kΩ – 0.5 W	C3	10 μF/25 V/Electrolytic
Q1	MTP6N60E	R4	100 kΩ	C4	220 nF/Polyester
Q2	MTP6N60E	R5	82 KΩ	C5	100 nF/63 V/Polyester
D1	MUR160RL	R6	1 MΩ	C6	220 nF/25 V/Polyester
D2	MUR120RL	R7	68 KΩ	C7	6.8 nF/5%/1000 V
D3	1N4148	R8	68 kΩ	C8	100 nF/400 V/Polyester
U1	MC33157	R9	22 Ω	C9	100 nF/400 V/Polyester
				C10	22 μF/450 V/Electrolytic
				C11	100 nF/25 V/Polyester
				C12	330 pF/500 V/Polyester

TO SEE: AN1682 (Using the MC33157 Electronic Ballast Controller)

Figure 13. Typical Application Schematic Diagram

PACKAGE DIMENSIONS

SO–16L
DW SUFFIX
PLASTIC PACKAGE
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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