MC14598B

8-Bit Bus-Compatible Latches

The MC14598B is an 8–bit latch addressed with an external binary address. The 8 latch–outputs are high drive, three–state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2.

All 8 outputs from the latches are available in parallel when $\overline{\text{Enable}}$ is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

- Serial Data Input
- Three–State Bus Compatible Parallel Outputs
- Three–State Control Pin ($\overline{\text{Enable}}$) TTL Compatible Input
- Open Drain $\overline{\text{Full}}$ Flag (Multiple Latch Wire–O Ring)
- Master Reset
- Level Shifting Inputs on All Except $\overline{\text{Enable}}$
- Diode Protection — All Inputs
- Supply Voltage Range — 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range
  With Fanout as Follows:
  1 TTL Load
  4 LSTTL Loads

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}	Input Voltage Range, Enable (DC or Transient)	–0.5 to V_{DD} + 0.5	V
V_{in}	Input Voltage Range, All Other Inputs (DC or Transient)	–0.5 to V_{DD} + 12	V
V_{out}	Output Voltage Range, (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

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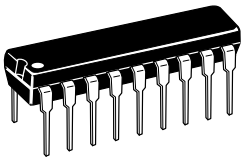
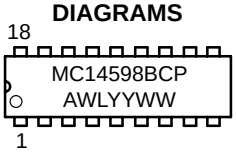


MARKING DIAGRAMS



PDIP–18
P SUFFIX
CASE 707

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

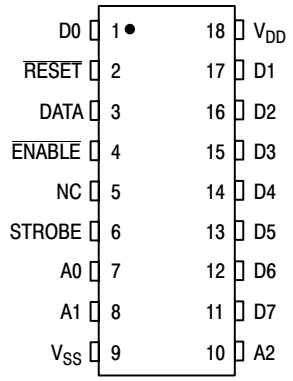
ORDERING INFORMATION

Device	Package	Shipping
MC14598BCP	PDIP–18	20/Rail

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

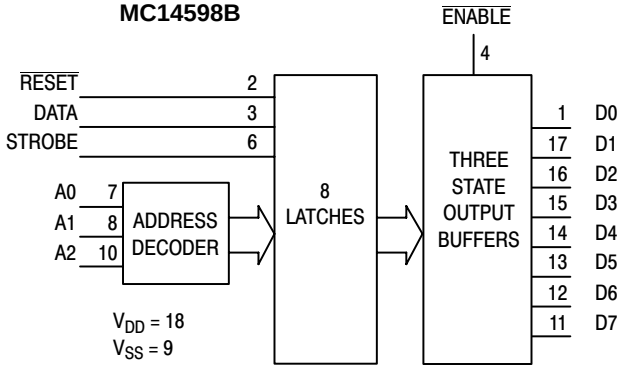
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



BLOCK DIAGRAMS

MC14598B



OUTPUT TRUTH TABLE

$\overline{\text{Enable}}$	Outputs
1	High Impedance
0	D_n

D_n = State of nth latch

NC = NO CONNECTION

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (4.) — $\overline{\text{Enable}}$ “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	0.8 1.6 2.4	— — —	1.1 2.2 3.4	0.8 1.6 2.4	— — —	0.8 1.6 2.4	Vdc
“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	2.0 6.0 10	— — —	2.0 6.0 10	1.9 3.1 4.3	— — —	2.0 6.0 10	— — —	Vdc
Input Voltage “0” Level Other Inputs (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) “1” Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current Source ($\overline{\text{Full}}$ — Sink Only) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 10 1 5	– 1.0 — —	– — —	– 1.0 — —	– 2.0 – 6.0 – 12	— — —	– 1.0 — —	— — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	1.6 — —	— — —	1.6 — —	3.2 6.0 12	— — —	1.6 — —	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Three–State Leakage Current	I_{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current at an External Load Capacitance of 130 pF (4.)	I_T	5.0 10	I_T = (2.0 µA/kHz) f + I_{DD} I_T = (4.0 µA/kHz) f + I_{DD} I_T = (6.0 µA/kHz) f + I_{DD}							µAdc

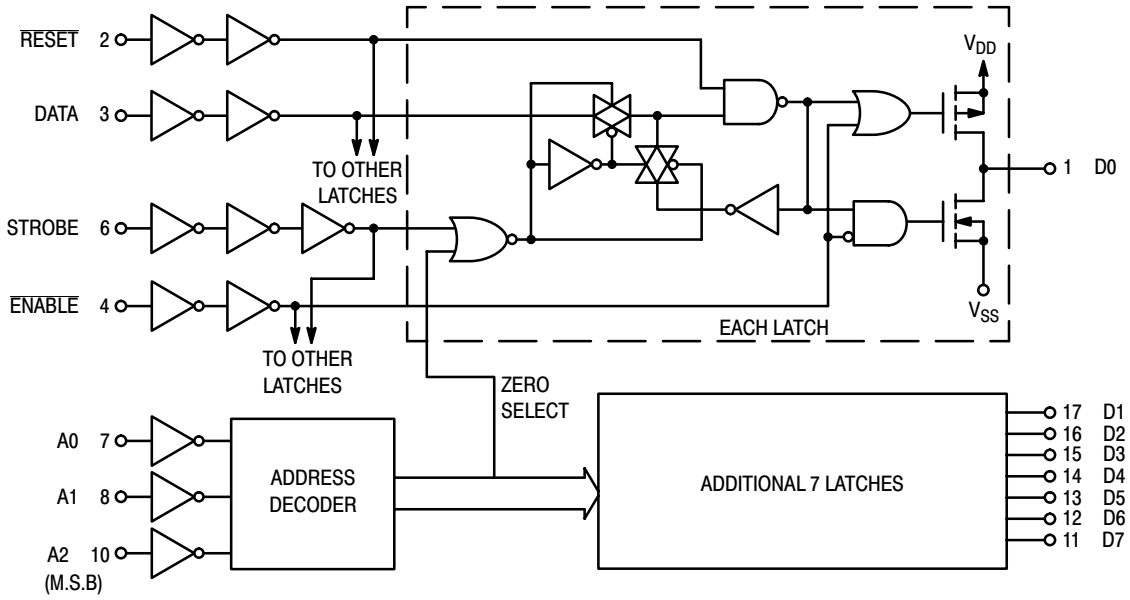
3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS [5.] (T_A = 25°C, C_L = 130 pF + 1 TTL Load)

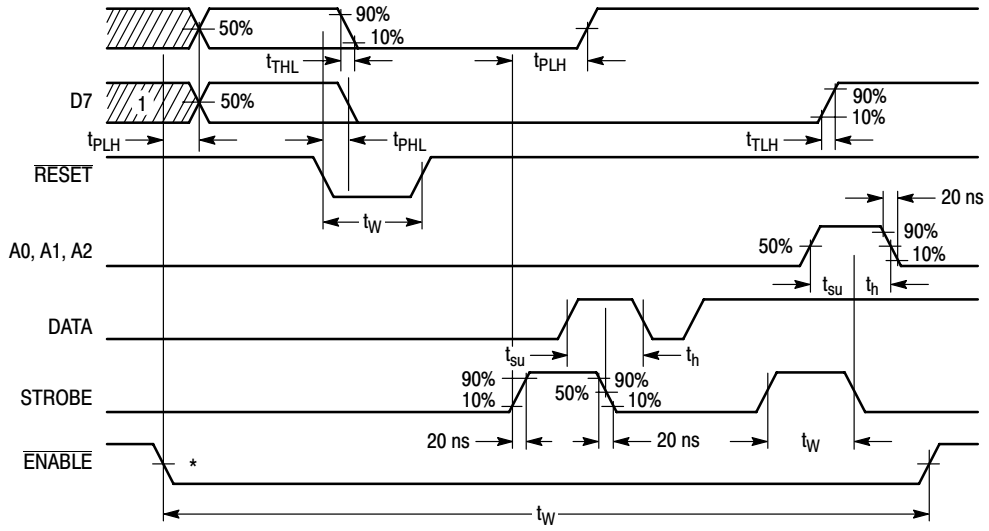
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ [6.]	Max	
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (0.5 ns/pF) C_L + 35 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.2 ns/pF) C_L + 25 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.16 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
$\overline{\text{Enable}}$ to Output	t_{PHL}	5.0	—	160	320	
		10	—	125	250	
		15	—	100	200	
Strobe to Output		5.0	—	200	400	
		10	—	100	200	
		15	—	80	160	
$\overline{\text{Reset}}$ to Output		5.0	—	175	350	
		10	—	90	180	
		15	—	70	140	
Pulse Width	t_{WH},					ns
$\overline{\text{Enable}}$	t_{WL}	5.0	320	160	—	
		10	240	120	—	
		15	160	80	—	
Strobe		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
Increment		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
$\overline{\text{Reset}}$		5.0	300	150	—	
		10	160	80	—	
		15	100	50	—	
Setup Time	t_{su}					ns
Data		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Address		5.0	200	100	—	
		10	100	50	—	
		15	70	35	—	
Hold Time	t_h					ns
Data		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Address		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	20	– 25	—	ns
		10	20	– 15	—	
		15	20	– 10	—	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

MC14598B FUNCTION DIAGRAM



MC14598B TIMING DIAGRAM



*1.4 V with V_{DD} = 5.0 V

NOTES:

1. High–impedance output state (another device controls bus).
2. Output Load as for MC14597B.

LATCH TRUTH TABLE

Strobe	$\overline{\text{Reset}}$	Address Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

*= No change in state of latch

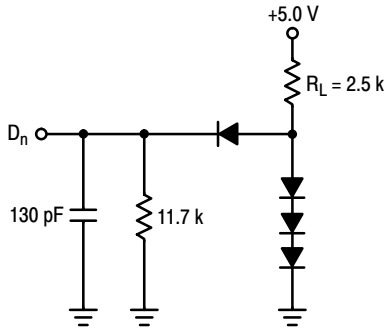
X = Don't care

TRUTH TABLE FOR MC14597B

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
↓	X	1	Count Up	—
↑	X	1	No Change	—
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care

TEST LOAD
ALL OUTPUTS



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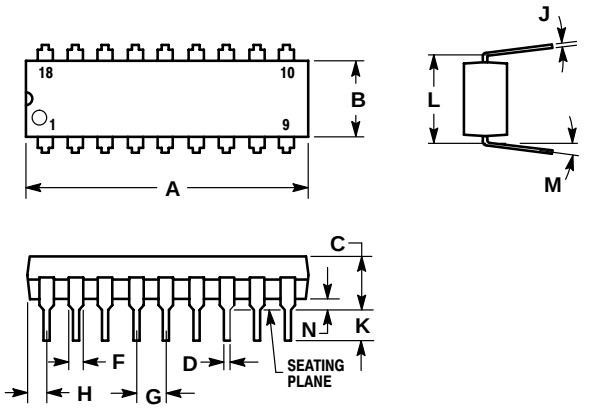
PACKAGE DIMENSIONS

PDIP–18
P SUFFIX
PLASTIC DIP PACKAGE
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

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