MC145572EVK

Technical Summary

ISDN U-Interface Transceiver Evaluation Kit

The MC145572EVK U–Interface Transceiver Evaluation Kit provides Motorola ISDN customers a convenient and efficient vehicle for evaluation of the MC145572 ISDN U–Interface Transceiver. The approach taken to demonstrate the MC145572 U–Interface Transceiver is to provide the user with a fully functional NT1 (Network Termination Type 1) connected to an LT (Line Termination). An NT1 provides transparent 2B+D data transfer between the U– and S/T–Interfaces. In addition, it provides for network initiated maintenance procedures. The MC145572EVK does not terminate any ISDN call control messages. It also does not terminate any maintenance messages received over the S/T–Interface.

The MC145572EVK U–Interface Transceiver Evaluation Kit can be functionally separated into two “halves”. The left half of the card is the NT1, while the right half of the card is the LT. Alternately it can be thought of as having both ends of the two–wire U–Interface, extending from the customer premise (NT1) to the switch line card (LT) on a single, stand–alone evaluation board.

The kit provides the ability to interactively manipulate status registers in the MC145572 U–Interface Transceiver as well as in the MC145474 S/T–Interface Transceiver with the aid of an external terminal. A unique combination of hardware and software features allows for standalone or terminal activation of the U–Interface, and as such provides an excellent platform for NT1 and LT hardware/software development. The NT1 function can be disabled by putting DIP switch S3–3 in the NT1 DIS position.

A complete data sheet for the MC145572EVK is available from the MOS Digital–Analog IC Division Service Center.

General

- Provides Standalone NT1 and LT on a Single Board
- Board Can Be Broken Apart Providing Separate NT1 and LT
- On–Board 68HC05 Microcontrollers with Resident Monitor Software
- Convenient Access to Key Signals
- NT1 and LT Software Development Platform

Hardware

- + 5 Volt Only Power Supply
- “Push–Button” Activation of U–Interface from NT1 or LT
- Standalone Operation for Bit Error Rate Testing
- Gated Data Clocks Provided for Bit Error Rate Testing
- Interfaces to ADS302 Evaluation Board
- Can Be Used as a U– or S/T–Interface Terminal Development Tool
- On–Board 5 ppm LT Frequency Reference
- EIA–232 (V.28) Serial Port(s) for Terminal Interface

Software

- Standalone or Terminal Operation
- Resident Firmware Monitor for User Control of Board
- Activation and Deactivation Menus
- Embedded Operations Channel
- Microcontroller Controlled or Automatic Activation/Deactivation
- Access to All Maintenance Channels
- MC68HC05 Assembly Language Source Code Available

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BLOCK DIAGRAM

Following is a basic functional block diagram for the MC145572EVK U–Interface Transceiver Evaluation Kit (Figure 1). Note that the dotted line represents the physical and logical separation between the NT1 and the LT sides of the evaluation board. While the board is capable of activating “standalone”, the user may decide to use a single ASCII terminal to gain total control of the MC145572EVK’s activities. Or, the user may choose to split the board, allowing the NT1 and LT entities to be physically located in separate areas.

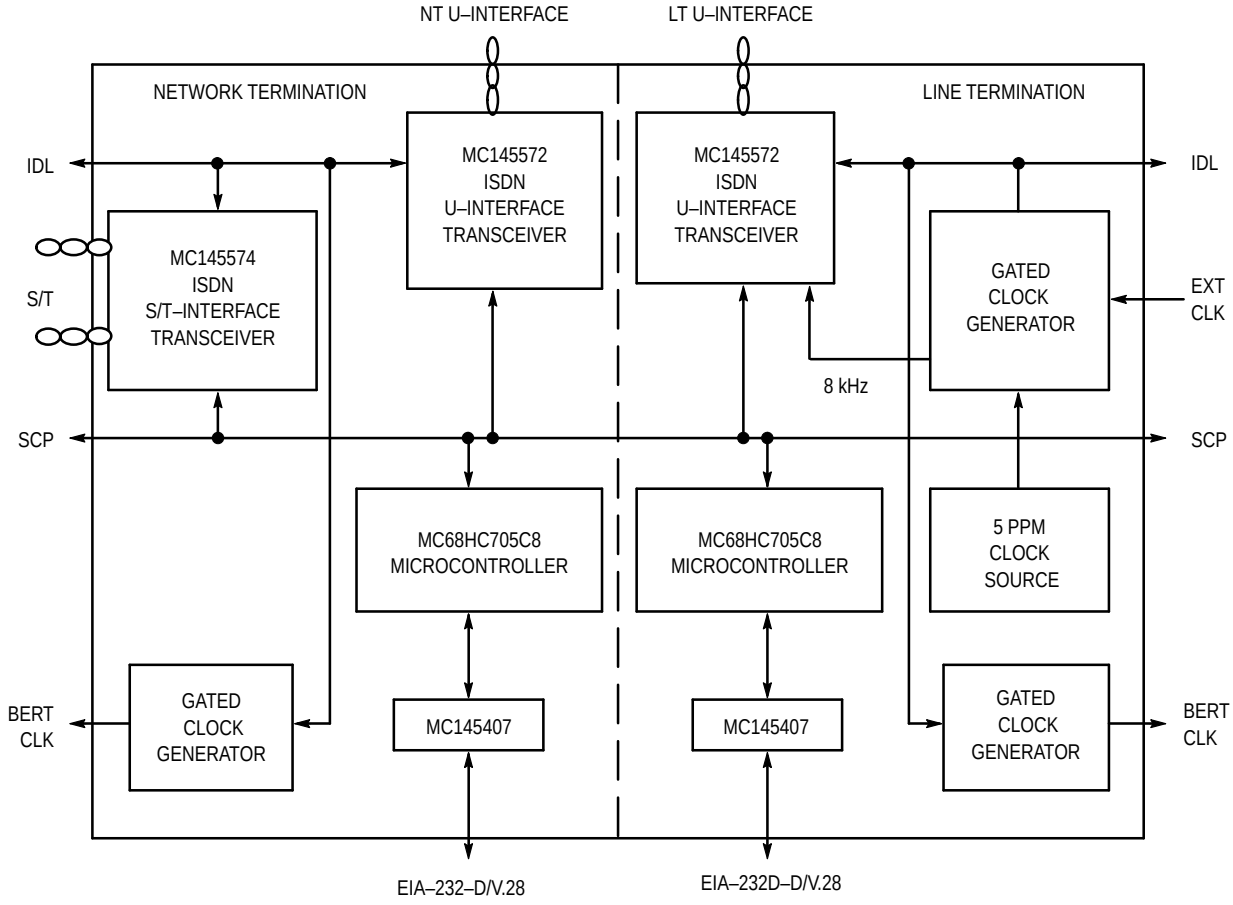

Figure 1. MC145572EVK Functional Block Diagram

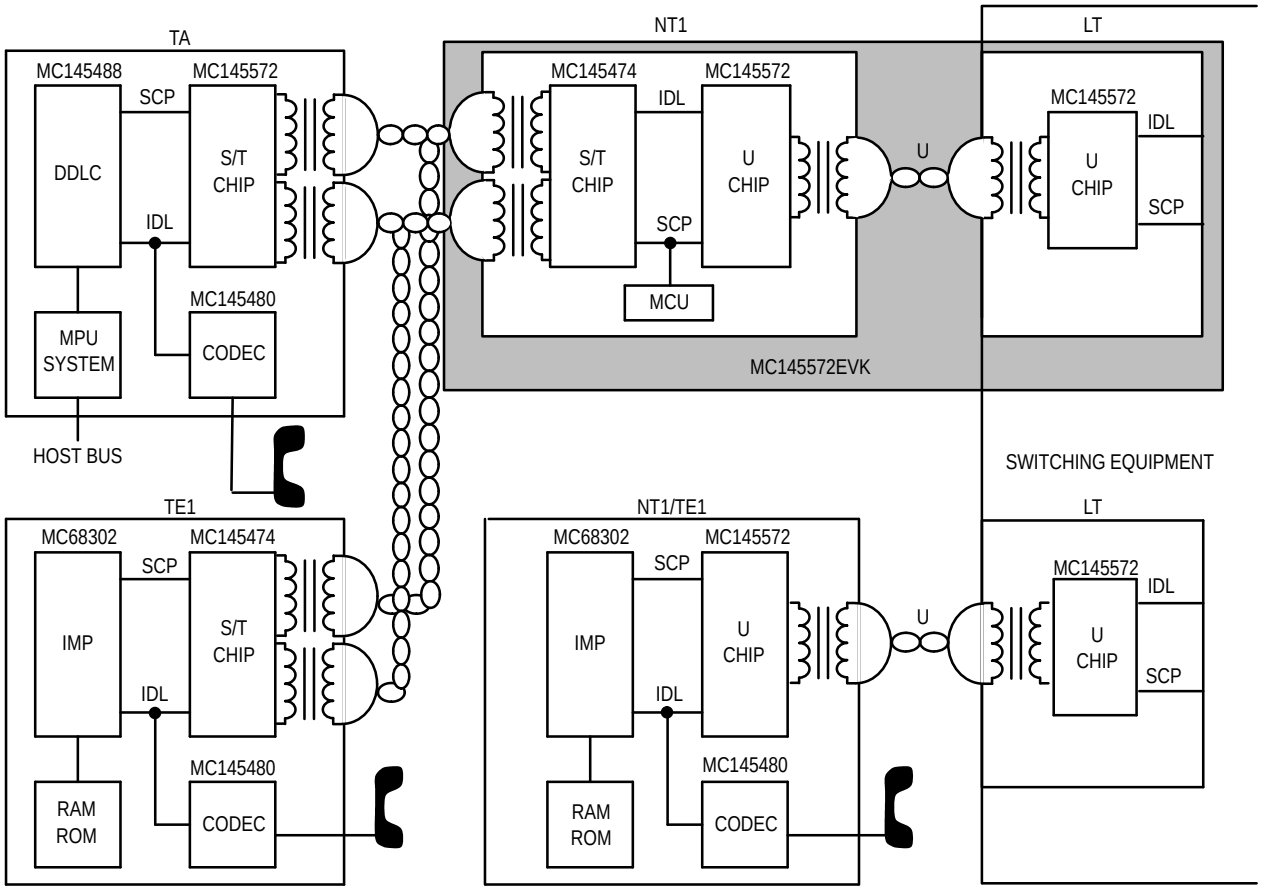

Figure 2. Motorola Silicon Applications and the MC145572EVK

MICROCONTROLLERS

The MC145572EVK is a MC68HC705C8 microcontroller–based system. Two microcontrollers reside on the board, U2 on the NT1 side, and U16 on the LT side. Hardware RESET push–buttons are located above each microcontroller. When the board is operating in the combined NT/LT mode, the NT1 and the LT are controlled via software residing in the NT1 side microcontroller EPROM. The monitor in the LT side microcontroller is used when the boards are physically separated and it becomes necessary to have one microcontroller to coordinate activities for each individual half. Both U2 and U16 must be populated for the display LEDs to operate properly.

The U–Interface may be activated using an ASCII terminal connected to the EIA–232 (V.28) port marked J3 on the NT1 side, when the board is together. When the board is separated, the EIA–232 connectors on both sides are used to monitor and control activities on their respective sides. Finally, the board may be activated as it “stands alone” with the push of a button. The default activation mode for the Activate/Deactivate push–buttons, PB1 and PB4 located near the front of the board, is as an NT1, with INFO1 continually transmitted on the S/T–Interface until it receives INFO2. When DIP switch S3–3 is in the NT1DIS position, the NT1 functionality is disabled. The LT side initiates activation on the U–Interface. Eight status LEDs are continuously updated by the MC68HC705C8s to provide the user a visual update of the U–Interface activation status.

NOTE

The LT side microcontroller (U16) must remain populated to guarantee proper operation of the LT NR1 status LEDs. The firmware version for U2 and U16 must be the same.

When the MC145572EVK is reset, it defaults to NT1 function enabled and automatic handling of M4 maintenance channel on the LT side U–transceiver. The NT1 function can also be disabled by entering the “NOF” command. The LT maintenance can be disabled by entering the “LOF” command.

STATUS LEDs

Fifteen status LEDs are provided on the MC145572EVK to offer the user a quick visual update to critical status parameters.

Two red LEDs, D12 on the NT1 side and D38 on the LT, are located near the power connectors and are illuminated when + 5 V is applied to the board. D12 indicates power is being applied to the NT1 side of the board while D38 indicates power is being applied to the LT side.

One green LED (D34) marked S/T ACT located near the S/T–Interface Transceiver, U10, illuminates to indicate that

the MC145474 when configured as an NT has achieved frame synchronization.

Located on both sides of the board are four LEDs representing Nibble Register 1 (NR1) of each U–Interface Transceiver. The LEDs in each bank are each marked with LINKUP, EI, SFS, and TP/AIP. They map directly to the register contents as shown below:

	b3	b2	b1	b0
NR1	Linkup	Error Indication	Superframe Sync	Transparent/ Activation in Progress
LED Silkscreen	LINKUP	EI	SFS	TP/AIP

NOTE

The received data is not transmitted on the IDL Interface until Linkup is a one, SFS is a one, TP/AIP is a one, and either CustEn (see NR2 in MC145572 U–Interface Transceiver data sheet) or VerifAct is a one (see BR9 in MC145572 U–Interface Transceiver data sheet).

Two red LEDs, D10 and D11 on the NT1 side, are located in the lower left corner of the printed circuit board. They indicate the status of the OUT1 and OUT2 pins of the MC145572 when it is configured for GCI operation.

Two red LEDs, D36 and D37 on the LT side, are located in the lower right corner of the printed circuit board. They indicate the status of the OUT1 and OUT2 pins of the MC145572 when it is configured for GCI operation.

COMMAND SET

A summary of the MC145572EVK software command set:

ACT: Activation/Deactivation Menu

BRL: Read/Write LT U–Interface Transceiver Byte Register

BRN: Read/Write NT U–Interface Transceiver Byte Register

BRS: Read/Write S/T–Interface Transceiver Byte Register

BRT: Read/Write S/T–Interface Transceiver Byte Register, Alternate Form

CLR: Clears febe/nebe, Re–Enters BR4 and BR5 in Both LT and NT Side U–Transceivers

DEA: Activation/Deactivation Menu, Alternate Form

DIS: Display Formatted Registers

EOC: Embedded Operations Channel Menu

HEL: Help Menu

LOF: Disable LT M4 Handler

LON: Enable LT M4 Handler

LPU: U–Interface Transceiver Analog Loopback

MM: Modify Memory

NOF: Disable NT1

NON: Enable NT1

NRL: Read/Write LT U–Interface Transceiver Nibble Register

NRN: Read/Write NT U–Interface Transceiver Nibble Register

NRS: Read/Write S/T–Interface Transceiver Nibble Register

NRT: Read/Write S/T–Interface Transceiver Nibble Register, Alternate Form

ORL: Read/Write LT U–Interface Transceiver Overlay Register

ORN: Read/Write NT U–Interface Transceiver Overlay Register

RES: Reset S/T– and/or U–Interface Transceivers

LOOPBACK OPTIONS

The activate command provides five different points on the MC145572EVK board where loopbacks are permitted when one or both U–Interface Transceivers are activated. At any given time only one loopback point can be enabled. This permits user equipment to be connected to the opposite side of the MC145572EVK. For example, if a loopback is selected on the NT1 half of the board, user equipment can be connected to the IDL Interface on the LT side of the MC145572EVK.

The LT side U–Interface Transceiver can be activated with 2B+D loopback to the U–Interface. This mode enables the received digital data from the U–Interface to be looped back to the LT side U–Interface Transceiver transmitter, and re–transmitted onto the U–Interface. The loopback point occurs in the IDL Interface block internal to the U–Interface Transceiver.

The LT side U–Interface Transceiver can also be activated without any loopbacks initially enabled. A loopback is then implemented simply by shorting JP26–21 to JP26–23.

The NT1 side U–Interface Transceiver can be activated with 2B+D loopback enabled in the S/T–Interface Transceiver IDL Interface. Received data from the NT1 side U–Interface Transceiver is transmitted on the IDL Interface to the S/T–Interface Transceiver where it is looped back to the IDL Interface and re–transmitted by the NT1 U–Interface Transceiver towards the U–Interface.

The NT1 side U–Interface Transceiver can be activated with the S/T–Interface Transceiver disabled. This causes the S/T–Interface Transceiver to three–state its IDL Interface transmitter. This provides the NT1 side U–Interface Transceivers IDL Interface direct access to the NT1 side IDL Interface. This permits the user to connect their own equipment to the NT1 side IDL Interface without any possibility of bus contention with the S/T–Interface Transceiver.

The NT1 side U–Interface Transceiver can also be activated without any loopback. This permits the NT1 side U–Interface Transceiver to communicate with the S/T–Interface Transceiver over the IDL Interface. A loopback is implemented by shorting JP7–21 to JP7–23.