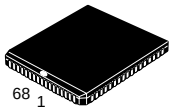
MC145488

Technical Summary
Dual Data Link Controller



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This technical summary gives a brief overview of the MC145488 Dual Data Link Controller. The MC145488 is a two–channel ISDN LAPD controller with an on–chip direct memory access (DMA) controller. It is intended for ISDN terminal and switch applications where one or two channels of data will use HDLC–type protocols. The DDLC can also be used in local area, wide area network, and bridge router applications. Each serial interface can be clocked at data rates up to 10 Mbps. The DDLC can operate with microprocessors using clock frequencies up to 20.5 MHz.

The DDLC is ideally suited for use with the MC145474 S/T–Transceiver. The interchip digital link (IDL) easily connects the chips together, providing a powerful layer one/layer two ISDN solution. A serial control port is provided to efficiently control the MC145474 or other ISDN family devices. The DDLC is compatible with 68000 and 80186 bus structures.

NOTE

This document is a summary of principal features and operation of the DDLC. Please refer to the MC145488 DDLC data book for the complete description and electrical specifications. It can be ordered from your local Motorola sales office or from the Motorola Literature Distribution Center as MC145488/D.

- Two Independent Full–Duplex Bit–Oriented Protocol Controllers Support HDLC, SDLC, CCITT X.25, CCITT Q.921 (LAPD), and V.120 at Basic and Primary Rates
- Four–Channel On–Chip DMA Controller
  - — 64 kbyte Address Range with Expansion Control
  - — Internal Programmable Wait–State Generator
  - — Two Buffer Descriptors for Each Receiver Channel
- Compatible with 68000 and 80186 Bus Structures
  - — Non–Multiplexed 16– or 8–Bit Data Bus
  - — Frame Sizes up to 4096 bytes
- Bit–Level HDLC Processing Including:
  - — Flag Generation/Detection
  - — Abort Generation/Detection
  - — Zero Insertion/Deletion
  - — CRC–CCITT Generation/Checking
  - — Residue Bit Handler
- TEI/SAPI Address Comparison
  - — Three Address Comparisons
  - — Wildcard Bits for Block Comparisons
- Transparent Mode for Codec Compatibility
- Programmable Interrupt Vector Generation
- Two Independent Timers Configurable as a Watchdog Timer
- Flexible Serial Interface with:
  - — IDL Interface for Connection to Other ISDN Family Devices
  - — Timeslot Interface for Connection to PBX–Type Backplanes
  - — Modem Interface for Other Applications
- Supports CCITT Specification 1.460
- Supports DMI Specification 3.1 Modes 0, 1, 2, and 3
- Serial Control Port for ISDN Family Device Control
- Low–Power CMOS with Automatic Power–Down
- Serial Data Rates up to 10 Mbps
- DDLC Master Clock up to 20.5 MHz

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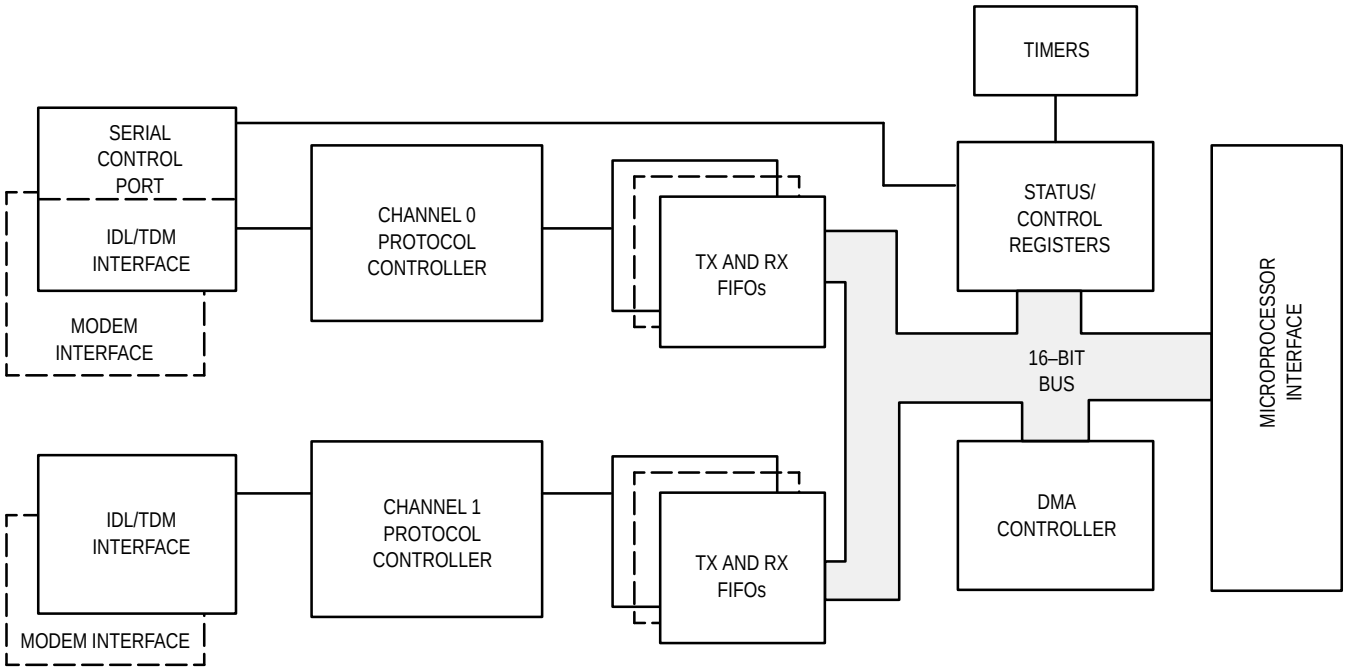
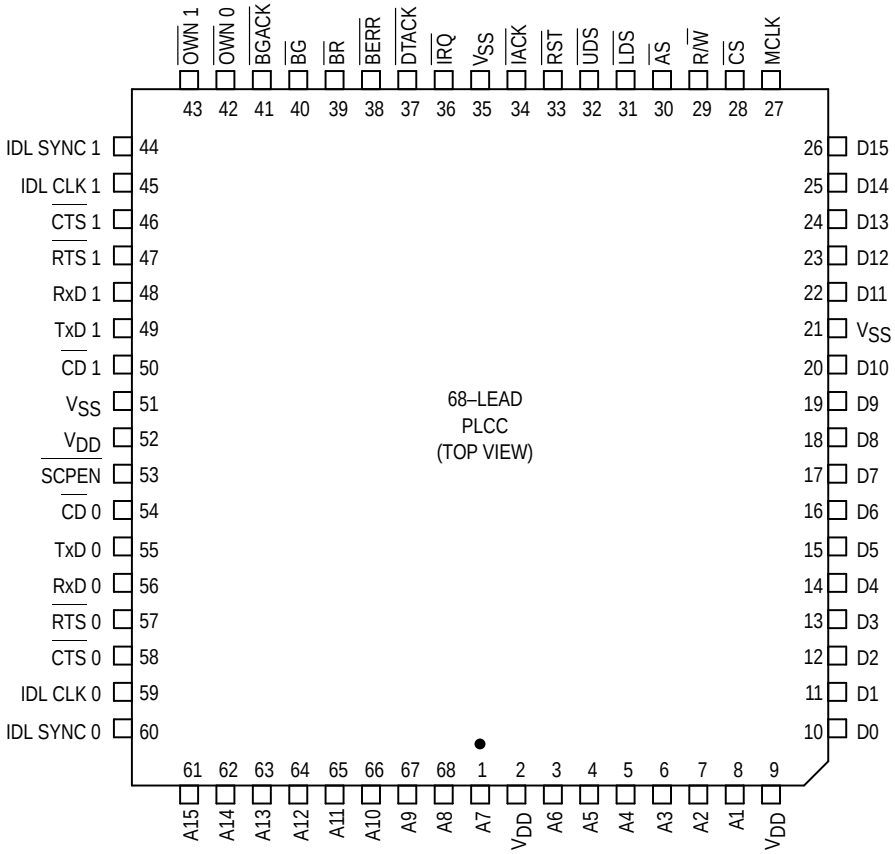
BLOCK DIAGRAM



PIN ASSIGNMENT



GENERAL DESCRIPTION

DDLC OVERVIEW

The MC145488 Dual Data Link Controller (DDLC) is a high–performance two–channel protocol controller with an on–chip direct memory access controller (DMAC). Each channel has a full–duplex transceiver with independent protocol controllers to handle the bit–level tasks of HDLC–type bit–oriented protocols, including LAPB and LAPD. Each channel also has dedicated DMA controllers for transmit and receive. A transparent mode is provided which bypasses the protocol circuitry so that serial data may be directly transferred between the host processor's memory and the serial interface. The DDLC's microprocessor interface is configurable to 68000 or 80186 systems and may be used in 8–bit or 16–bit bus modes. The DDLC's master clock can be obtained from microprocessor clocks up to 20.5 MHz.

Each channel has a serial data interface which operates up to and above T1 or E1 primary rate speeds in three modes: IDL, Timeslot, and Modem. In the IDL (Interchip Digital Link) mode for ISDN applications, the IDL bus is supported. When in the IDL D channel mode, the DREQ and DGRNT access control lines to the ISDN D channel, through the MC145474 S/T transceiver, are enabled. The timeslot mode is used to connect the DDLC to PBX–type PCM highway backplanes. Both long–frame and short–frame timing are supported as well as synchronous transmit and receive. In the modem mode, each channel has its own separate transmit and receive clock inputs along with modem control lines (RTS, CTS, and CD). The two channels are independent and may be in different interface modes.

A serial control port (SCP) is provided to pass control information to other devices in a system. The SCP is compatible with Motorola's Serial Peripheral Interface (SPI) and National Semiconductor's MICROWIRE™ Plus. Two internal timers may be used for general purpose, low resolution timing of HDLC–type protocols. One of the timers may be configured as a watchdog timer to reset the entire system in the event of a hardware or software failure.

Power consumption is an important aspect of ISDN terminal designs, and the DDLC was designed to use the minimum power possible while maintaining maximum functionality. The DDLC keeps power consumption to a minimum with an automatic power–down feature that turns off sections of circuitry that are not being used. Only those circuits that are actually used (e.g., when the CS pin is activated for a register read/write or when the DMA controller performs a bus transaction) enter the normal power state for the duration of the access and for any time required for internal processing.

Two internal loopback functions and special chip and system test modes are available. The loopbacks are controlled by the host for on–line maintenance. The test modes are activated by bits in the master control register and provide access to the internal state machines.

HDLC PROTOCOL OVERVIEW

HDLC (High–Level Data Link Control) and its descendants, LAPB (Link Access Protocol–Balanced) and LAPD (Link Access Protocol for the D channel), are bit–oriented synchronous protocols which are widely used in data communications systems. LAPB and LAPD share the basic format of HDLC but differ in minor aspects (see Figure 1).

In the packet mode, the DDLC transmits and receives data in a format called a frame or packet. All frames start with an opening flag and end with a closing flag. Between the flags, a frame contains an address field, control field, information field, and a cyclic redundancy check field (CRC).

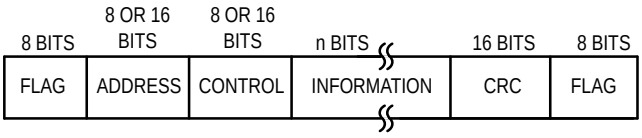


Figure 1. HDLC Frame Format

Flag

The flag is the unique binary pattern (01111110). It provides the frame boundary and a reference for the position of each field of the frame.

Address Field

The 8 or 16 bits following the opening flag comprise the address field. The address field is used to distinguish between the various devices in a network. The DDLC has address recognition circuitry included, which relieves the host from this task.

Control Field

The 8 or 16 bits following the address field are the control field. Commands and responses between the devices in a network are exchanged in this field.

Information Field

This field follows the control field and precedes the CRC field. The information field contains the data to be transferred and may be a null field.

Cycle Redundancy Check Field

The 16 bits preceding the closing flag are the Cycle Redundancy Check (CRC) field. This field detects bit errors in the address, control, and information fields. Checking is with the standard CCITT polynominal $x^{16} x^{12} x^5 + 1$ for both the transmitter and receiver. The transmitter calculates the CRC on all bits of the frame (except for the flags) and transmits the complement of the resulting remainder as the CRC field. The receiver performs the similar computation on all bits (except for the flags) and compares the result to F0B8.

Zero Insertion and Deletion

Zero insertion and deletion, which allows the content of the frame to be transparent, is automatically performed by the DDLC. A binary 0 is inserted by the transmitter after any succession of five 1s within a frame (between flags). This eliminates the possibility of data imitating a flag character. The receiver deletes all 0s that were inserted by the transmitter to regenerate the original data.

Abort

The function of prematurely terminating a data frame is called an abort. The transmitter aborts a frame by sending between seven and fourteen consecutive 1s. When the receiver detects an abort character, it responds by clearing the FIFO and clearing the buffer in memory. It then begins searching for a new frame.

In–Frame, Inter–Frame Time Fill, and Idle

For LAPB and other applications, there are three states that the data link may be in: in–frame, inter–frame time fill, and idle. In–frame is the period from the beginning of an opening flag and the end of a closing flag. Inter–frame time fill is the period between frames when continuous flags are transmitted. Idle is an out–of–frame period when continuous 1s are on the link. In LAPD, on the D channel, there are only two states: in–frame and idle. Continuous flags are not transmitted between frames.

BLOCK DIAGRAM DESCRIPTION

This section is a brief overview of the internal blocks of the DDLC. The blocks include two protocol controllers that handle the bit–level aspects of HDLC–like packet protocols and four FIFOs that buffer the data, a four–channel DMA controller, and a microprocessor interface block that connects the DDLC to the host system. Figure 3 is a simplified block diagram of the DDLC. While the DDLC has two data transceivers, only one is shown for simplicity.

TRANSMIT BIT HANDLER

Two identical bit–level protocol transmitters are provided which perform HDLC–type framing. This section describes the operation of only one transmitter, but it applies to both.

Packet Operation

The transmitter is designed to operate with as little intervention from the host processor as possible. To transmit a frame of data, the host merely informs the DDLC of the starting address of the data frame in memory and the length of the frame in bytes. The DDLC then transmits an opening flag and the data (LSB first) from memory. When the transmitter detects that the end of the data buffer has been reached, a CRC field and a closing flag are appended. The transmitter generates an abort character if the FIFO underruns. During inter–frame periods, the DDLC can be configured to transmit either continuous flags (7E hex) or continuous marks (FF hex).

State Diagram

Figure 2 is the state diagram for the transmitter in packet operation.

Abort

The DDLC can be configured to transmit a standard HDLC abort character. It can also transmit an abort character which is compatible with DMI 3.1 modes 2 or 3 for restricted B–channel applications. An abort character will be transmitted when the TX Fifo underruns, when the Force Abort bit is set in the Transmit Control Register, or when the CTS pin is deasserted.

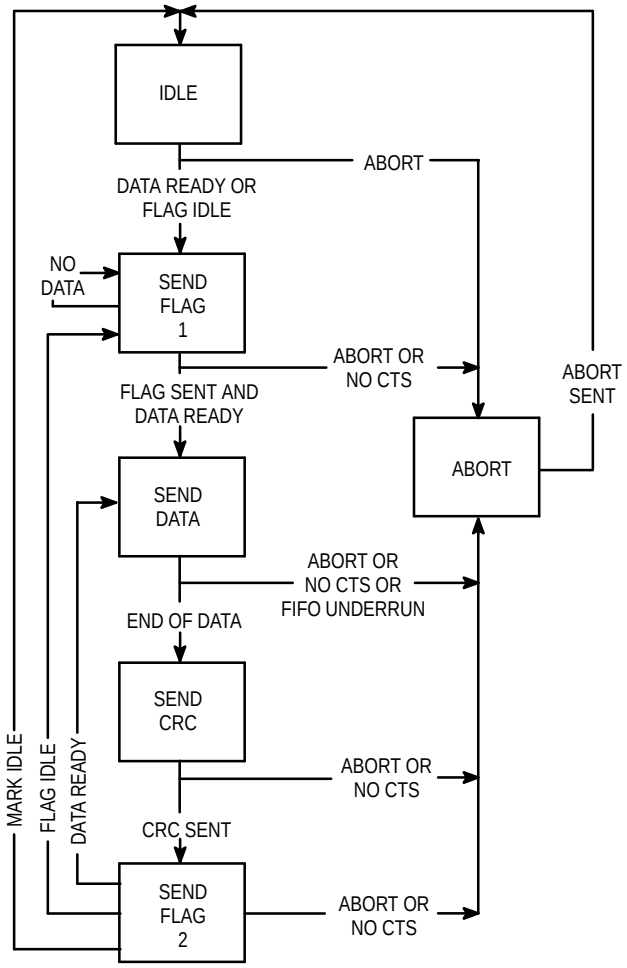


Figure 2. Transmitter State Diagram
HDLC Operation

Flow Control Mechanisms

The DDLC provides two flow control mechanisms: one for basic rate ISDN applications and the other for standard modem applications. The following paragraphs describe the operation of the two schemes.

ISDN D Channel Contention

When the DDLC is operating on the D channel with the companion MC145474 S/T transceiver, the DREQ and DGRNT lines must be used to comply with the basic rate D channel contention algorithm. When the DDLC has a data frame to transmit, it asserts DREQ (high). When DGRNT is detected high from the MC145474 transmission from the DDLC begins in the IDL D–bit time slots when DREQ and DGRNT are both active. If DGRNT is deasserted (goes low) in the middle of a frame, the DDLC automatically aborts the frame in progress and prepares to retransmit the entire frame when the D channel becomes available again. This is done without interrupting the host.

Modem Flow Control

The transmitter indicates to a modem that it has data ready to transmit with signals similar to D channel operation. In this mode, Request–To–Send (RTS) is directly controlled by the Transmit Enable (TE) bit. When TE is high, the RTS pin is asserted (low). During inter–frame periods, either flags or

marks (as selected) are transmitted but the $\overline{\text{RTS}}$ pin remains asserted until the user negates the TE bit. Transmission of a frame, if one is ready, actually begins when the modem asserts Clear–to–Send (CTS low). If CTS is negated for more than one Tx CLK period while a frame is in transmission, the frame is aborted and the DMA pointers are reset so that the frame can be retransmitted without interrupting the host.

Interrupts

There is one interrupt generated by the transmitter state machine. Transmit Frame Complete indicates that an entire frame and its closing flag have been successfully transmitted. Ordinarily, this interrupt is used for basic rate ISDN D channel operation. Two other interrupts associated with the transmitter are generated by the DMA controller and are discussed in the section describing the DMA controller.

Transmit FIFO

The transmitter has a FIFO which buffers it from the DMA controller. It is four characters deep and nine bits wide. The ninth bit is a Tag bit which is set when the the last byte of a frame is read from memory by the DMA controller. After the tagged byte, the DDLC sends a closing CRC and flag sequence.

Transparent Operation

The transmitter has the capability of operating with unframed data such as PCM–encoded voice or proprietary protocols. Raw data may be transmitted from memory with byte alignment maintained through the FIFO and transmitter. Byte alignment signals must be provided. In the modem mode, the alignment signal is externally generated. In IDL and timeslot operation, it is internally generated but user programmable. The DDLC transmits data continuously as long as there is data to transmit.

Inter–Frame Time Fill

The bit sequence that is transmitted between frames is determined by the value of the ITF bit in the Transmit Control register. The inter–frame time fill can be either the X.25 flag character (7E hex) or the LAPD marks (1) idle.

RECEIVE BIT HANDLER

The receiver provides the complementary functions to the transmitter. This section describes the operation of one receiver, but it applies to both receivers.

Packet Operation

The receiver is reset and idle until the Receive Enable bit is set, at which time it begins searching for a flag character. When a flag is found, the selected address field of the frame, if desired, is checked and if a match is found, the DDLC passes the frame of data to the allocated buffer in memory. If no address match is found, the DDLC clears the FIFO, resets the DMA pointers, and searches for a new frame. Zeros inserted by the transmitter are removed from the data before placing the bytes in memory. When the closing flag is detected, the CRC field is checked and if found to be correct, the DDLC queues an interrupt indicating that a good data frame has been received and is in memory. If the CRC is found to be in error, the DDLC automatically resets the buffer pointers to the start of the buffer and searches for a new frame.

Each receiver has two receive buffers, A and B. This permits one buffer to be actively receiving a frame while software is obtaining the data from and reinitializing the other buffer. If an incoming frame is longer than the length defined for the active receive buffer, the DDLC will switch to the second buffer if it is enabled.

If an abort character is found, the buffer pointers in the DMA controller are reset and the aborted frame is ignored. The FIFO is cleared and the receiver begins searching for a flag. No interrupt is generated.

State Diagram

Figure 4 shows the state diagram of the receiver.

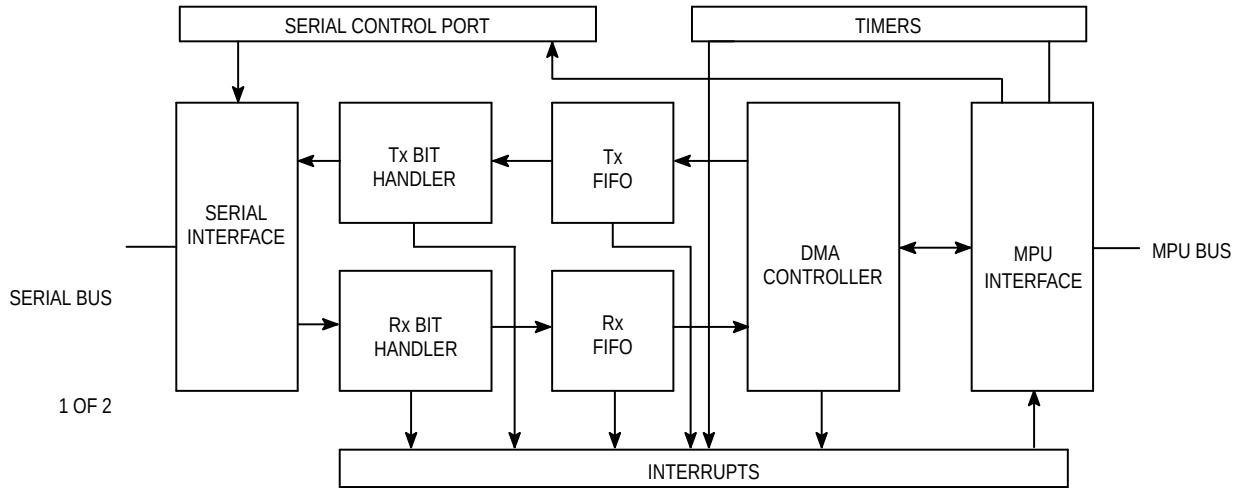


Figure 3. DDLC Block Diagram (One Transceiver Shown)

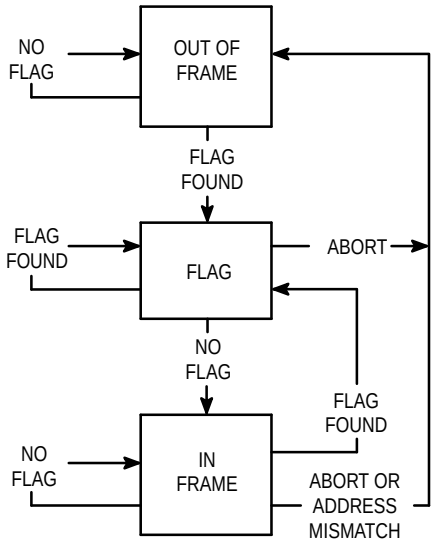


Figure 4. Receiver State Diagram HDLC Operation

Non–Octet Aligned Packets

The receiver has the capability of operating in non–octet aligned packet systems. The residue bit count indicating the number of orphan data bits at the end of the information field is placed in the RC bits of the Receive Status register. These bits are valid until overwritten by another frame. In non–octet aligned systems, the software should check the residue count soon after receiving a Receive Buffer Complete Interrupt to ensure that the residue count is not overwritten by the next frame. Orphan bits are LSB justified in memory. Note: The DDLC does not transmit non–octet aligned frames.

Address Recognition (Filtering)

The receiver can filter received frames by comparing their address fields to user programmable addresses. Two addresses may be programmed with another (broadcast, FF hex) hardwired into the receiver. Address filtering may be performed on either the first OR second octet following the opening flag of a frame. Typically, in ISDN terminal applications, the TEI address (second) field will be of interest. In network applications, the SAPI (first) field will be checked. A separate Wildcard register allows selected bits of Compare Address 0 to be ignored during the comparison procedure. If received frames are rejected by address recognition, the receiver is reset and searches for a new frame. Address recognition may be disabled by clearing the Address Compare Enable bit to 0.

Receive FIFO

The receiver has a FIFO that is similar to the transmitter's. It is four characters deep and ten bits wide (eight bits for data and two bits for the Tag). Serial bytes are produced by the receiver and converted to parallel. As each byte is formed, it is pushed into the FIFO. A comparator in the controller keeps track of the occupancy of the FIFO and requests that the DMA controller place a word of data (16 bits) in memory when there are two or more bytes in the FIFO. In 8–bit operation, the FIFO requests service when one or more bytes of data read are ready to be placed in memory. If the FIFO overruns because the DMA controller did not service a request, an interrupt is queued. When a receiver is operating at 64 kbps in the 16–bit mode, DMA requests from that FIFO occur at approximately 250 μs intervals.

Transparent Operation

The DDLC receiver provides a transparent operation mode for passing raw octet–aligned serial data to memory via DMA. This feature is useful for storing PCM voice or proprietary protocols in memory. When using the DDLC to pass PCM voice to memory, maximum buffer size of 4096 bytes should be used. The Receive Buffer Overrun Interrupt is used in conjunction with Receive Buffers A and B that are available for each channel when transparent mode is used. Because the transparent mode requires that data be in eight–bit quantities, synchronization procedures for defining octet boundaries are required. In the modem mode, the sync signal is externally generated and input on the CD pin. In IDL mode timeslot operation, the sync signal is internally generated but user programmable. Once byte alignment is obtained in the receiver, it is maintained through the DMA controller into memory.

Interrupts

There are two interrupts generated by the receiver. The receiver queues an interrupt when a frame has been successfully received. The receive idle interrupt indicates that 15 or more consecutive 1s were received. This interrupt is considered normal operation. The current status of receive idle and carrier detect is available in the Receive Status register, but the user must remember that they can change immediately after being read. The carrier detect pin also generates an interrupt when it changes state.

DMA CONTROLLER

In order to relieve the host software from critically timed data transfers to or from the protocol controllers, the DDLC provides four DMA channels, one for each transmitter and receiver.

DMA Operation

When the DMA controller detects a service request from one of the FIFOs, it prepares the address and data from the transfer then requests ownership of the system bus from the host. When ownership is granted, the DMA controller assumes control of the bus and transfers data either to or from memory. Transfers are 16 bits or 8 bits, depending on the selected bus width. When the number of bytes in a received frame is odd, the last byte is placed in the most significant byte of the last word. The least significant byte contains unknown data. The receive byte count contains the correct number of bytes received (including the CRC). When odd length frames are transmitted, the last word read from memory has the last byte transmitted in the most significant byte, and the least significant byte of that word is discarded.

The DMA controller uses a round robin strategy to service internal DMA requests. A channel that was just serviced is not polled again until all other channels have been polled and serviced, if needed. The DDLC services one DMA request per bus arbitration cycle. The DDLC does not perform burst DMAs, so other devices can have access to the microprocessor bus. This type of operation improves system performance and guarantees that the DDLC is well behaved.

It is impossible to precisely predict what the DDLC bus occupancy will be, but worst case with both channels operating full–duplex at 64 kbps (aggregate rate of 256 kbps) in a 16–bit 68000 system with a 12 MHz MCLK, approximately 0.66% of the host bus bandwidth is consumed by the DDLC. Bus occupancy increases linearly with data rate. At very high data rates, latency from the bus request to the bus grant and interrupt service latency become the limiting factors. It must also be kept in mind that the DDLC can generate interrupts quickly, especially with a large number of small data packets at a high clock rate.

Buffer Descriptors

As previously stated, the DDLC has four DMA channels. Pointer registers and counters are required so that the DMA controller knows where to place or fetch data in memory.

Transmit Buffer Descriptors

When the host has a frame of data to transmit, it informs the DMA controller where the data resides in memory. A 16–bit register, the Transmit Base Address register, points to the first word of the transmitted frame and provides a 64 kbyte address range. The host programs the address of the first word to be transmitted into this register. The length of the data frame must also be given to the DMA controller, so a 12–bit Transmit Frame Length register is used to indicate the length of the frame in bytes. Frames of up to 4096 bytes in length may be transmitted.

Back to back frames can be transmitted by updating the transmit buffers when the Transmit DMA Complete interrupt is generated.

NOTE

Once a transmit buffer descriptor has been prepared, it must not be disturbed until the transmit DMA complete or transmit frame complete interrupts are generated.

Receive Buffer Descriptors

The receive buffer descriptors have a 16–Bit Receive Buffer Base Address register, a 12–Bit Buffer Length register, and a 12–Bit Frame Length register. The 16–Bit Base Address register provides 64 kbyte address range and contains the address of the first word of the data buffer to accept a data frame. The 12–Bit Frame Length register indicates the length of the memory buffer in bytes. Buffers of up to 4096 bytes may be built. The DMA controller never places data outside of the boundaries set–up by these two registers. The Frame Length register indicates the number of bytes (including the CRC) received.

Each channel has a pair of buffer descriptors. These may be used alternately so that while one buffer is filling, another buffer is ready–in–waiting. If back–to–back data frames are received, after the first buffer has been closed the second is immediately ready for the next frame. There must be at least one buffer ready to accept data when the Rx Enable bit is set. Figure 6 describes the activity of the receiver with four buffers in memory.

If a packet is being received and no buffers are ready, the receive FIFO will overrun, the Receiver Enable bit is reset, and an interrupt is queued indicating the overrun. If both descriptors are ready, then Buffer A is filled first. If a received frame is larger than a buffer, the Buffer (A or B) Overrun Interrupt is queued, but the receiver continues to receive and the DMA controller places the data in the alternate buffer (if it is available). If an alternate buffer is not ready, the Rx FIFO Overrun Interrupt is generated and the receiver is reset.

Once a data frame has been completely received, the number of bytes received is indicated in the Frame Length register. The number in this register is valid only when the Receive DMA Complete bit (Buffer A or Buffer B) in the Receive Status register is set to ‘1’.

NOTE

As with the transmitter, once a receive buffer descriptor has been prepared, it must not be disturbed until the closing flag has been found and DMA activity on the buffer has stopped.

Address Expansion

The DDLC provides signals for expansion of the 64 kbyte address space. The OWN pins are activated with timing identical to the address pins to enable external address expansion circuitry onto the address bus. Using the OWN pins with the R/W pin, the transmit and receive buffers may all be on separate 64 kbyte pages in memory.

Transmit Channel Operation

Figure 5 is a simplified state diagram of the DMA controller’s operation when a transmit channel requests service.

Four interrupts are produced by the transmitter DMA channel. Transmit DMA Complete indicates that the last byte of data has been transferred from the buffer into the transmit FIFO. FIFO Underrun indicates the DMA requests were not serviced and the FIFO underran. Bus Error is generated when the BERR pin is activated during a DMA cycle. Address Error is generated when either IACK or CS are activated during a DMA cycle.

Receive Channel Operation

Figure 7 is a simplified state diagram for operation of the DMA controller when a receive channel requests service.

MICROPROCESSOR INTERFACE

The microprocessor block interfaces the internal 16–bit bus to the host 8– or 16–bit bus. The block also performs all timing conversion and buffering. This block has three modes of operation described in this section: system slave, system master, and interrupt generator.

System Slave Mode

When the DDLC is in this mode, it appears as fast memory to the host processor. The host can read from or write to the registers in the DDLC. This mode is entered when the CS pin is activated. Internal address decoding circuitry is selected and the desired register is connected to the internal bus for access by the host.

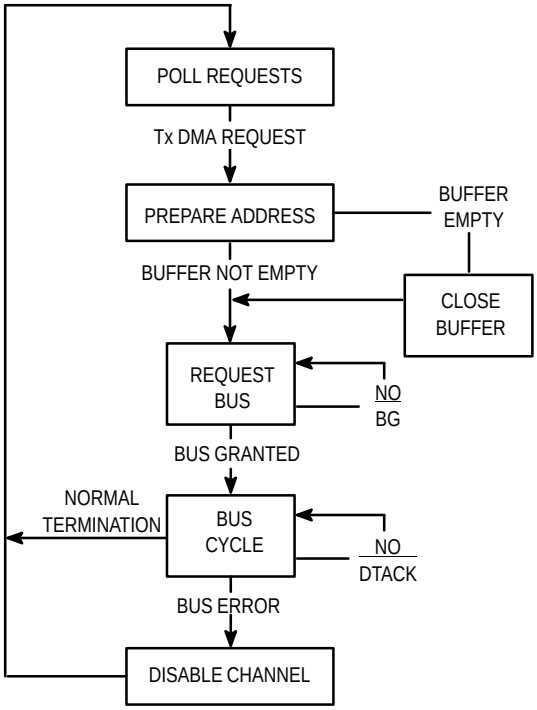


Figure 5. Transmit DMA State Diagram

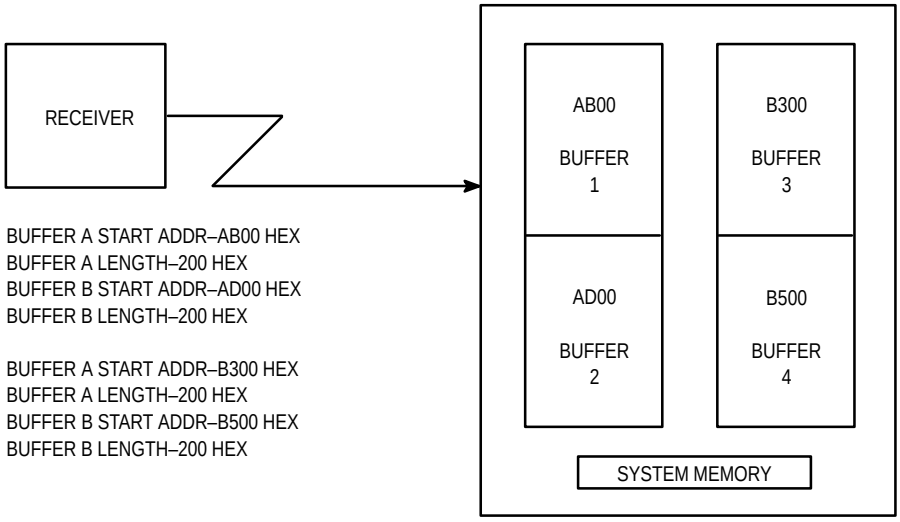


Figure 6. Alternate Receive Buffer Operation

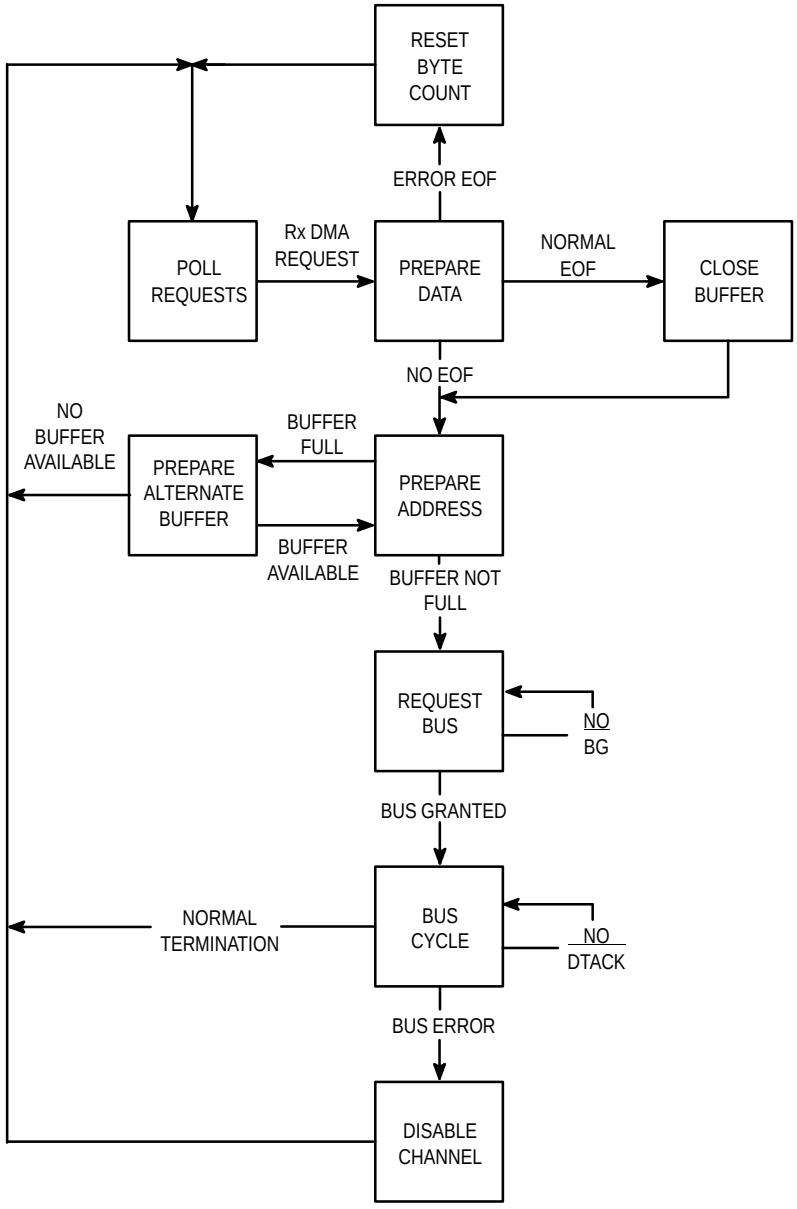


Figure 7. Receive DMA State Diagram

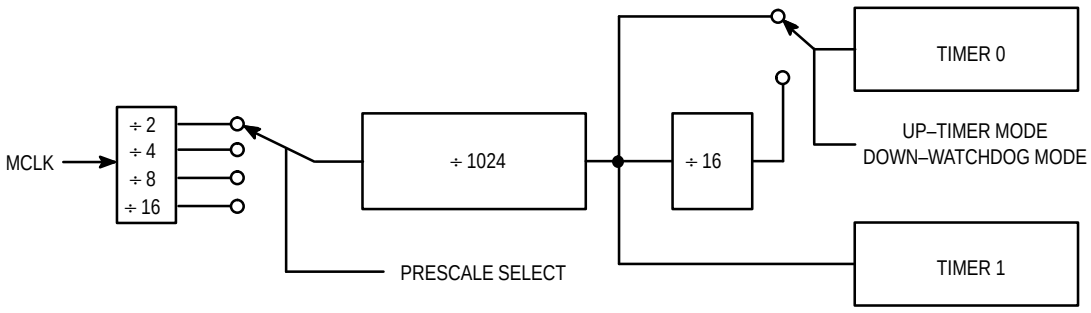


Figure 8. Timer Clock Selection

System Master (DMA) Mode

During DMA operation, the DDLC becomes a system master and controls the system bus. When one of the internal FIFOs requests a DMA transfer, the DDLC negotiates with the system host for ownership of the bus. After successful negotiation, one DMA request is serviced, and then the bus is relinquished. The DDLC has the capability of reading or writing data from or to memory. If the memory system is slow, the DDLC inserts wait states (user selectable) until the memory is ready to complete the access. The DDLC has the capability of recovering from system faults such as address or bus errors.

Interrupt Operation

The DDLC has 27 vectored interrupt sources to inform the host of its status. One group of interrupts is normal operation interrupts. These inform the host that a particular task was completed and that new tasks are desired. Another group is bit handler faults, which inform the host that a DDLC channel detected a fault from which it cannot recover without assistance from the host. A third group is the timer and SCP interrupts. The last group of interrupts is the system faults. These include DMA bus and address errors. The interrupts are presented to the host as a vector number in an interrupt acknowledge cycle. The interrupts are encoded into the low four bits so the DDLC vector space consumes 16 out of 256 locations. Software can program the base vector number, so the DDLC vectors can be located anywhere within the vector table. For applications not using vectored interrupts, the equivalent vector number is accessible in the Master Status register.

SERIAL INTERFACE

The serial interface block has a variety of configurations that make it compatible with most common interfaces. Each serial interface is independent, so two different configurations may be active simultaneously. The serial interface has an IDL mode, a timeslot mode, and a general purpose modem mode. The serial interface supports long frame and short frame timing. It also supports subrate multiplexing. The serial mode is selected by programming the appropriate bits in the Serial Interface Control register.

A full set of serial interface control and handshake pins are provided. The name and functionality change to reflect the serial mode of operation. Separate receive and transmit clock inputs are provided for all modes except IDL and timeslot modes.

The serial interface also supports transfer of transparent data. Depending on which type of serial interface is used, an external synchronization signal must be provided to maintain byte alignment. In IDL mode, the byte synchronization is programmed by the microprocessor.

SERIAL CONTROL PORT

A Serial Control Port, similar to the Serial Peripheral Interface (SPI) on Motorola single–chip microprocessors, is provided to communicate with external devices via a serial link. The SCP functions are multiplexed onto other serial pins so when the SCP is enabled, certain modem control features are lost. Please refer to the MC145488/D Data Book for complete details.

TIMERS

Two timers are provided for general purpose low–resolution protocol uses. The clock to the timer is derived from the Master MPU Clock (MCLK). The baud rate generator in the SCP block is used to drive the timer divide chain. This clock is then divided by 1024 and applied to an eight–bit down–counter. The counter is readable and writable by the host and may be set to any value. The counter counts down toward zero from the current value. A non–maskable interrupt is generated when the counter underflows from FF to FE. The timers continue counting down after reaching FE. The status bit from the previous interrupt must be cleared before a new interrupt is generated. The timer function and interrupt are enabled by setting the Timer Enable bit in the Timer register to one. The timer interrupt status bits must be read while set before they can be cleared. The timers are intended for low accuracy uses such as protocol timers. Figure 8 describes the clock selection choices for the timers.

Watchdog Timer

Timer 0 may be configured as a watchdog timer for the entire host system. When the Watchdog Enable bit is set, an extra divide–by–16 is added to the clock input of the counter. When the counter underflows from FF to FE, the Reset pin becomes an output for 16 MCLK cycles and a logic low is output. This provides a system reset to the host. The host can write any value (except FE hex) to the Timer register to setup any timeout. Timeouts of up to 5.6 seconds are available with a 12 MHz MCLK.

POWER CONSUMPTION

The DDLC is designed utilizing high–performance CMOS technology. As as result, average power consumption is very low. However, because there are wide address and data buses, peak currents may exceed 150 mA for short periods of time (less than 20 ns) while the drivers are charging or discharging the buses.

REGISTER SET

The DDLC has many user accessible registers. These registers control the blocks or indicate status. Other registers, used by the DMA section, are used as buffer descriptors and counters. For a more detailed description, please refer to the DDLC data book. The address for each register is the hexadecimal offset from the base address of the chip select. The registers may be accessed as 8–bit registers or 16–bit registers. Table 1 is a map of the registers and their principal function.

Table 1. Register Memory Map

00	SYSTEM CONTROL	
02	MASTER STATUS	
04	INTERRUPT ENABLE	
06	DATA BUS SIZE SELECT	
10	SCP REGISTER	
12	CH 0 TIMER	
14	CH 1 TIMER	
20	CHANNEL 0 SERIAL INTERFACE CONTROL	CHANNEL 0 REGISTERS
22	CHANNEL 0 Tx CONTROL	
24	CHANNEL 0 Rx CONTROL	
26	CHANNEL 0 Tx STATUS	
28	CHANNEL 0 Rx STATUS	
2A	CHANNEL 0 ADDRESS COMPARE	
2C	CHANNEL 0 ADDRESS WILDCARD BITS	
2E	CHANNEL 0 CRC ERROR COUNT	
30	CHANNEL 0 Tx FRAME LENGTH	
32	CHANNEL 0 Tx BASE ADDRESS	
34	CHANNEL 0 Tx BYTE COUNT	
36	CHANNEL 0 Rx BUFFER LENGTH	
38	CHANNEL 0 Rx BUFFER A BASE ADDRESS	
3A	CHANNEL 0 Rx BUFFER A BYTE COUNT	
3C	CHANNEL 0 Rx BUFFER B BASE ADDRESS	
3E	CHANNEL 0 Rx BUFFER B BYTE COUNT	
40	CHANNEL 1 SERIAL INTERFACE CONTROL	CHANNEL 1 REGISTERS
42	CHANNEL 1 Tx CONTROL	
44	CHANNEL 1 Rx CONTROL	
46	CHANNEL 1 Tx STATUS	
48	CHANNEL 1 Rx STATUS	
4A	CHANNEL 1 ADDRESS COMPARE	
4C	CHANNEL 1 ADDRESS WILDCARD BITS	
4E	CHANNEL 1 CRC ERROR COUNT	
50	CHANNEL 1 Tx FRAME LENGTH	
52	CHANNEL 1 Tx BASE ADDRESS	
54	CHANNEL 1 Tx BYTE COUNT	
56	CHANNEL 1 Rx BUFFER LENGTH	
58	CHANNEL 1 Rx BUFFER A BASE ADDRESS	
5A	CHANNEL 1 Rx BUFFER A BYTE COUNT	
5C	CHANNEL 1 Rx BUFFER B BASE ADDRESS	
5E	CHANNEL 1 Rx BUFFER B BYTE COUNT	