MC14526B

Presettable 4-Bit Down Counters

The MC14526B binary counter is constructed with MOS P–channel and N–channel enhancement mode devices in a monolithic structure.

This device is presettable, cascadable, synchronous down counter with a decoded "0" state output for divide–by–N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide–by–N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

This complementary MOS counter can be used in frequency synthesizers, phase–locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge–Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

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MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
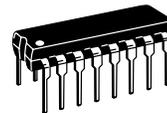   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq$ (V_{in} or V_{out}) $\leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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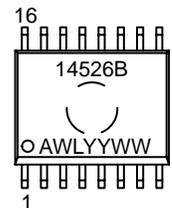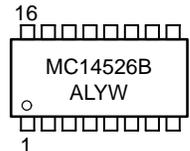## PIN ASSIGNMENT

Q3	1 ●	16	V_DD
P3	2	15	Q2
PE	3	14	P2
INHIBIT	4	13	CF
P0	5	12	"0"
CLOCK	6	11	P1
	7	10	RESET
V_SS	8	9	Q1
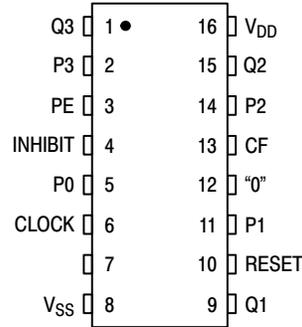
FUNCTION TABLE

Inputs					Output	Resulting Function
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	
X	H	X	L	L	L	Asynchronous reset*
X	H	X	H	L	H	Asynchronous reset
X	H	X	X	H	H	Asynchronous reset
X	L	X	H	X	L	Asynchronous preset
⌐	L	H	L	X	L	Decrement inhibited
L	L	⌐	L	X	L	Decrement inhibited
⌐	L	L	L	L	L	No change** (inactive edge)
H	L	⌐	L	L	L	No change** (inactive edge)
⌐	L	L	L	L	L	Decrement**
H	L	⌐	L	L	L	Decrement**

X = Don't Care

NOTES:

 * Output "0" is low when reset goes high only it PE and CF are low.

** Output "0" is high when reset is low, only if CF is high and count is 0000.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ [4.]	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	— — — —	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	— — — —	−1.7 −0.36 −0.9 −2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance ($V_{in} = 0$)	C_{in}		—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15				$I_T = (1.7\ \mu A/kHz)\ f + I_{DD}$ $I_T = (3.4\ \mu A/kHz)\ f + I_{DD}$ $I_T = (5.1\ \mu A/kHz)\ f + I_{DD}$				µAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ [8.]	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL} (Figures 4, 5)	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time (Inhibit Used as Negative Edge Clock) Clock or Inhibit to Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns	t_{PLH}, t_{PHL} (Figures 4, 5, 6)	5.0 10 15	— — —	550 225 160	1100 450 320	ns
Clock or Inhibit to "0" t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 155 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		5.0 10 15	— — —	240 130 100	480 260 200	
Propagation Delay Time Pn to Q	t_{PLH}, t_{PHL} (Figures 4, 7)	5.0 10 15	— — —	260 120 100	520 240 200	ns
Propagation Delay Time Reset to Q	t_{PHL} (Figure 8)	5.0 10 15	— — —	250 110 80	500 220 160	ns
Propagation Delay Time Preset Enable to "0"	t_{PHL}, t_{PLH} (Figures 4, 9)	5.0 10 15	— — —	220 100 80	440 200 160	ns
Clock or Inhibit Pulse Width	t_w (Figures 5, 6)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Clock Pulse Frequency (with PE = low)	f_{max} (Figures 4, 5, 6)	5.0 10 15	— — —	2.0 5.0 6.6	1.5 3.0 4.0	MHz
Clock or Inhibit Rise and Fall Time	t_r, t_f (Figures 5, 6)	5.0 10 15	— — —	— — —	15 5 4	µs
Setup Time Pn to Preset Enable	t_{su} (Figure 10)	5.0 10 15	90 50 40	40 15 10	— — —	ns
Hold Time Preset Enable to Pn	t_h (Figure 10)	5.0 10 15	30 30 30	− 15 − 5 0	— — —	ns
Preset Enable Pulse Width	t_w (Figure 10)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Reset Pulse Width	t_w (Figure 8)	5.0 10 15	350 250 200	175 125 100	— — —	ns
Reset Removal Time	t_{rem} (Figure 8)	5.0 10 15	10 20 30	− 110 − 30 − 20	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
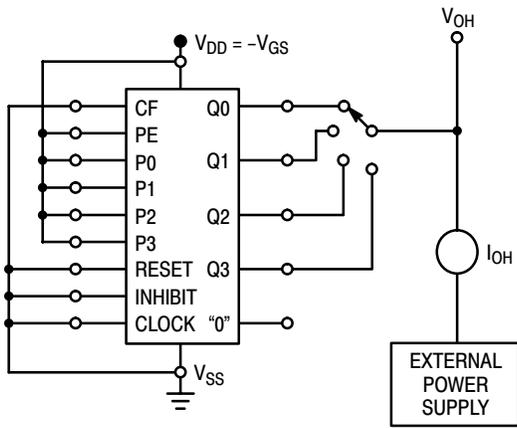
MC14526B

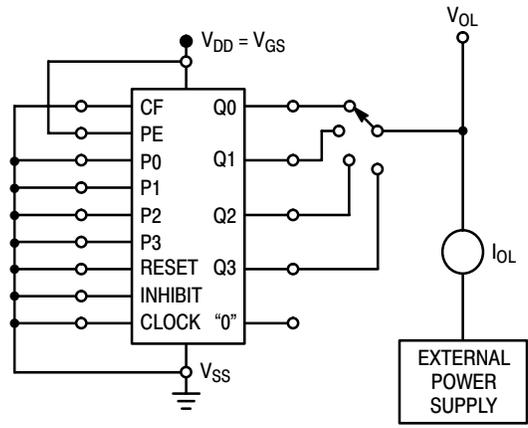**Figure 1. Typical Output Source Characteristics Test Circuit**

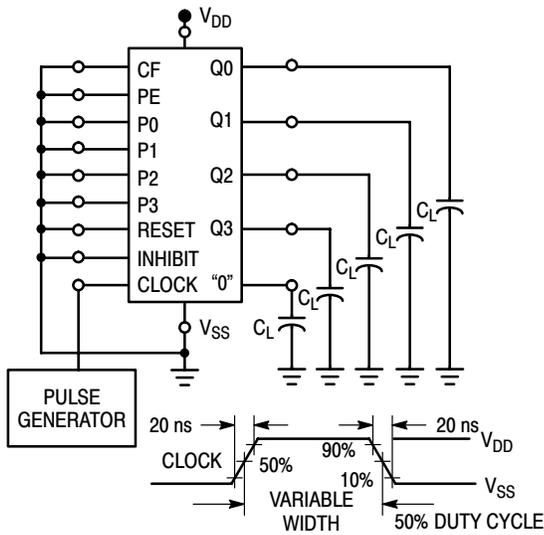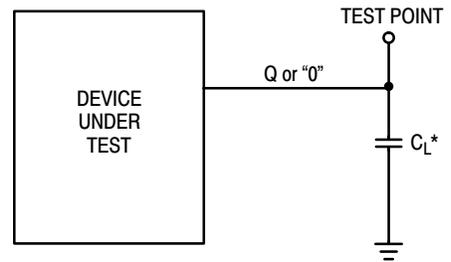**Figure 2. Typical Output Sink Characteristics Test Circuit**

Figure 3. Power Dissipation

* Includes all probe and jig capacitance.
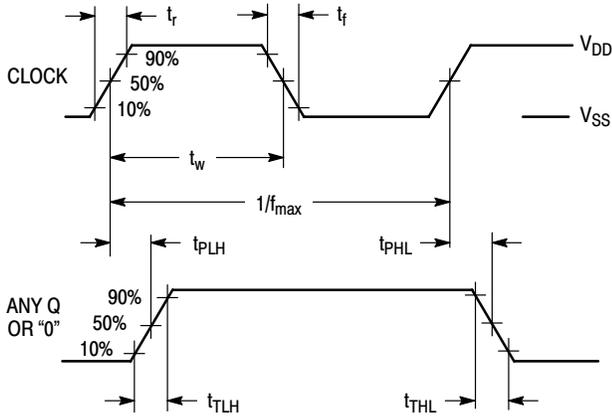
Figure 4. Test Circuit

SWITCHING WAVEFORMS

Figure 5.

Figure 6.
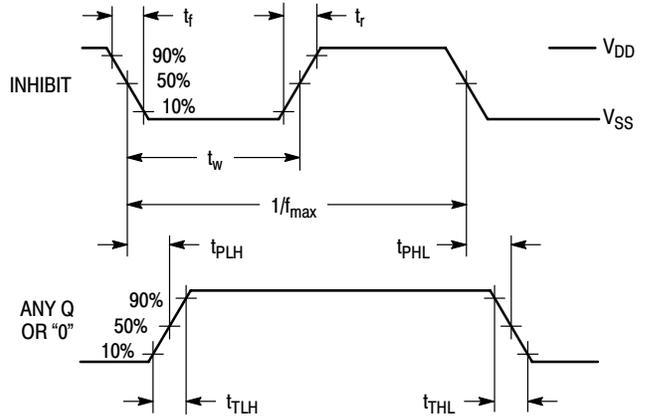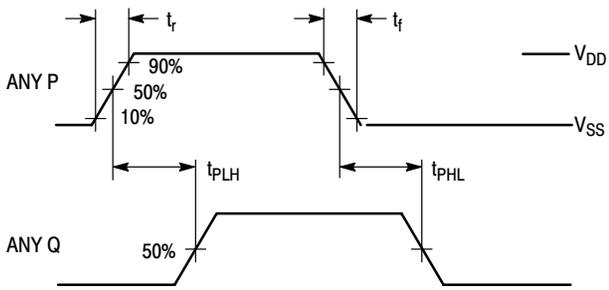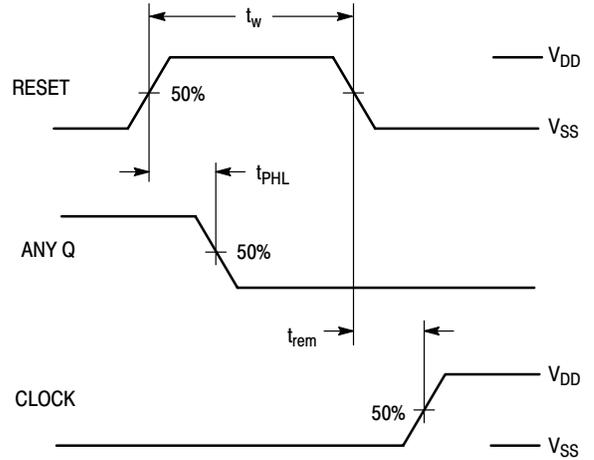
Figure 7.

Figure 8.
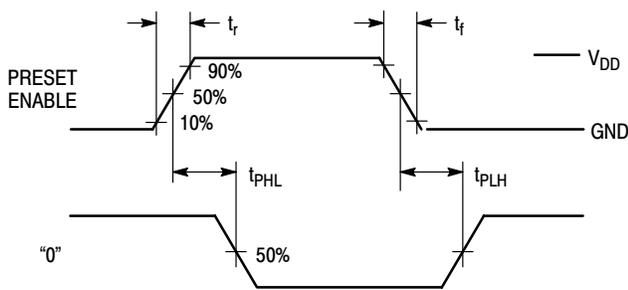
Figure 9.
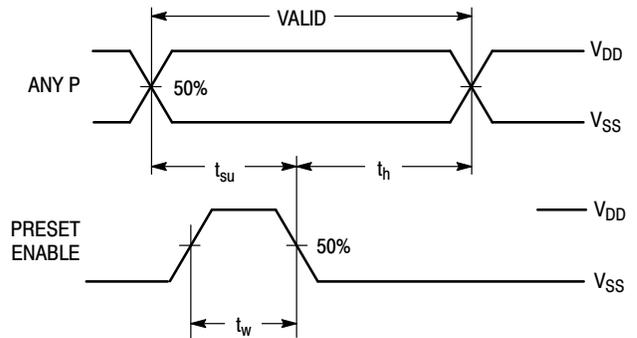
Figure 10.

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PIN DESCRIPTIONS

Preset Enable (Pin 3) — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

Inhibit (Pin 4) — A high level on the Inhibit input pre–vents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

Clock (Pin 6) — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

Reset (Pin 10) — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the "0" output to go high.

"0" (Pin 12) — The "0" (Zero) output issues a pulse one clock period wide when the counter reaches terminal count (Q0 = Q1 = Q2 = Q3 = low) if Cascade Feedback is high and Preset Enable is low. When presetting the counter to a value other than all zeroes, the "0" output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

Cascade Feedback (Pin 13) — If the Cascade Feedback input is high, a high level is generated at the "0" output when the count is all zeroes. If Cascade Feedback is low, the "0" output depends on the Preset Enable input level. See the Function Table.

P0, P1, P2, P3 (Pins 5, 11, 14, 2) — These are the preset data inputs. P0 is the LSB.

Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1) — These are the synchronous counter outputs. Q0 is the LSB.

V_{SS} (Pin 8) — The most negative power supply potential. This pin is usually ground.

V_{DD} (Pin 16) — The most positive power supply potential. V_{DD} may range from 3 to 18 V with respect to V_{SS}.

STATE DIAGRAM

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MC14526B LOGIC DIAGRAM (Binary Down Counter)
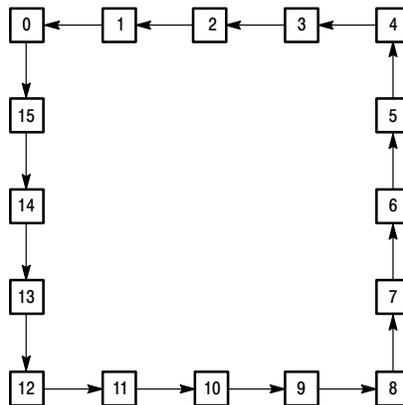
APPLICATIONS INFORMATION

Divide–By–N, Single Stage

Figure 11 shows a single stage divide–by–N application.

To initialize counting a number, N is set on the parallel inputs (P0, P1, P2, and P3) and reset is taken high asynchronously. A zero is forced into the master and slave of each bit and, at the same time, the "0" output goes high. Because Preset Enable is tied to the "0" output, preset is enabled. Reset must be released while the Clock is high so the slaves of each bit may receive N before the Clock goes low. When the Clock goes low and Reset is low, the "0" output goes low (if P0 through P3 are unequal to zero).

The counter downcounts with each rising edge of the Clock. When the counter reaches the zero state, an output pulse occurs on "0" which presets N. The propagation delays from the Clock's rising and falling edges to the "0" output's rising and falling edges are about equal, making the "0" output pulse approximately equal to that of the Clock pulse.

The Inhibit pin may be used to stop pulse counting. When this pin is taken high, decrementing is inhibited.

Cascaded, Presettable Divide–By–N

Figure 12 shows a three stage cascade application. Taking Reset high loads N. Only the first stage's Reset pin (least significant counter) must be taken high to cause the preset for all stages, but all pins could be tied together, as shown.

When the first stage's Reset pin goes high, the "0" output is latched in a high state. Reset must be released while Clock is high and time allowed for Preset Enable to load N into all stages before Clock goes low.

When Preset Enable is high and Clock is low, time must be allowed for the zero digits to propagate a Cascade Feedback to the first non–zero stage. Worst case is from the most significant bit (M.S.B.) to the L.S.B., when the L.S.B. is equal to one (i.e. N = 1).

After N is loaded, each stage counts down to zero with each rising edge of Clock. When any stage reaches zero and the leading stages (more significant bits) are zero, the "0" output goes high and feeds back to the preceding stage. When all stages are zero, the Preset Enable automatically loads N while the Clock is high and the cycle is renewed.
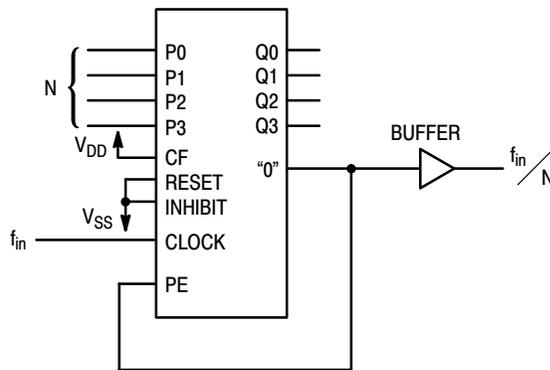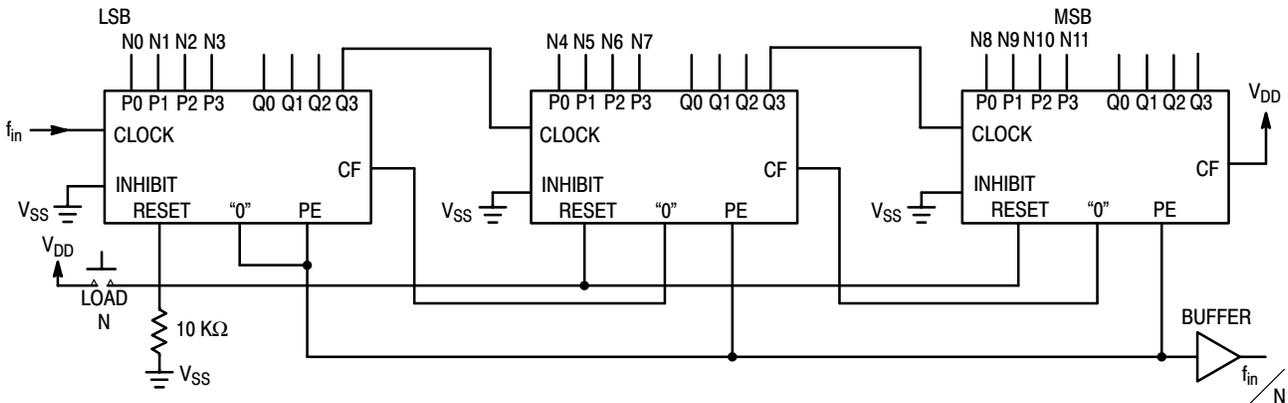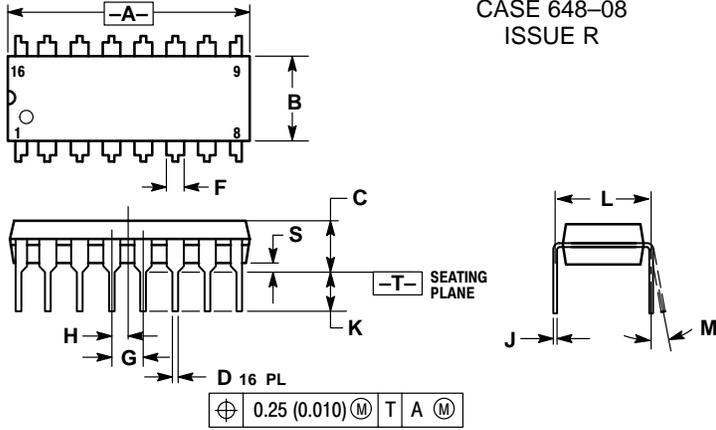

Figure 11. ÷ N Counter

Figure 12. 3 Stages Cascaded

MC14526B

PACKAGE DIMENSIONS

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC–16
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–03
ISSUE B
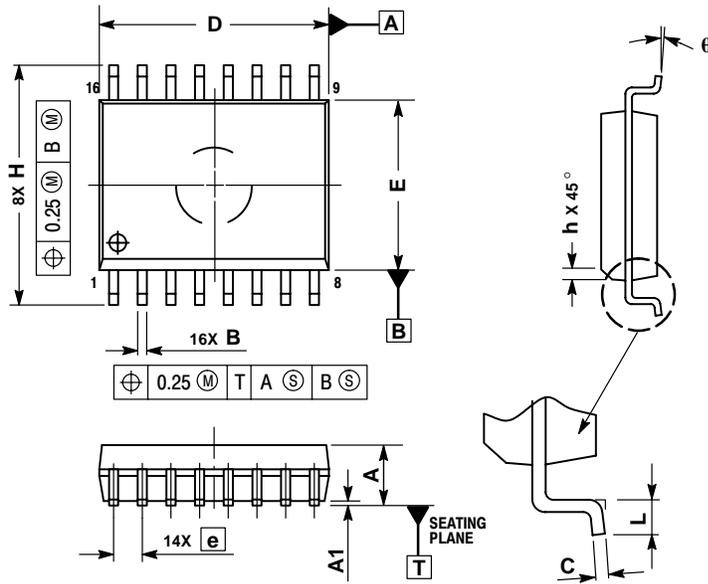
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

MC14526B

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966–01
ISSUE O

DETAIL P

VIEW P
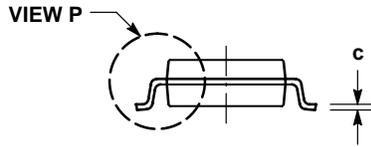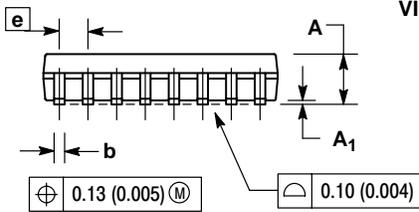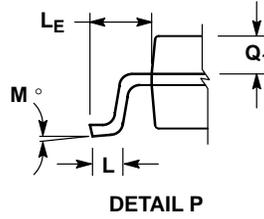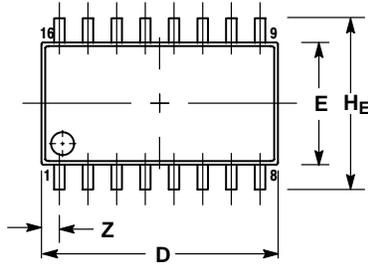
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

⊕ 0.13 (0.005) Ⓜ

△ 0.10 (0.004)

PUBLICATION ORDERING INFORMATION