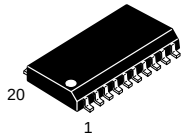
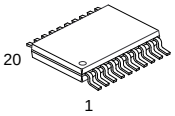
MC145220

Dual 1.1 GHz PLL Frequency Synthesizer

BiCMOS



F SUFFIX
SOG PACKAGE
CASE 803C

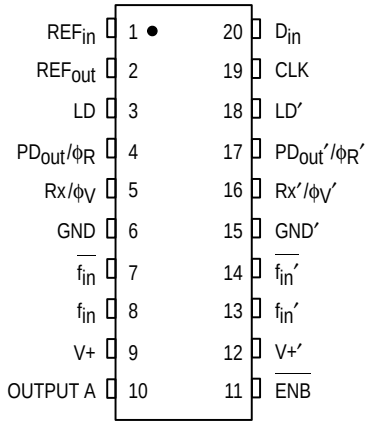


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145220F	SOG Package
MC145220DT	TSSOP

PIN ASSIGNMENT



The MC145220 is a low–voltage, single–chip frequency synthesizer with serial interface capable of direct usage up to 1.1 GHz. The device simultaneously supports two loops. The two on–chip dual–modulus prescalers may be independently programmed to divide by either 32/33 or 64/65.

The device consists of two dual–modulus prescalers, two 6–stage A counters, two 12–stage N counters, two fully programmable 13–stage R (reference) counters, and two lock detectors. Four phase/frequency detectors are included: two with current source/sink outputs and two with double–ended outputs.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte–oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145220 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or multiple address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals. Because this device is a dual synthesizer, a single steering bit is used in the serial data stream to direct the data to either side of the chip.

The phase/frequency detectors have linear transfer functions (no dead zones). The current delivered by the current source/sink outputs is controllable via the serial port.

Also featured are low–power standby for either one or both loops and on–board support of an external crystal. In addition, the part may be configured such that the REF_{in} pin accepts an external reference signal. In this configuration, the REF_{out} pin may be programmed to output the REF_{in} frequency divided by 1, 2, 4, 8, or 16.

- Operating Frequency: 40 to 1100 MHz
- Operating Supply Voltage Range: 2.7 to 5.5 V
- Supply Current: Both PLLs Operating — 12 mA Nominal
  One PLL Operating, One on Standby — 6.5 mA Nominal
  Both PLLs on Standby — 30 μA Maximum
- Phase Detector Output Current: Up to 2 mA @ 5 V
  Up to 1 mA @ 3 V
- Operating Temperature Range: – 40 to 85°C
- Independent R Counters Allow Use of Different Step Sizes for Each Loop
- Double–Buffered R Register — Reference and Loop Divide Ratios Updated Simultaneously
- R Counter Division Range: 1 and 10 to 8,191
- Dual–Modulus Capability Provides Total Division of the VCO Frequency up to 262,143
- Direct Interface to Motorola SPI Data Port
- Evaluation Kit Available (Part Number MC145220EVK)
- See Application Note AN1253/D for Low–Pass Filter Design, and AN1277/D for Offset Reference PLLs for Fine Resolution or Fast Hopping

NOTE: This product has been evaluated for operation over a wider range than 40 MHz to 1.1 GHz. If your design requires a wider frequency range, contact your local Motorola representative for further information.

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REV 4
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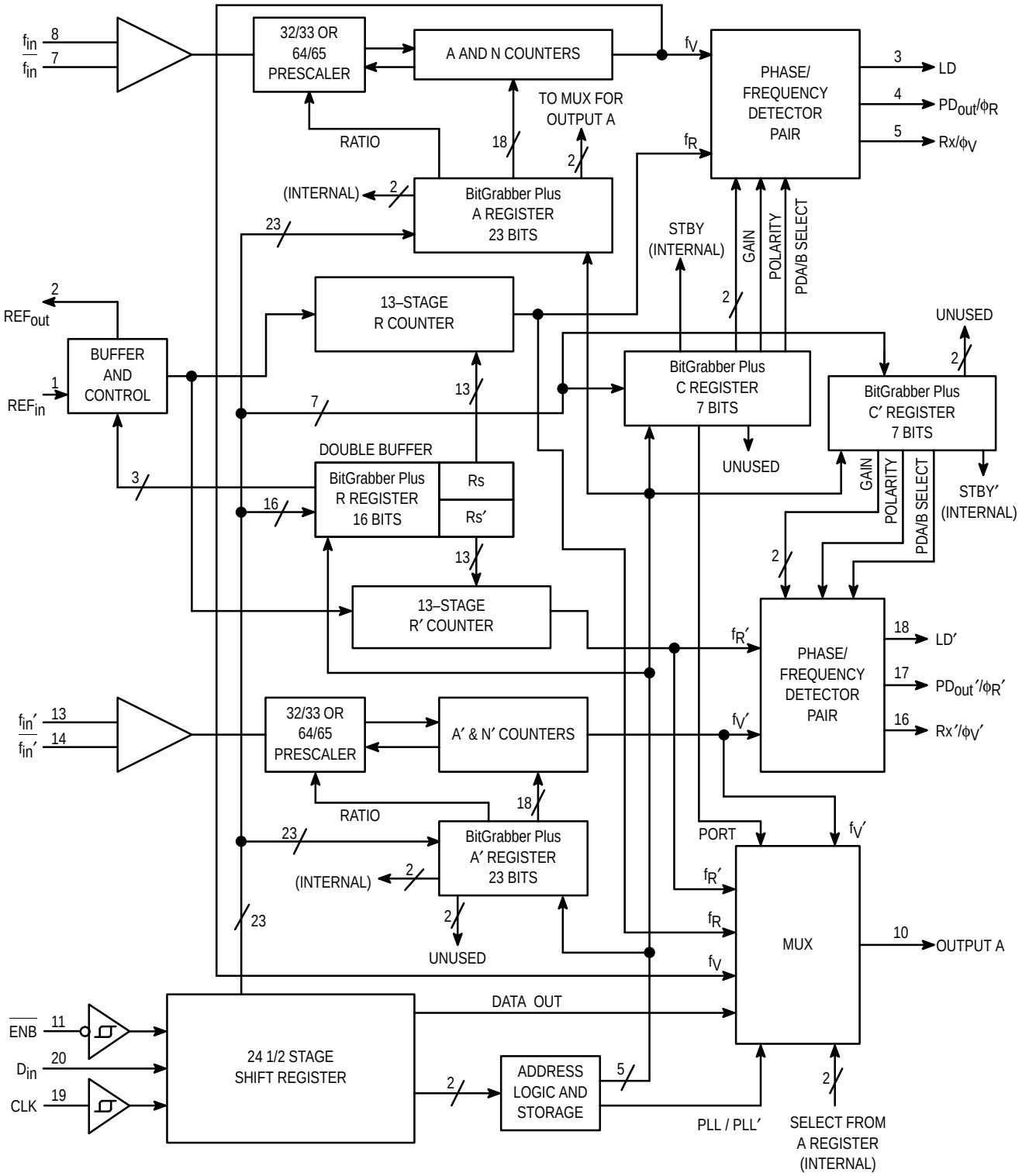
BLOCK DIAGRAM



PIN 9 = V+ (Positive Power to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 6 = GND (Ground to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 12 = V+′ (Positive Power to PLL′ and a portion of the Serial Port)
PIN 15 = GND′ (Ground to PLL′ and a portion of the Serial Port)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V+, V+′	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V+ + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V+ + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I	DC Supply Current, V+, V+′, GND, and GND′ Pins	30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, Voltages Referenced to GND, T_A = – 40 to 85°C, unless otherwise stated)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.3 x V+	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.7 x V+	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, ENB)		100	mV
V_{OL}	Maximum Low–Level Output Voltage (LD, LD′, REF_{out}, Output A)	I_{out} = 20 µA, Device in Reference Mode; Output A Not Selected as Port	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, Output A)	I_{out} = – 20 µA, Device in Reference Mode; Output A Not Selected as Port	V+ – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out})	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx′/ϕ_V')	V_{out} = 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	0.5	mA
I_{OL}	Minimum Low–Level Output Current (Output A)	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (LD, LD′)	V_{out} = 0.3 V	0.5	mA
I_{OH}	Minimum High–Level Output Current (REF_{out})	V_{out} = V+ – 0.3 V	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx′/ϕ_V')	V_{out} = V+ – 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (Output A)	V_{out} = V+ – 0.3 V; Output A Not Selected as Port	– 0.4	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V+ or GND; Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V+ or GND; Device in Reference Mode	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R')	V_{out} = V+ or GND; Phase/Frequency Detectors Configured with PD_{out} Output, Output in High–Impedance State	± 150	nA
I_{OZ}	Maximum Output Leakage Current (Output A, LD, LD′)	V_{out} = V+ or GND; Output A Selected as Port; Output in High–Impedance State	± 5	µA
I_{STBY}	Maximum Standby Supply Current	V_{in} = V+ or GND; Outputs Open; Both PLLs in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode	30	µA
I_T	Total Operating Supply Current	f_{in} = f_{in}' = 1.1 GHz; both loops active; REF_{in} = 13 MHz @ 1 V p–p; Output A = Inactive; All Outputs = No Connect; D_{in}, ENB, CLK = V+ or GND; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	*	mA

* The nominal value is 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUTS — PD_{out}/ϕ_R AND PD_{out}'/ϕ_R'

(Phase/Frequency Detectors Configured with PD_{out} Outputs, $I_{out} \leq 2$ mA @V+ = V+′ = 4.5 to 5.5 V, $I_{out} \leq 1$ mA @V+ = V+′ = 2.7 to 4.4 V, GND = GND′, Voltages Referenced to GND)

Parameter	Test Condition	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part (Notes 3 and 4)	V_{out} = 0.5 x V+	± 20	%
Maximum Sink–versus–Source Mismatch (Note 3)	V_{out} = 0.5 x V+	12	%
Output Voltage Range (Note 3)	I_{out} variation ≤ 20%	0.5 to V+ – 0.5 V	V

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40 to 85°C and given supply voltage within 2.7 to 5.5 V.
4. Applicable for the Rx/ϕ_V or Rx'/ϕ_V' reference pin tied to the GND or GND′ pin through a resistor. See Pin Descriptions for suggested resistor values.

AC INTERFACE CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, C_L = 25 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Serial Data CLK Frequency (Figure 1) NOTE: Refer to Clock t_w below	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to Output A (Selected as Data Out) (Figures 1 and 5)	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, ENB to Output A (Selected as Port) (Figures 2 and 6)	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Output A; t_{THL} only, on Output A when Selected as Port (Figures 1, 5, and 6)	200	ns
C_{in}	Maximum Input Capacitance — D_{in}, CLK, ENB	10	pF

TIMING REQUIREMENTS (V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} versus CLK (Figure 3)	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, ENB versus CLK (Figure 4)	100	ns
t_w	Minimum Pulse Width, ENB (Figure 4)	*	cycles
t_w	Minimum Pulse Width, CLK (Figure 1)	250	ns
t_r, t_f	Maximum Input Rise and Fall Times — CLK (Figure 1)	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} or f_{in}' cycles with selection of a 64/65 prescale ratio or 99 f_{in} or f_{in}' cycles with selection of a 32/33 prescale ratio, whichever is greater.

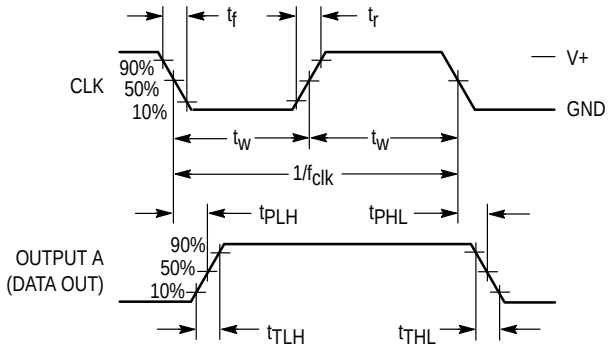


Figure 1.

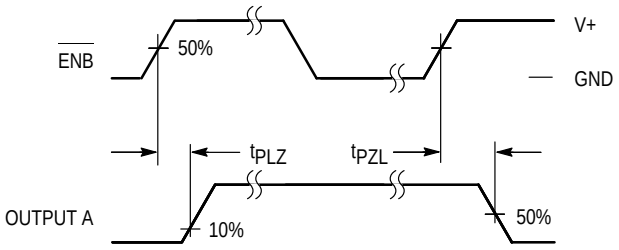


Figure 2.

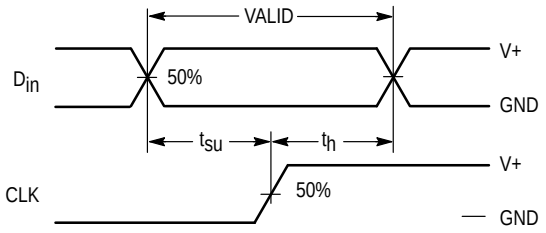


Figure 3.

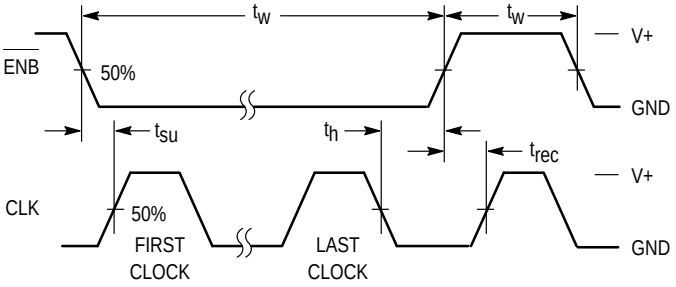
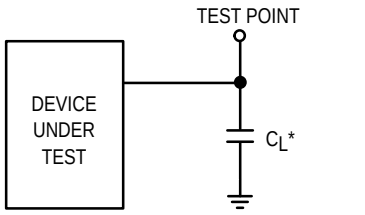
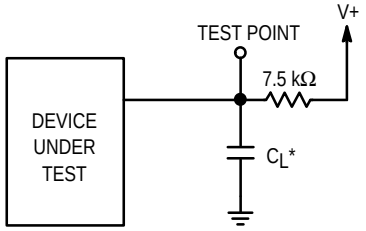


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5.



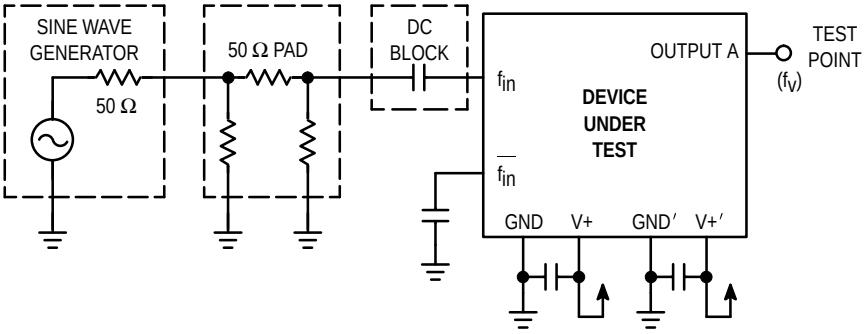
* Includes all probe and fixture capacitance.

Figure 6.

LOOP SPECIFICATIONS (V+ = V+′ = 2.7 to 5.5 V unless otherwise indicated, GND = GND′, T_A = – 40 to 85°C)

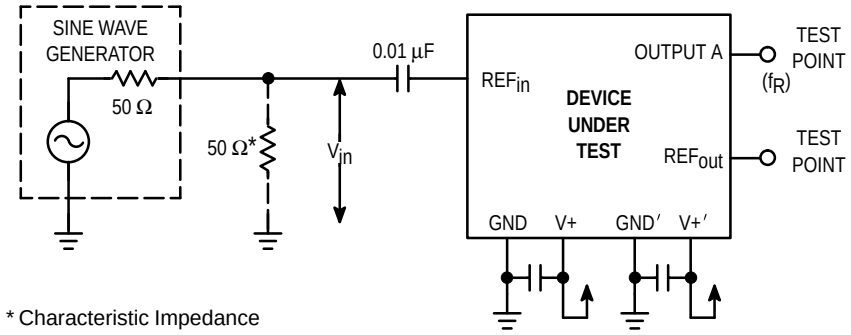
Symbol	Parameter	Test Condition	Guaranteed Operating Range		Unit
			Min	Max	
P_{in}	Input Sensitivity Range, f_{in} or f_{in}' (Figure 7)	40 MHz ≤ frequency < 300 MHz 300 MHz ≤ frequency < 700 MHz 700 MHz ≤ frequency < 1100 MHz	– 2 – 5 – 16	8 6 4	dBm*
ΔP_{in}	Difference Allowed Between f_{in} and f_{in}'			10	dB
—	Isolation Between f_{in} and f_{in}'		15		dB
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode (Figure 8)	V_{in} ≥ 400 mV p–p, R Counter set to divide ratio such that f_R ≤ 1 MHz, REF Counter set to divide ratio such that REF_{out} ≤ 5 MHz	4	27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance; R Counter and REF Counter same as above V+ = 2.7 V V+ = 3.5 V V+ = 4.5 V V+ = 5.5 V	 2 2 2 2	 10 13 15 15	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 25 pF	dc	5	MHz
f	Operating Frequency of the Phase Detectors		dc	1	MHz
t_w	Output Pulse Width, ϕR, ϕV, $\phi R'$, $\phi V'$ (Figures 11 and 12)	f_R in Phase with f_V, C_L = 25 pF	16	125	ns
C_{in}	Input Capacitance, REF_{in}		—	5	pF

* Power level at the input to the dc block.



NOTE: Alternately, the 50 Ω pad may be a T network.

Figure 7. Test Circuit



* Characteristic Impedance

Figure 8. Test Circuit — Reference Mode

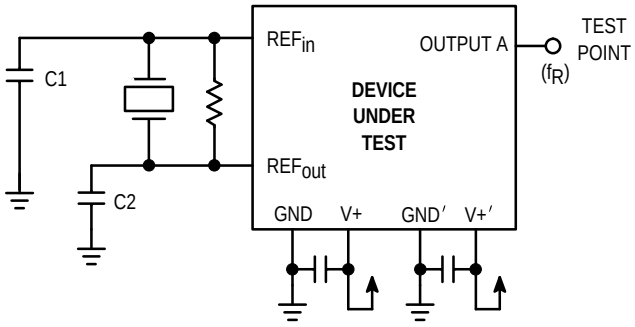


Figure 9. Test Circuit — Crystal Mode

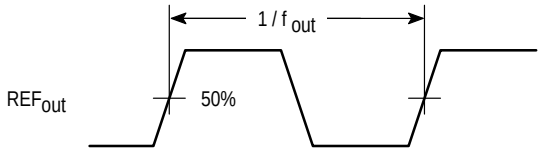


Figure 10. Switching Waveform

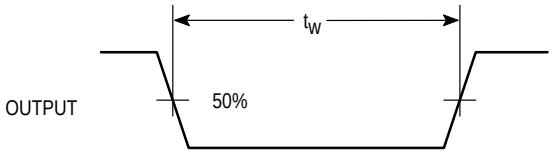
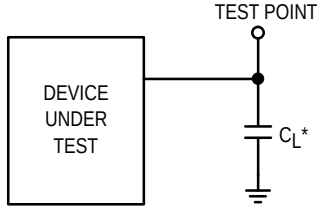
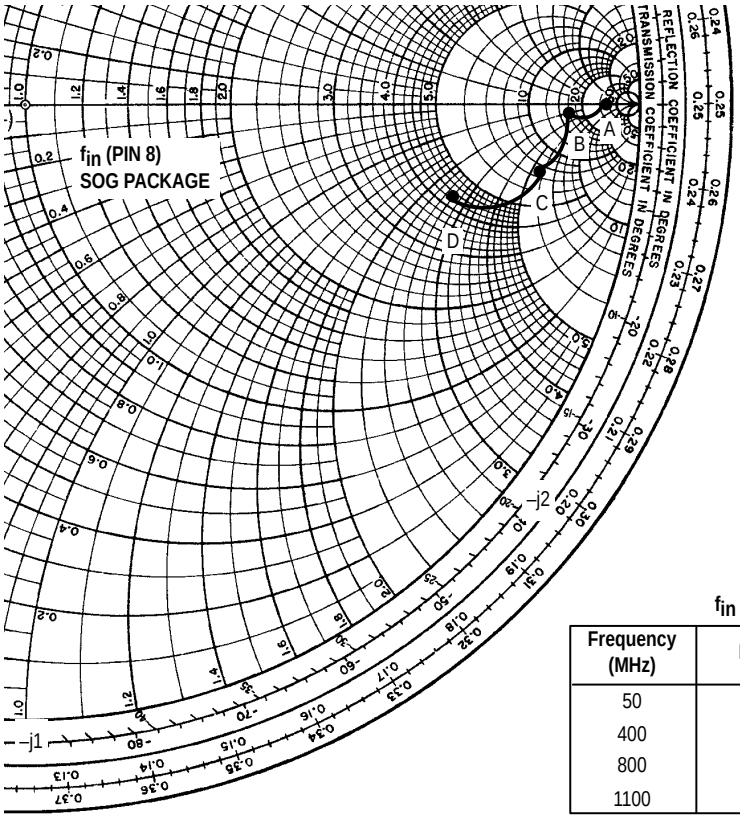


Figure 11. Switching Waveform



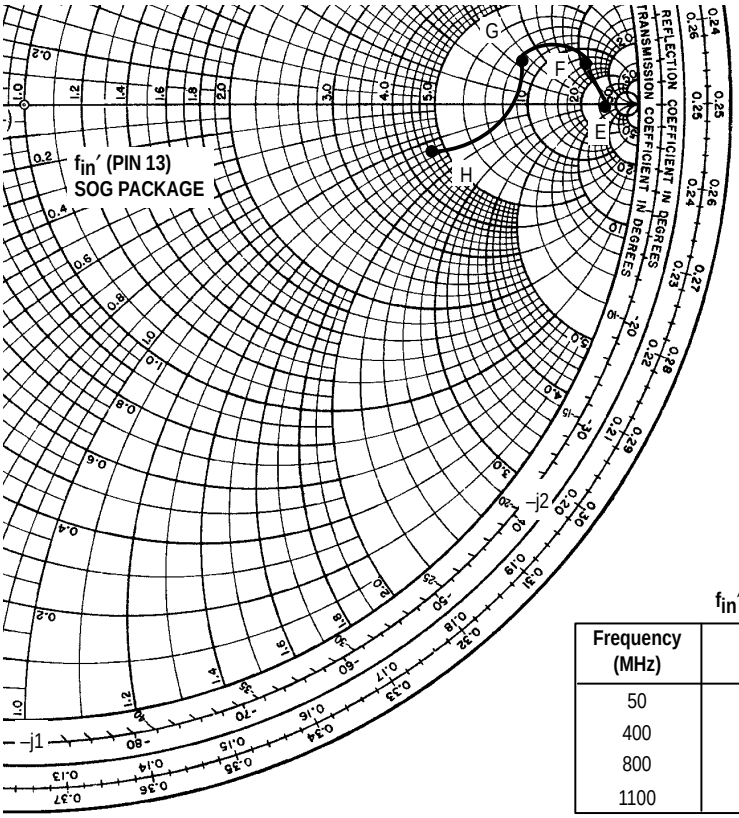
* Includes all probe and fixture capacitance.

Figure 12. Test Circuit



f_{in} (PIN 8) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	A	1900 – j 157	1970 – j 102
400	B	1440 – j 228	1510 + j 19
800	C	552 – j 380	671 – j 334
1100	D	196 – j 141	223 – j 147



f_{in}' (PIN 13) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	E	1900 + j 149	1930 + j 214
400	F	878 + j 703	746 + j 741
800	G	705 + j 208	626 + j 327
1100	H	215 – j 69.3	243 – j 61.3

Figure 13. Nominal Input Impedance of f_{in} and f_{in}' — Series Format (R + jX) (50 – 1100 MHz)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 20)

The bit stream begins with the MSB and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration registers, 2 bytes (16 bits) to access the first buffer of the R registers, or 3 bytes (24 bits) to access the A registers (see Table 1). The values in the registers do not change during shifting because the transfer of data to the registers is controlled by ENB.

NOTE

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 LSBs of the R registers are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The two second buffers of the R register contain the two 13–bit divide ratios for the R counters. These second buffers are loaded with the contents of the first buffer as follows. Whenever the A register is loaded, the Rs (second) buffer is loaded from the R (first) buffer. Similarly, whenever the A′ register is loaded, the Rs′ (second) buffer is updated from the R (first) buffer. This allows presenting new values to the R, A, and N counters simultaneously. Note that two different R counter divide ratios may be established: one for the main PLL and another for PLL′.

The bit stream does not need address bits due to the innovative BitGrabber Plus registers. A steering bit is used to direct data to either the main PLL or PLL′ section of the chip. Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 14, 15, and 16.

D_{in} typically switches near 50% of V+ to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Registers	C7, C6, C5, . . ., C0
16	R Register, First Buffer	R15, R14, R13, . . ., R0
24	A Registers	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 24 to 27	

CLK
Serial Data Clock Input (Pin 19)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from Output A (when configured as Data Out, see Pin 10). The 24–1/2 stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C registers. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A registers. See Table 1 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 25 through 27.

CLK typically switches near 50% of V+ and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with ENB being a don't care) or ENB must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. Floating, toggling, or having these pins in the wrong state during power–up does not harm the chip, but causes two potentially undesirable effects. First, the outputs of the device power up in an unknown state. Second, if two devices are cascaded, the A Registers must be written twice after power up. After these two accesses, the two cascaded chips perform normally.

$\overline{ENB}$
Active–Low Enable Input (Pin 11)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When ENB is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, ENB (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and ENB is taken back high. The low–to–high transition on ENB transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever ENB is high and CLK is low.

This input is Schmitt–triggered and switches near 50% of V+, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 10)

Output A is selectable as f_R, f_V, f_R', f_V', Data Out, or Port. Bits A21 and A22 and the steering bit (A23) control the selection; see Figure 15. When selected as Port, the pin becomes an open–drain N–channel MOSFET output. As such, a pullup device is needed for pin 10. With all other selections, the pin is a totem–pole (push–pull) output.

If A22 = A21 = high, Output A is configured as f_R when the steering bit is low and f_R' when the bit is high. These signals are the buffered outputs of the 13–stage R counters. The signals appear as normally low and pulse high. The signals can be used to verify the divide ratios of the R counters. These ratios extend from 10 to 8191 and are determined by the binary value loaded into bits R0 – R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of one. See Figure 16. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R and f_R' should not exceed 1 MHz.

If A22 = high and A21 = low, Output A is configured as f_V when the steering bit is low and f_V' when the bit is high. These signals are the buffered outputs of the 12–stage N counters. The signals appear as normally low and pulse high. The signals can be used to verify the operation of the prescalers, A counters, and N counters. The divide ratio between the f_{in} or f_{in}' input and the f_V or f_V' signal is N x P + A. N is the divide ratio of the N counter, P is 32 with a 32/33 prescale ratio or 64 with a 64/65 prescale ratio, and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A registers. See Figure 15. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V and f_V' should not exceed 1 MHz.

If A22 = low and A21 = high, Output A is configured as Data Out. This signal is the serial output of the 24–1/2 stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, Output A is automatically configured as Data Out to facilitate cascading devices.

If A22 = A21 = low, Output A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high impedance when the Port bit is high. See Figure 14.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Oscillator Input and Output (Pins 1 and 2)

Configurable Pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In the crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the crystal are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C or C′ register, the oscillator runs, but the R or R′ counter is stopped, respectively. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode shown in Figure 16, and can be engaged whether in standby or not.

In the reference mode, REF_{in} (pin 1) accepts a signal from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. The ac–coupled signal must be at least 400 mV p–p. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for large output swings (V_{OH} to V_{OL}) and 25 pF loads. Therefore, for REF_{in} frequencies above 5 MHz, the one–to–one ratio may not be used for these large signal swing and large C_L requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in}, $\overline{f_{in}}$ and f_{in}', $\overline{f_{in}}'$
Frequency Inputs (Pins 8, 7 and 13, 14)

These pins feed the onboard RF amplifiers which drive the prescalers. These inputs may be fed differentially. However, they usually are used in single–ended configurations (shown in Figure 7). Note that f_{in} is driven while f_{in} must be tied to ac ground (via capacitor). The signal sources driving these pins originate from external VCOs.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the **Loop Specifications** table.

PD_{out}/ϕ_R, PD_{out}'/ϕ_R'
Single–Ended Phase/Frequency Detector Outputs (Pins 4 and 17)

When the C2 bits in the C or C′ registers are low, these pins are independently configured as single–ended outputs PD_{out} or PD_{out}', respectively. As such, each pin is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

These outputs can be enabled, disabled, and inverted via the C and C′ registers. If desired, these pins can be forced to the floating state by utilization of the standby feature in the C or C′ registers (bit C6). This is a patented feature.

The phase detector gain is controllable by bits C4 and C5: gain (in amps per radian) = PD_{out} current in amps divided by 2π.

PD_{out}/ϕ_R, Rx/ϕ_V and PD_{out}'/ϕ_R', Rx'/ϕ_V'
Double–Ended Phase/Frequency Detector Outputs (Pins 4, 5 and 17, 16)

When the C2 bits in the C or C′ registers are high, these two pairs of pins are independently configured as double–ended outputs ϕ_R, ϕ_V or ϕ_R', ϕ_V', respectively. As such, these outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detectors are described below and are shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, or interchanged via C register bits C6 or C0. This is a patented feature. Note that when disabled in standby, these outputs are forced to their rest condition (high state). See Figure 14.

The ϕ_R and ϕ_V output signals swing from approximately GND to V+.

LD and LD′
Lock Detector Outputs (Pins 3 and 18)

Each output is essentially at a high–impedance state with very narrow low–going pulses of a few nanoseconds when the respective loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V, while LD′ is the logical ANDing of ϕ_R' and ϕ_V'. See Figure 17.

Upon power up, on–chip initialization circuitry forces LD and LD′ to the high–impedance state. These pins are low during standby. If unused, LD should be tied to GND and LD′ should be tied to GND′.

These outputs have open–drain N–channel MOSFET drivers. This facilitates a wired–OR function. See Figure 21.

Rx/ϕ_V and Rx'/ϕ_V'
External Current Setting Resistors (Pins 5 and 16)

When the C2 bits in the C or C′ registers are low, these two pins are independently configured as current setting pins Rx or Rx′, respectively. As such, resistors tied between each of these pins and GND and GND′, in conjunction with bits C4 and C5 in the C and C′ registers, determine the amount of current that the PD_{out} pins sink and source. When bits C4 and C5 are both set high, the maximum current is obtained; see Table 2 for other values of current.

Table 2. PD_{out} or PD_{out}' Current

C5	C4	Current
0	0	5%
0	1	50%
1	0	80%
1	1	100%

The formula for determining the value of Rx or Rx′ is as follows.

$$Rx = \frac{V1 - V2}{I}$$

where Rx is the value of external resistor in ohms, V1 is the supply voltage, V2 is 1.5 V for a reference current through Rx of 100 μA or 1.745 V for a reference current of 200 μA, and I is the reference current flowing through Rx or Rx′.

The reference current flowing through Rx or Rx′ is multiplied by a factor of approximately 10 (in the 100% current mode) and delivered by the PD_{out} or PD_{out}' pin, respectively. To achieve a maximum phase detector output current of 1 mA, the resistor should be about 15 kΩ when a 3 V supply is employed. See Table 3.

Table 3. Rx Values

Supply Voltage	Rx	PD_{out} or PD_{out}' Current in 100% Mode
3 V	15 kΩ	1 mA
5 V	16 kΩ	2 mA

Do not use a decoupling capacitor on the Rx or Rx′ pin. Use of a capacitor causes undesirable current spikes to appear on the phase detector output when invoking the standby mode.

POWER SUPPLY PINS

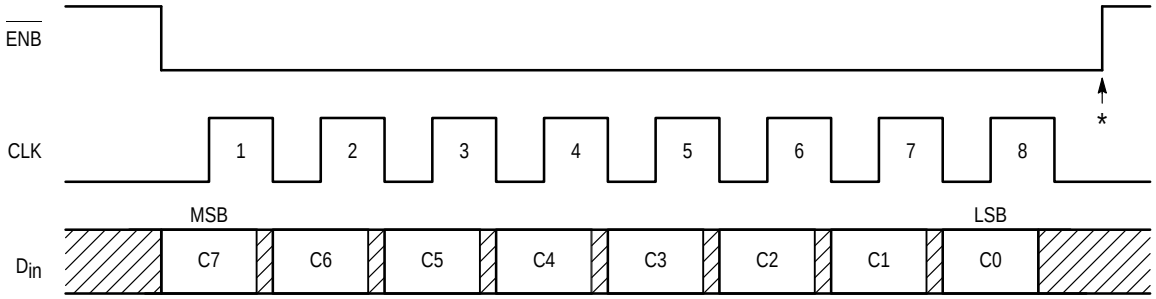
V+ and V+′
Positive Supply Potentials (Pins 9 and 12)

V+ supplies power to the main PLL, reference circuit, and a portion of the serial port. V+′ supplies power to PLL′ and a portion of the serial port. Both V+ and V+′ must be at the same voltage level and may range from 2.7 V to 5.5 V with respect to the GND and GND′ pins.

For optimum performance, V+ should be bypassed to GND and V+′ bypassed to GND′ using separate low–inductance capacitors mounted very close to the MC145220. Lead lengths and printed circuit board traces to the capacitors should be minimized. (The very fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

GND and GND′
Grounds (Pins 6 and 15)

The GND pin is the ground for the main PLL and GND′ is the ground for PLL′.



* At this point, the new byte is transferred to the C or C′ register and stored. No other registers are affected.

C7 – Steer: Used to direct the data to either the C or C′ register. A low level directs data to the C register; a high level is for the C′ register.

C6 – Standby: When set high, places both the main PLL and PLL′ (when C6 is set in the C register) or PLL′ only (when C6 is set in the C′ register) in the standby mode for reduced power consumption. The associated PD_{out} is forced to the floating state, the associated counters (A, N, and R) are inhibited from counting, the associated Rx current is shut off, and the associated prescaler stops counting and is placed in a low current mode. The associated double–ended phase/frequency detector outputs are forced to a high level. In standby, the associated LD output is placed in the low–state, thus indicating "not locked" (open loop). During standby, data is retained in all registers and any register may be accessed.

In standby, the condition of the REF/OSC circuitry is determined by bits R13, R14, and R15 in the R register per Figure 16. However, if REF_{out} = *static low* is selected, the internal feedback resistor is disconnected and the REF_{in} is inhibited when both PLL and PLL′ are placed in standby via the C register. Thus, the REF_{in} only presents a capacitive load. **Note**: PLL/PLL′ standby does not affect the other modes of the REF/OSC circuitry as determined by bits R13, R14, and R15 in the R register. The PLL′ standby mode (controlled from the C′ register) has no effect on the REF/OSC circuit.

When C6 is reset low, the associated PLL (or PLLs) is (are) taken out of standby in two steps. First, the REF_{in} (only in 1 mode, PLL/PLL′ in standby) resistor is reconnected, REF_{in} (only 1 mode) is gated on, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detectors. Second, when the appropriate f_R pulse occurs, the A and N counters are jam loaded, the prescaler is gated on, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C5, C4 – I2, I1: Independently controls the PD_{out} or PD_{out}' source/sink current per Table 2. With both bits high, the maximum current (as set by Rx or Rx′) is available. POR forces C5 and C4 to high levels.

C3 – Spare: Unused

C2 – PDA/B: Independently selects which phase/frequency detector is to be used. When set high, the double–ended detector is selected with outputs ϕ_R and ϕ_V or ϕ_R' and ϕ_V'. When reset low, the current source/sink detector is selected with outputs PD_{out} or PD_{out}'. In the second case, the appropriate Rx or Rx′ pin is tied to an external resistor. POR forces C2 low.

C1 – Port: When the Output A pin is selected as "Port" via bits A22 and A21, C1 of the C register determines the state of Output A. When C1 is set high, Output A is forced to the high–impedance state; C1 low forces Output A low. The Port bit is not affected by the standby mode. **Note**: C1 of the C′ register is not used in any mode.

C0 – POL: Selects the output polarity of the associated phase/frequency detectors. When set high, this bit inverts the associated current source/sink output and interchanges the associated double–ended output relative to the waveforms in Figure 17. Also, see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

Figure 14. C and C′ Register Accesses and Format (8 Clock Cycles are Used)

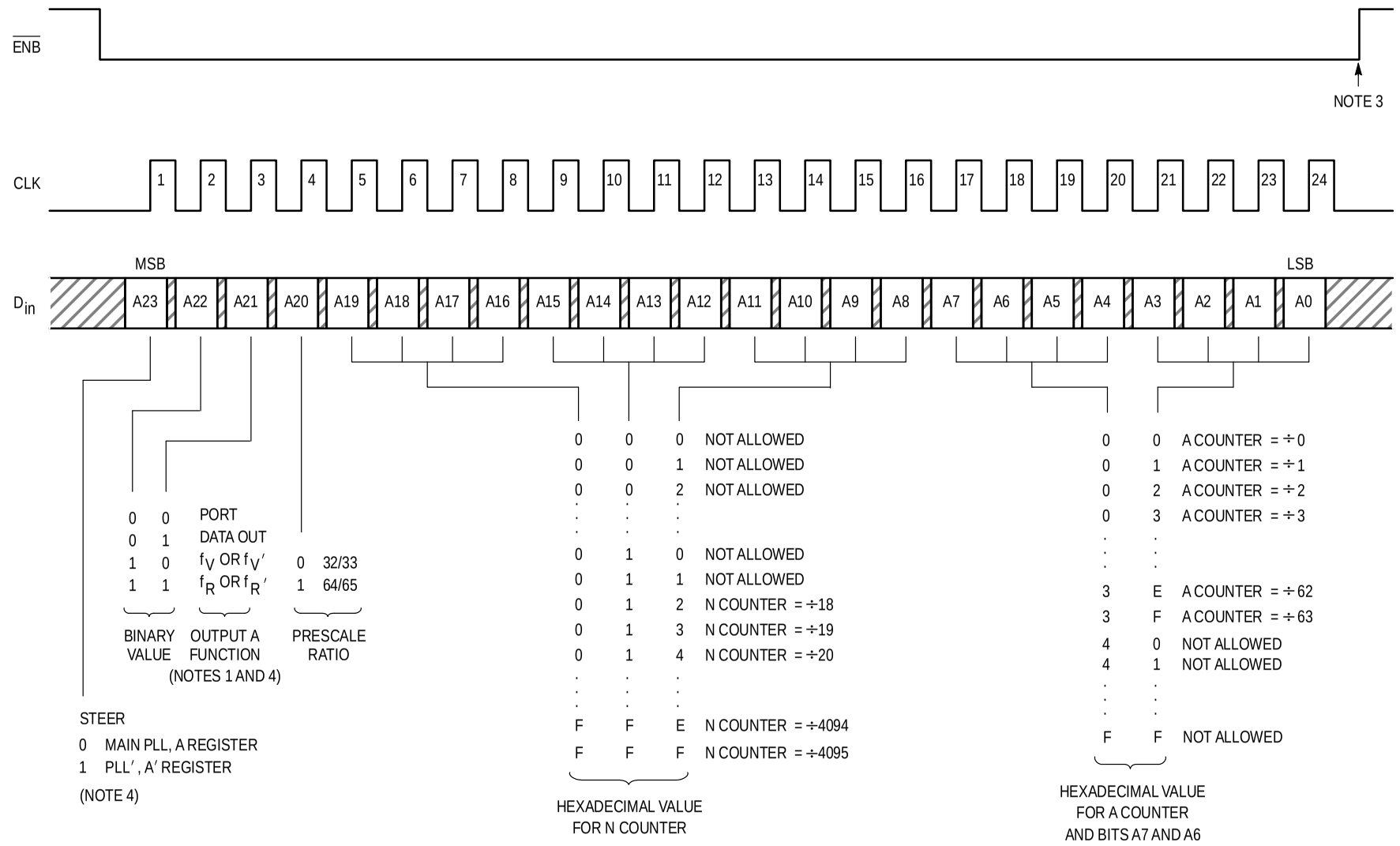
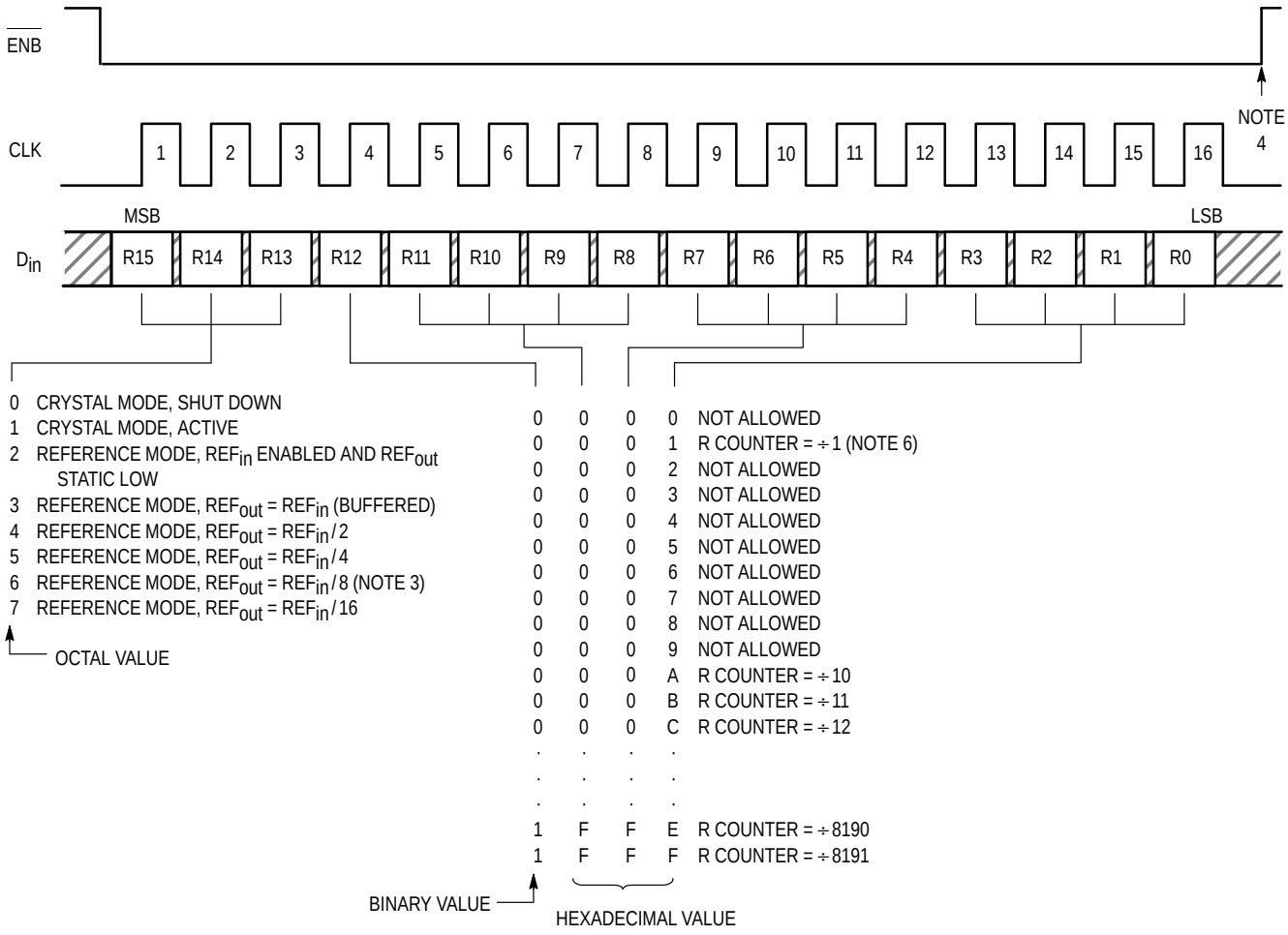


Figure 15. A and A′ Register Accesses and Format (24 Clock Cycles are Used)

NOTES:

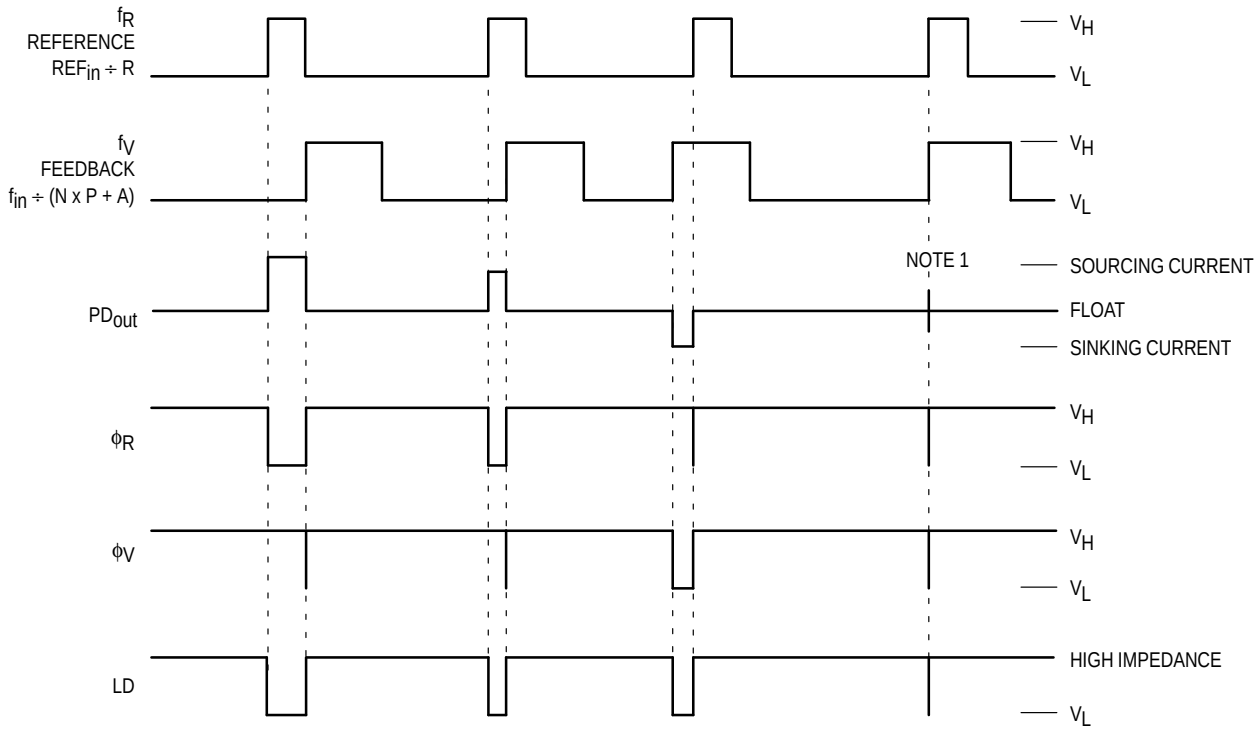
1. A power-on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x P + A where N is the value programmed for the N counter, P is 32 if bit A20 is low or 64 if A20 is high, and A is the value programmed for the A counter.
3. At this point, the three new bytes are transferred to the A register if bit A23 is a "0" or A′ register if A23 is a "1". In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's relative second buffer, Rs or Rs′. Thus, the R, N, and A (or R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C or C′ registers are not affected.
4. A "0" for the Steering bit allows selection of f_R, f_V, Data Out, or Port by bits A21 and A22. A "1" for the Steering bit allows selection of $f_{R'}$, $f_{V'}$, Data Out, or Port.



NOTES:

1. Bits R15 – R13 control the configurable “Buffer and Control” block (see Block Diagram).
2. Bits R12 – R0 control the “13–stage R counter” blocks (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the “Buffer and Control” block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R or R′ counter divide ratio is not altered yet and retains the previous ratio loaded. The C, C′, A, and A′ registers are not affected.
5. Bits R0 – R12 are transferred to the second buffer of the R register (Rs in the Block Diagram) on a subsequent 24–bit write to the A register. The bits are transferred to Rs′ on a subsequent 24–bit write to the A′ register. The respective R counter begins dividing by the new ratio after completing the rest of its present count cycle.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles are Used)



NOTES:

1. At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
2. The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is mostly in a floating condition and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.
3. V_H = High voltage level, V_L = Low voltage level.
4. The waveforms are applicable to both the main PLL and PLL′.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} must be used. See Figure 8.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 20 pF when used near the highest operating frequency of the MC145220. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

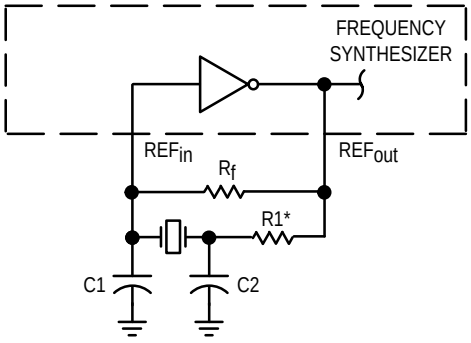
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making either a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at Output A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. Note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 4.



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

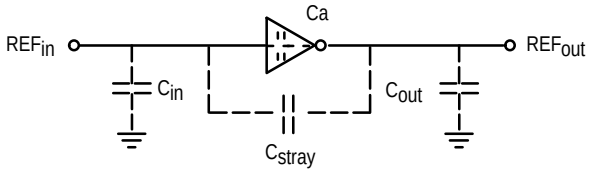
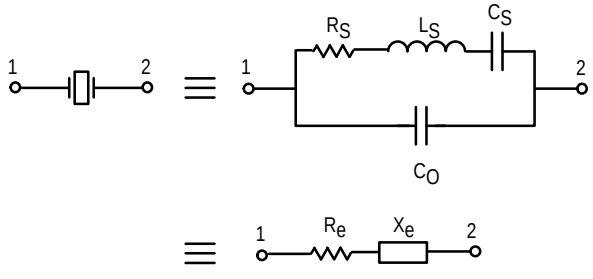


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit – Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

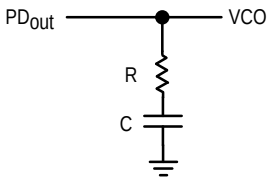
Table 4. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



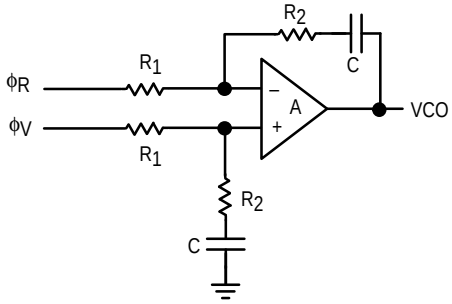
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$Z(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V+/2\pi$ volts per radian for ϕ_V and ϕ_R

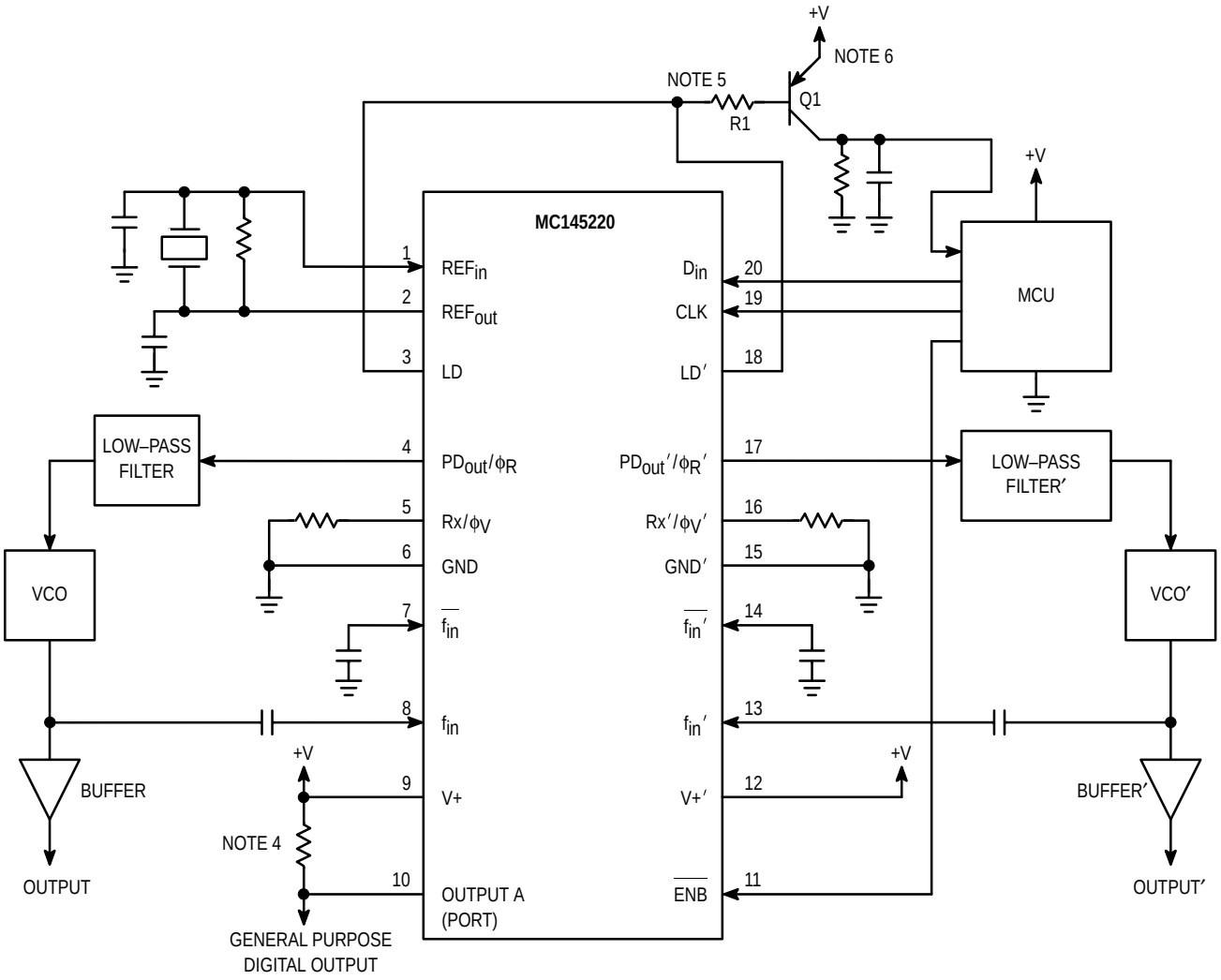
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

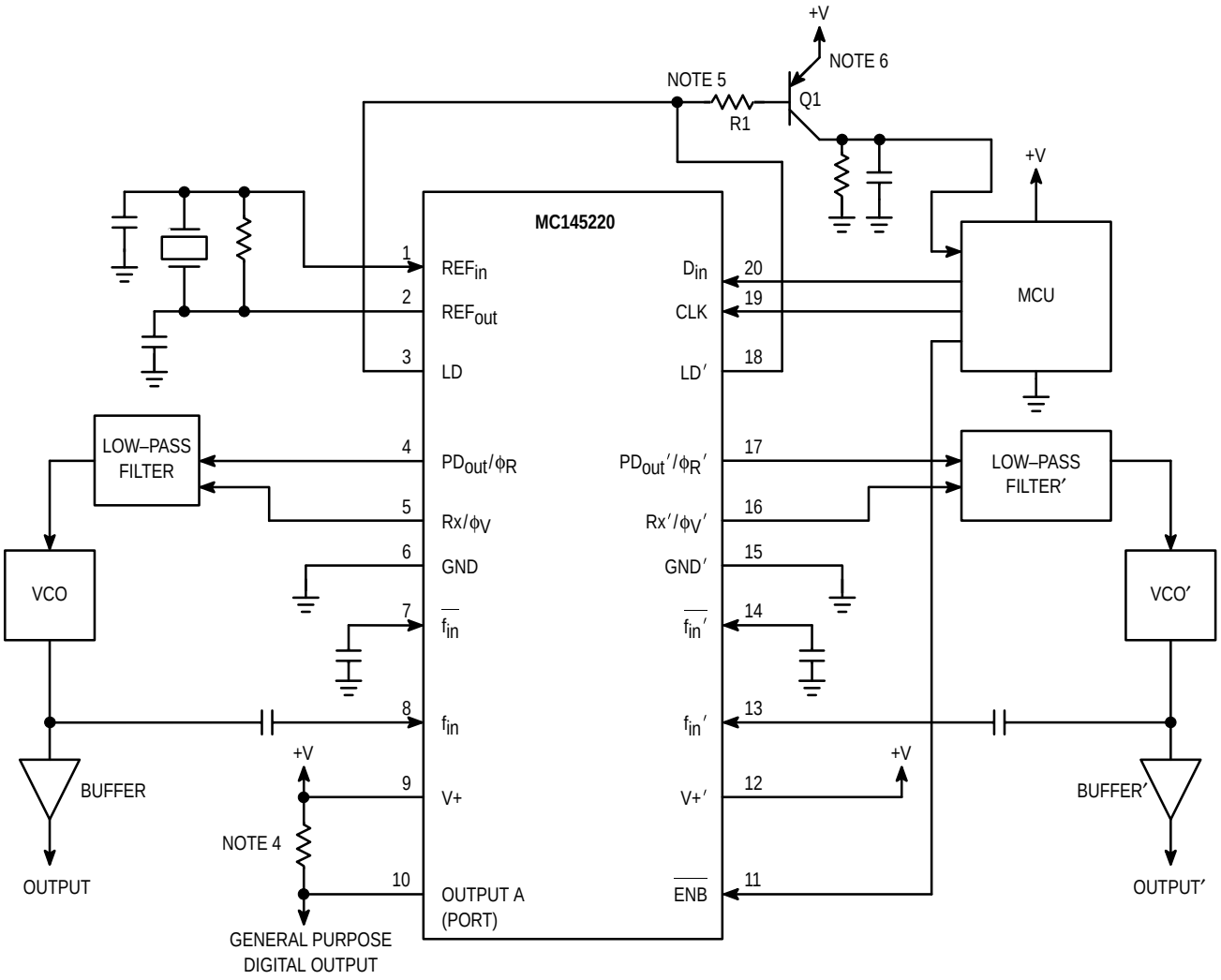
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. The PD_{out} output is fed to an external loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R', f_V, f_V', DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the “pull–up device”.
6. Use of Q1 is optional and depends on loading.

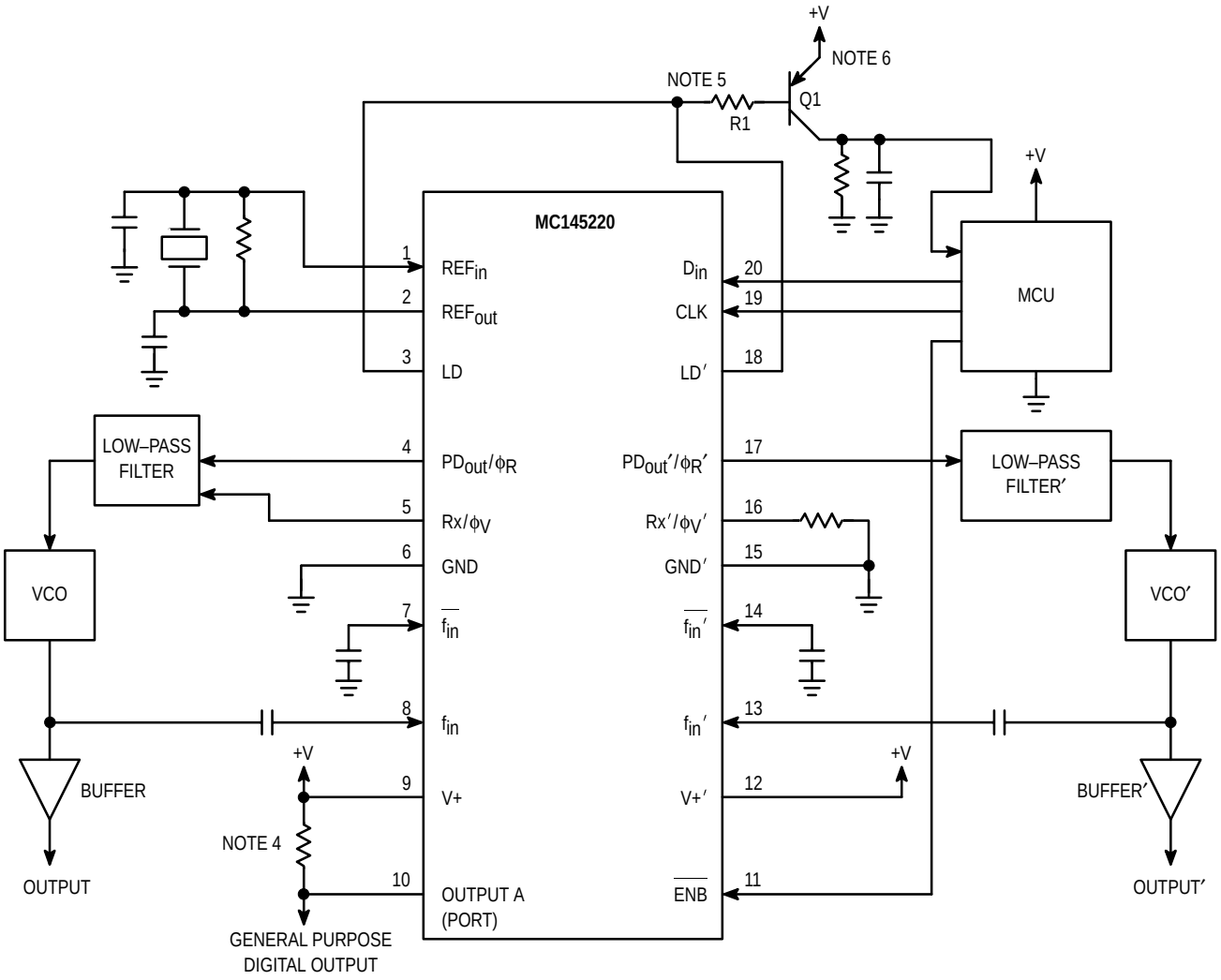
Figure 21. Application Showing Use of the Two Single–Ended Phase/Frequency Detectors



NOTES:

1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R', f_V, f_V', DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the “pull–up device”.
6. Use of Q1 is optional and depends on loading.

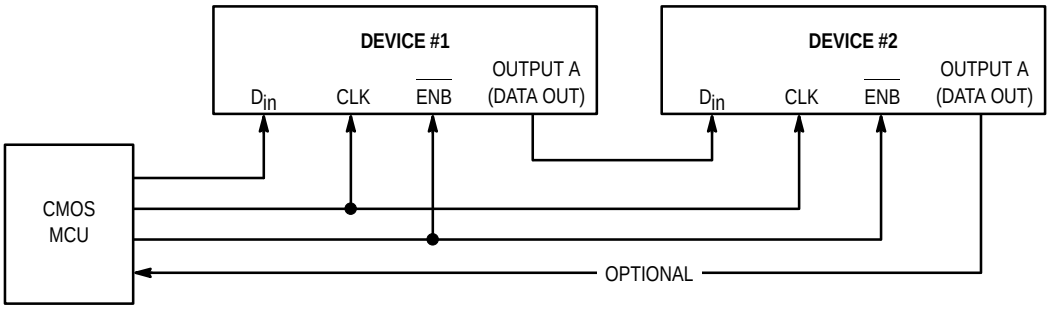
Figure 22. Application Showing Use of the Two Double–Ended Phase/Frequency Detectors



NOTES:

1. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, $f_R′$, f_V, $f_V′$, DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the “pull–up device”.
6. Use of Q1 is optional and depends on loading.

Figure 23. Application Showing Use of Both the Single– and Double–Ended Phase/Frequency Detectors



NOTE: See related Figures 25, 26, and 27.

Figure 24. Cascading Two Devices

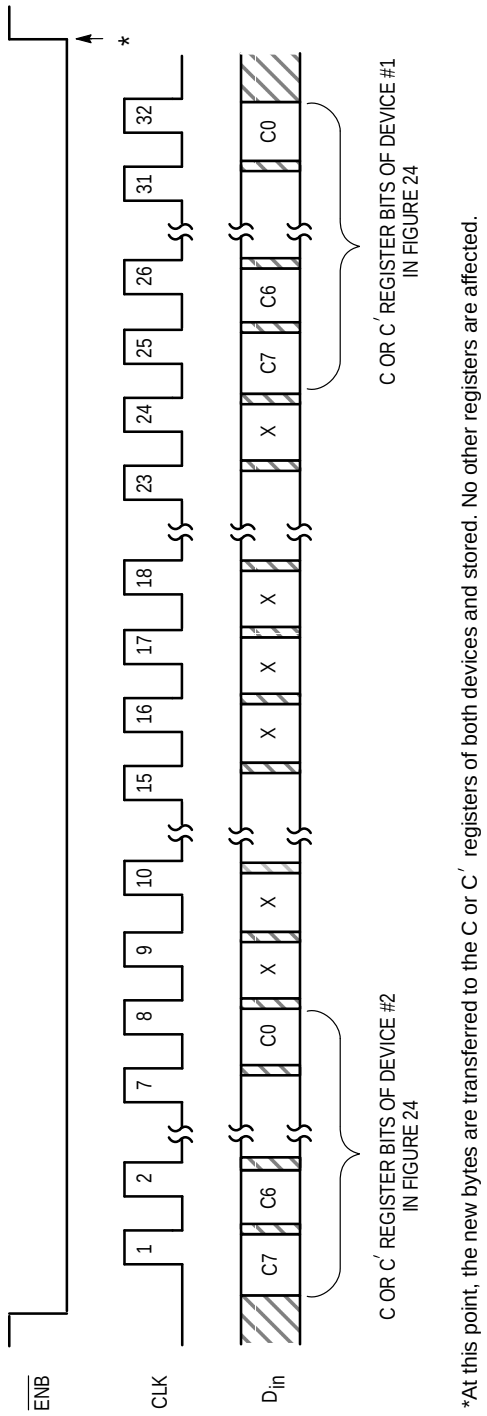
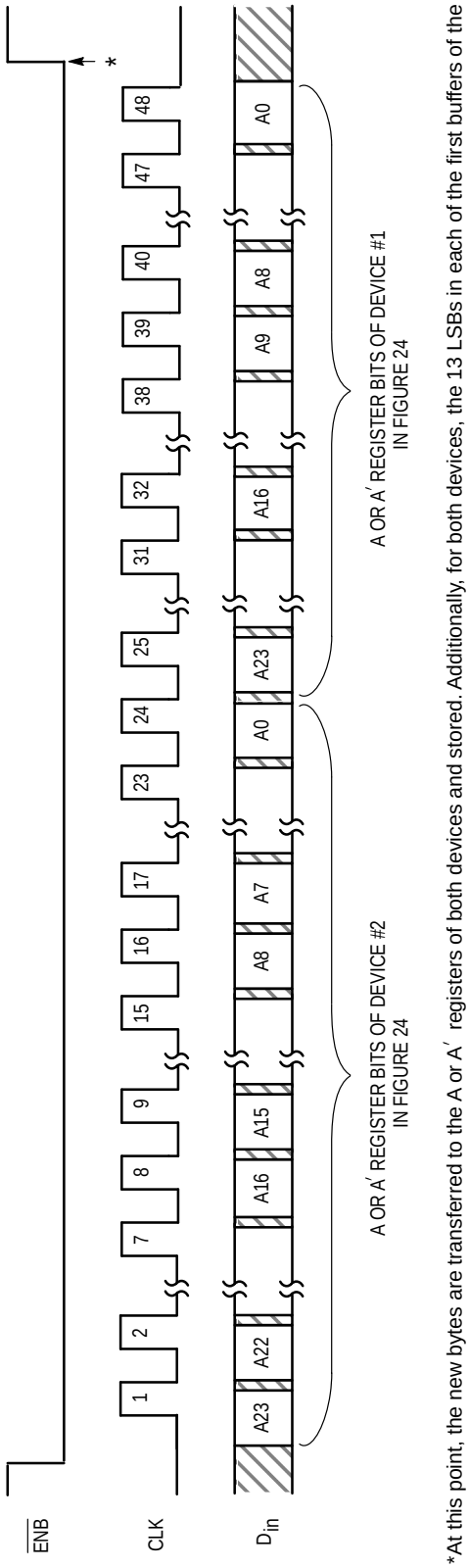
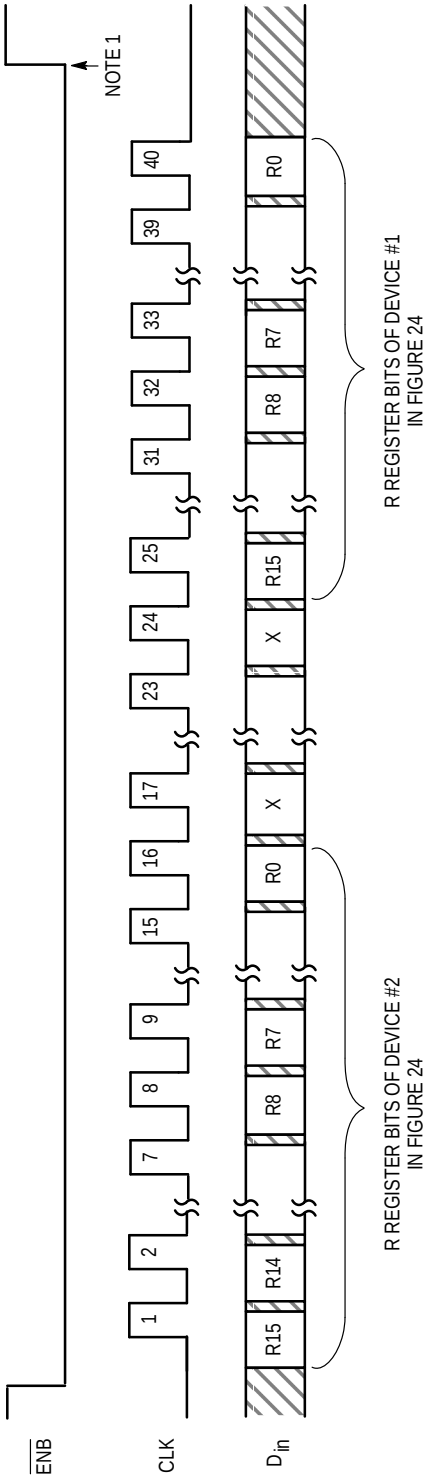


Figure 25. Accessing the C or C′ Registers of Two Cascaded MC145220 Devices (32 Clock Cycles are Used)



*At this point, the new bytes are transferred to the A or A′ registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R Registers are transferred to the respective R register's second buffer. Thus, the R, N, and A (R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. None of the C or C′ registers are affected.

Figure 26. Accessing the A or A′ Registers of Two Cascaded MC145220 Devices (48 Clock Cycles are Used)



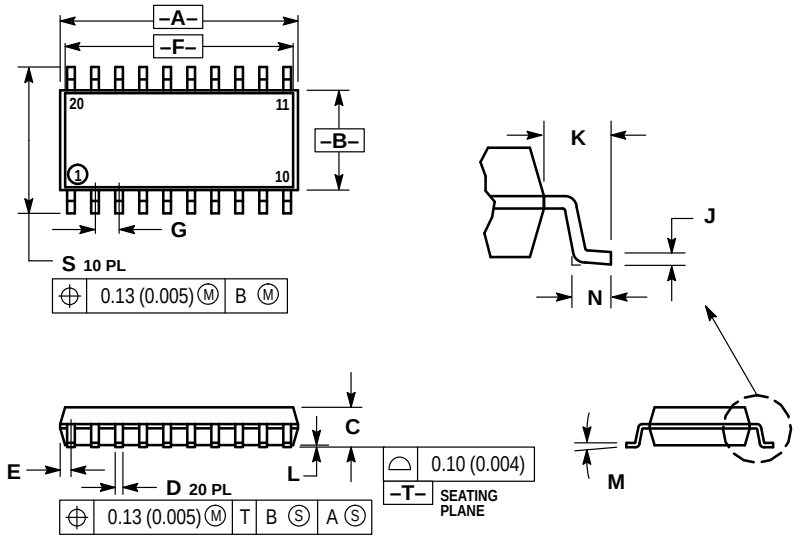
NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the Buffer and Control block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R and R′ counter divide ratios are not altered yet and retain the previous ratios loaded. The other registers are not affected.
2. See note of Figure 26 for the method of loading the second buffers in the R register to achieve new divide ratios.

Figure 27. Accessing the R Registers of Two Cascaded MC145220 Devices (40 Clock Cycles are Used)

PACKAGE DIMENSIONS

F SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 803C–01

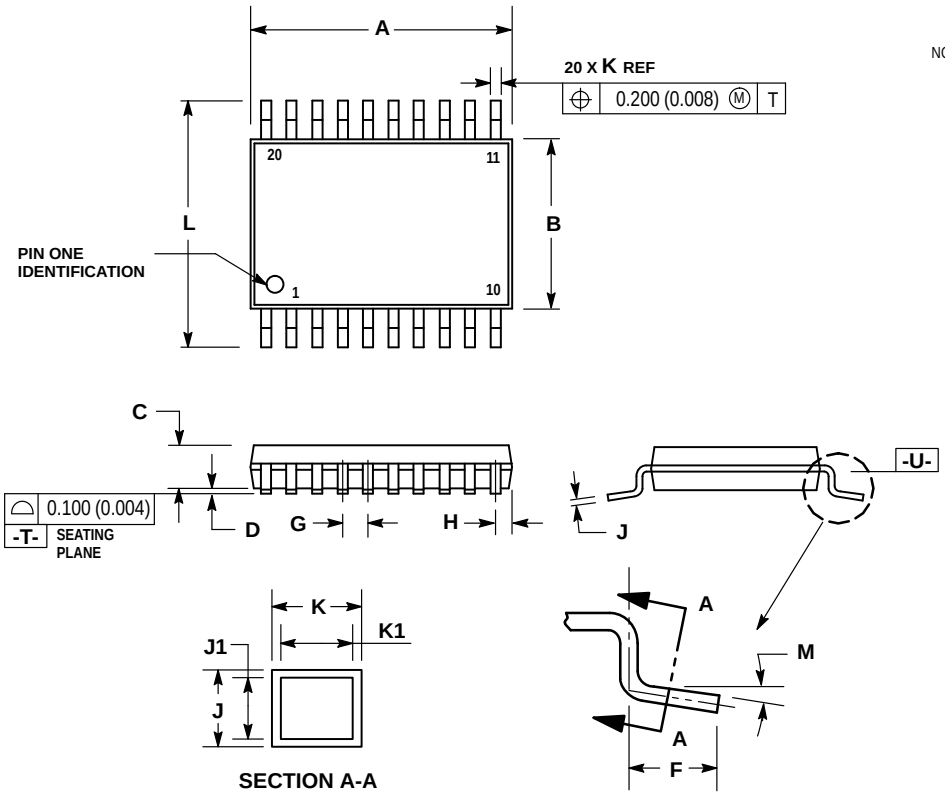


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.008) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.006) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.35	12.80	0.486	0.504
B	5.10	5.45	0.201	0.215
C	1.95	2.05	0.077	0.081
D	0.35	0.50	0.014	0.020
E	—	0.81	—	0.032
F	12.40*		0.488*	
G	1.15	1.39	0.045	0.055
H	0.59	0.81	0.023	0.032
J	0.18	0.27	0.007	0.011
K	1.10	1.50	0.043	0.059
L	0.05	0.20	0.001	0.008
M	0 °	10 °	0 °	10 °
N	0.50	0.85	0.020	0.033
S	7.40	8.20	0.291	0.323

*APPROXIMATE

DT SUFFIX
TSSOP (THIN SHRUNK SMALL OUTLINE PACKAGE)
CASE 948D–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	6.60	—	0.260
B	4.30	4.50	0.169	0.177
C	0.95	1.05	0.037	0.041
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.275	0.375	0.010	0.015
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

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