MC145220EVK

Technical Summary

MC145220 Evaluation Board

INTRODUCTION

The MC145220EVK makes it easy to exercise features of the MC145220 and build PLLs which meet individual performance requirements. The EVK is controlled through menu driven software operating on an IBM PC or compatible. Other Motorola PLL EVKs (MC145190, MC145191, MC145192, MC145200, MC145201, MC145202) in up to three–board cascades can use the same program. Frequency defaults that apply to each are automatically selected. All board functions are controlled through the printer port of an IBM PC. Up to three different EVKs may be controlled at the same time from one printer port. The functional block diagram is given in Figure 1.

This technical summary contains the hardware description for the evaluation board and a summary of the software section. For complete information, consult the manual that is provided in the evaluation kit.

ORDERING INFORMATION

These kits may be ordered through your local Motorola Semiconductor sales office or authorized distributor. Ask your Motorola representative to order the kits from the finished goods warehouse, not the literature distribution center. Request the part number shown below.

Part Number	Description
MC145220EVK	Kit with the MC145220 installed.

REV 1
1/98 TN98012100

SECTION 1 – HARDWARE

FEATURES

1. The EVK is a complete working synthesizer, including VCOs.
2. Board is controlled by an IBM PC–compatible computer through the printer port.
3. Up to three boards can be operated independently through one printer port.
4. A prototype area and mounting holes are provided for VCOs, mixers, and amplifiers.
5. External reference input can be used.
6. Five element loop filter is included.
7. Frequency range of operation, step size and reference frequency can be changed in the control program.
8. Lock Detect, Out A, and Out B on any single board are accessible through the printer port.

CONTENTS OF EVALUATION KIT

1. Assembled evaluation board.
2. Nine–foot flat cable with four DB–25 male connectors.
3. MC145220EVK manual.
4. 3.5″ PC–compatible disk containing compiled program.
5. PLL device data sheets.

GETTING STARTED

To perform basic functions, do the following:

1. Plug in 12 volts at J8, observing the polarity marked on the board.
2. Short circuit section 1 of the DIP switch (S1) and open circuit all other sections.
3. Connect the supplied flat cable between the computer printer port and the DB–25 connector on the board (J9).
4. Type PLL at the DOS prompt. Then press enter.
5. Type the number that corresponds with the type of board given in the on–screen menu. The MC145220 may operate in single loop or dual loop mode. Then press Q.

You should now see the main menu displayed. There should be a signal present at J5 if single loop, or J12 if dual loop. The frequency will be the current output frequency given in the main menu. If the signal is not on the correct frequency, check to see if your printer port address is $278 (hexadecimal 278). If not, then select the P menu item and enter the correct address. After returning to the main menu, select the I menu item to send data to the board. You should now be on frequency.

MODIFICATIONS

The user may modify the hardware, such as utilizing a different VCO, by using the prototyping area of the board. After such modifications are made, the default values in the software may need to be changed. This is facilitated from the ‘Select from the available options’ screen.

Note that the on–board voltage regulators allow for a maximum VCO control voltage range of 0.5 – 4.5 volts.

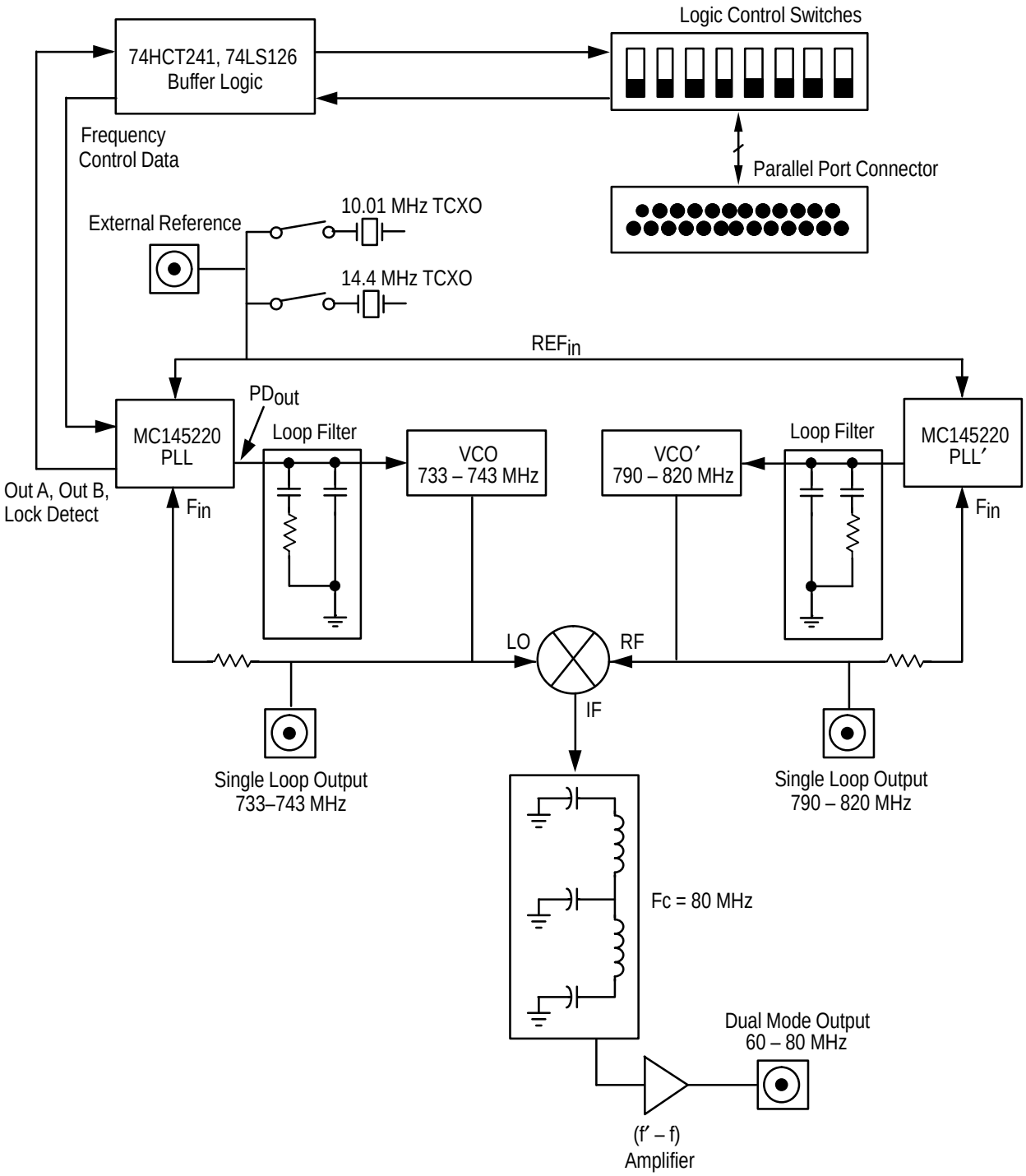

Figure 1. Evaluation Kit Block Diagram

TYPICAL PERFORMANCE

Typical performance applies only to the configuration as shipped. The MC145220EVK is shipped with V+ = 5 V. For lowest phase noise in single or dual loop mode, a 50 Ω load must be connected to J12.

	Single Loop PLL	Single Loop PLL′	Dual Loop PLL
Supply Voltage (J8)	11.5 – 12.5 V		
Supply Current (J8) (Note 1)	177 mA		
Available Current (Note 2)	45 mA		
Frequency Range (Note 3)	733 – 743 MHz	790 – 820 MHz	60 – 80 MHz
Reference Frequency (M1)	10.01 MHz		
Temperature Stability (M1, – 30°C to + 70°C)	< ± 2.5 ppm		
Reference Frequency (M5)	14.4 MHz		N/A
Temperature Stability (M5, – 30°C to + 85°C)	< ± 2 ppm		N/A
TCXO Aging (M1, M5)	< ± 1 ppm / year		
Step Size	10 kHz		10 Hz
Power Output	– 3.0 dBm	– 5.0 dBm	4.5 – 7.5 dBm
Frequency Accuracy	± 1.5 kHz	± 1.5 kHz	± 50 Hz
Reference Sidebands (Note 4)	– 57 dB	– 74 dB	– 57 dB
Phase Noise (100 Hz)	– 65 dBc/Hz	– 56 dBc/Hz	– 50 dBc/Hz
Phase Noise (10 kHz) (Note 5)	– 104 dBc/Hz	– 90 dBc/Hz	– 89 dBc/Hz
Switching Time (Note 6)	24 ms	40 ms	45 ms

NOTES:

1. Supply current is current the board requires without user modifications.
2. Available current is the sum of currents available to the user (in the prototype area) from the 5 V and 8.5 V supply. The 12 V supply is not regulated. Current at 12 V is limited by the external power supply. If the on–board VCO and amplifier are disconnected from the power bus, more current can be drawn in the prototype area. The current flowing into U5 (the 8.5 V regulator) should not exceed 180 mA. This will limit temperature rise in U5.
3. Frequency ranges require use of the 5 V default charge pump supply voltage.
4. VCO sidebands on PLL at low step sizes (10 kHz) are limited by control line leakage of the VCO. Up to 24 nA of leakage has been seen. At higher step sizes (100 kHz and above), this effect is much less noticable. This did not affect PLL′ because its VCO leakage was less than 10 pA.
5. 10 kHz phase noise is limited by the PLL device noise. For low noise designs, the loop bandwidth is made narrower and the VCO is relied upon to provide the 10 kHz phase noise. This can be seen on the EVKs since the VCOs have much lower noise.
6. 10 MHz step, within ± 1 kHz of final frequency (’220).
   Due to the software architecture, when the user is measuring the switching time of a single board in dual loop mode, it takes 20 ms to load the data as compared to single loop mode, which takes 8 ms to load the data. This is a limitation of the software, not the IC.
   To find the actual PLL switching time, subtract 8 or 20 ms from the switching time stated in the table.

SUPPORT MATERIAL

The following documents are included in the appendix:

1. Schematic diagram of MC145220EVK.
2. Bill of materials.
3. Parts layout diagram.
4. Mechanical drawing of board.
5. MC145220 data sheet.
6. Typical signal plots.

PRODUCTION TEST

After assembly is complete, the following alignment and test is performed:

1. The control program is started in ’220 single loop mode.
2. [L]! is selected to set PLL frequency to 733 MHz.
3. Power is applied to the board. DIP switch section 1 is closed circuit with all others being open circuit.
4. After attaching computer cable, [I]! is selected.
5. Trim resistor VR1 is adjusted to obtain an output frequency at J5 of 733 MHz $\pm$ 500 Hz.
6. Voltage at the control voltage test point (TP2) is measured. It must be > 0.5 V.
7. [H]! is selected.
8. Voltage at the control voltage test point (TP2) is measured. It must be < 4.4 V.
9. [T]! is selected to toggle to PLL′.
10. [L]! is selected to set PLL′ frequency to 790 MHz.
11. Voltage at the control voltage test point (TP9) is measured. It must be > 0.5 V.
12. [H]! is selected to set PLL′ frequency to 820 MHz.
13. Voltage at the control voltage test point (TP9) is measured. It must be < 4.4 V.
14. [G] is selected and the board type is changed to ’220 dual loop mode.
15. [Q]!, then [I]!, is selected to initialize the dual mode output (J12) to 70 MHz. The frequency should be 70 MHz $\pm$ 50 Hz.

If in step 5 it isn’t possible to obtain a signal on frequency, the adjustment screw in M1 may be turned for further frequency adjustment range. If neither adjustment works, [P] should be selected and the correct printer port address entered. [I]! is then selected to reload the data.

BOARD OPERATION

A computer is connected to the DB–25 connector J9. Data is output from the printer port. The printer card is in slot 0 using the default address in the control program. Data is sent to the PLL device (U1) through the DIP switch (S1), and 74HCT241 buffer (U2). D1, D2, D3, R7, R8, and R12 are in the data path between the ’HCT241 and PLL device. This limits the high level output voltage of the buffer. Voltage on PLL device inputs must be no greater than 0.5 V above V+. A ’220 PLL has three output lines which are routed through a 74LS126 line driver (U3) back to the computer.

U2, the 74HCT241, provides isolation and logic translation for PLL input lines. Logic translation is needed from the TTL levels on the printer port to the CMOS levels on the ’220 inputs.

A 12 V power supply should be used to power the board at J8 (Augat 2SV–02 connector). The 2SV–02 will accept 18–24 AWG bare copper power leads. No tools are needed for connection. If power is properly connected, LED D4 will be lit.

Power passes from J8 to U5 (LM317 regulator) configured as an 8.5 V regulator. 8.5 V powers the VCOs. Regulators U6 and U7 use the 8.5 V supply to produce 3 V and 5 V. The ’220 board can use either to power the logic and charge pump. V+ voltage is selected by J11. U6 and U7 are cascaded with U5 to equalize their individual voltage drops.

The ’220 operates in both a single loop and dual loop mode. There are no component changes between the two modes. The differences are in the programming of the counters and the SMA connector that is used.

The PLL loop is composed of the MC145220 (U1), 733 – 743 MHz VCO (M2), and a passive loop filter (R4, R5, C6, C7, C8). In single loop mode, output is taken from J5. A passive loop filter was used to keep the design simple, reduce noise, and reduce the quantity of traces susceptible to stray pickup. The PLL′ loop is composed of the MC145220 (U1), 790 – 820 MHz VCO (M3), and a passive loop filter (R22, R25, C24, C26, C30). In single loop mode, output is taken from J10.

Dual mode output is the (f′ – f) frequency output from the mixer. It is low pass filtered (L1, L2, C15, C21, C22) then amplified (U4). The output is available at J12.

Phase detector current is 2 mA. J1 is a removable jumper used for current measurement of V+.

Two TCXOs, a Motorola Saber 14.4 MHz (M5), and Raltron 10.01 MHz (M1) are supplied. As shipped from the factory, the 10.01 MHz TCXO is in use. This allows both the 10 kHz and 10 Hz step sizes to be used with one TCXO. 10.01 MHz cannot be divided for larger step sizes such as 100 kHz. For larger step sizes use the Saber. Jumpers J3, J4, J13, and J14 determine which TCXO or the external reference input is in use.

DUAL MODE OUTPUT

The dual mode output (J12) is the difference frequency from mixing PLL and PLL′. By using a reference frequency of 10.01 MHz, PLL can be operated with a 10.01 kHz step size and PLL′ with a 10 kHz step size. If both PLL and PLL′ step down in frequency, the mixed output will step up by 10 Hz. More information on the offset reference technique is in **AN1277/D, Offset Reference PLLs for Fine Resolution or Fast Hopping**. The block diagram, formulas, and an example are shown in Figure 2.

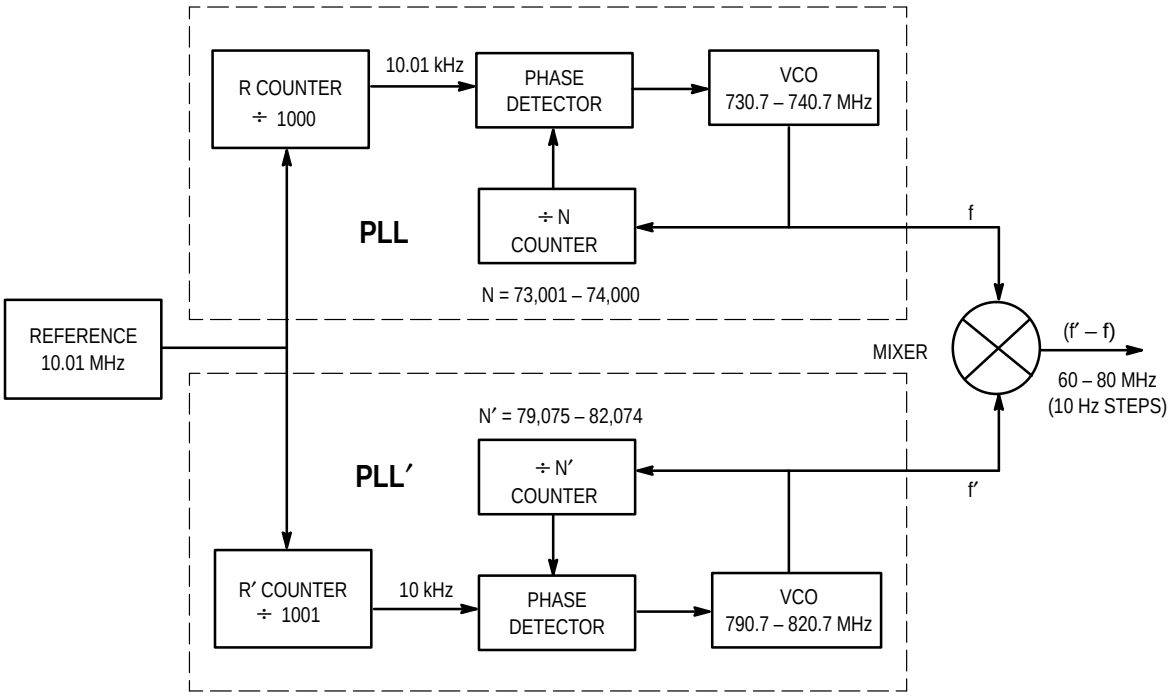

Figure 2. Dual Mode Block Diagram

PLL	PLL′
$f = N\ (10.01\ kHz)$	$f' = N'\ (10\ kHz)$
$f = 10.01\ kHz \left[74{,}000 - \frac{r(f' - f)}{10\ Hz}\right]$	$f' = 10\ kHz \left[\frac{w(f' - f) + 740\ kHz}{10\ kHz} + N\right]$
$N = 74{,}000 - \frac{r(f' - f)}{10\ Hz}$	$N' = N + 74 + \frac{w(f' - f)}{10\ kHz}$
$(f' - f) = w(f' - f) + r(f' - f)$	
$(f' - f)$ = Desired Output Frequency	
$w(f' - f)$ = Output Frequency Portion that Divides Evenly by 10 kHz	
$r(f' - f)$ = Remainder from Output Frequency Division by 10 kHz	

Dual Mode Formulas

Example: Synthesize 76.849 930 MHz

$r(f' - f) = 9.930\ kHz$, $w(f' - f) = 76.840\ MHz$

$N = 74{,}000 - \frac{9.930\ kHz}{10\ Hz} = 73{,}007$ $f = 73{,}007\ (10.01\ kHz) = 730.800\ 070\ MHz$

$N' = 73{,}007 + 74 + \frac{76.840\ MHz}{10\ kHz} = 80{,}765$ $f' = 80{,}765\ (10\ kHz) = 807.650\ 000\ MHz$

$(f' - f) = 807.650\ 000\ MHz - 730.800\ 070\ MHz = 76.849\ 930\ MHz$

EXTERNAL REFERENCE INPUT

To use an external reference, disconnect J3, J4, J13, and J14. Use a reference signal at J2 which complies with data sheet requirements. Then modify the reference frequency in the program main menu to reflect the changes made (F menu item).

DATA TRANSFER FROM COMPUTER TO EVK

To control the serial input EVK with the parallel printer port, a conversion is done. Printer cards are designed to output eight bits through eight lines. A bit mask is used to obtain the bit combination for the three required output lines (Data, Clock, Load). As bytes are sent to the printer card in sequence, it appears to be a serial transfer. The printer port is used because data transfer using the serial port would be much slower. A standard IBM PC can support a parallel port data rate of 4.77 MHz.

IBM PCs and compatibles can accept up to three printer port configurations. These ports are called LPT1, LPT2, and LPT3. Each printer port has a unique address. Two sets of addresses are in common use. One set applies to IBM PC XT, AT, and clones. The other is for the PS 2 line. To load data into the EVK, the correct address must be selected. The program default is $278. If $278 is not the address in use, it must be modified by entering the P menu item in the main menu. All allowed addresses given in hexadecimal are as follows:

Label	IBM PC and Clones	PS 2
LPT1	278	3BC
LPT2	378	378
LPT3	3BC	278

Up to three EVK boards can operate independently from one printer port. All lines on the printer port are connected to every EVK. Even with three boards operating, only three output lines (Clock, Data, and Load) from the printer card are used. If two boards are controlled together, data for the second board is received from the Output A of the first. Output A is a configurable output on ’220 devices, which in this case is used to shift data through chip 1 into chip 2. Output A and Data are connected using a printer port input line. This was done to avoid connecting extra wires. Fortunately not all port input lines are needed for computer input. Load and Clock are common to both boards.

A three–board cascade is handled similarly to a two–board cascade. Out A on the first board is fed to Data on the second. Out A on the second connects to Data on the third. Instructing the program on the quantity of boards connected together allows it to modify the number of bits sent.

All boards have a DIP switch S1 which gives each a unique address. The configuration menu is used to tell the program what type of board is connected at a board address. Switch positions for all possible addresses are given in Figure 3.

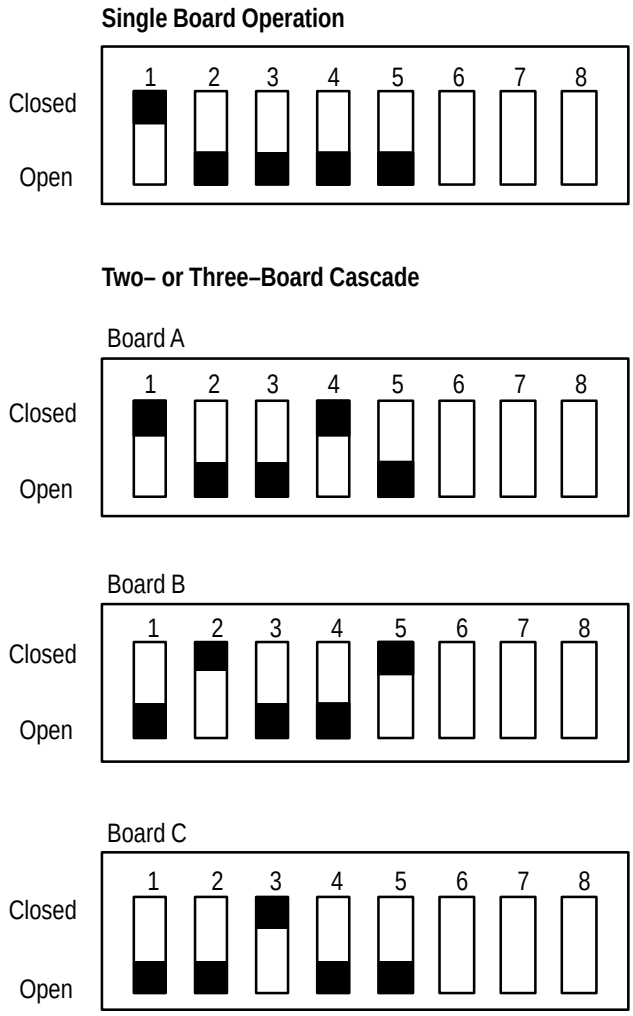

Figure 3. Switch Positions

In Figure 3, DIP switch sections 6, 7, and 8 allow the computer to read Out A, Lock Detect′, or Lock Detect from the PLL device. Each of the inputs can only be read on one board at a time, but each item could be read on a different board. In a three–board cascade, Out A could be read from the first board, Out B from the second, and Lock Detect from the third. There is no way to determine the board address of a particular input with software. The control program does not make use of these inputs; however, source code could be modified as required. Pin assignment on the printer port connector is:

Label	Pin Number
Out A	12
Out B	13
Lock Detect	15

PRINTER PORT CONFIGURATION

Printer port outputs on an IBM PC or clone use TTL–LS logic levels. Inputs are one TTL–LS load. Signal lines can be used for any purpose. The standard names, direction of data flow, true and inverted data are shown in Figure 4.

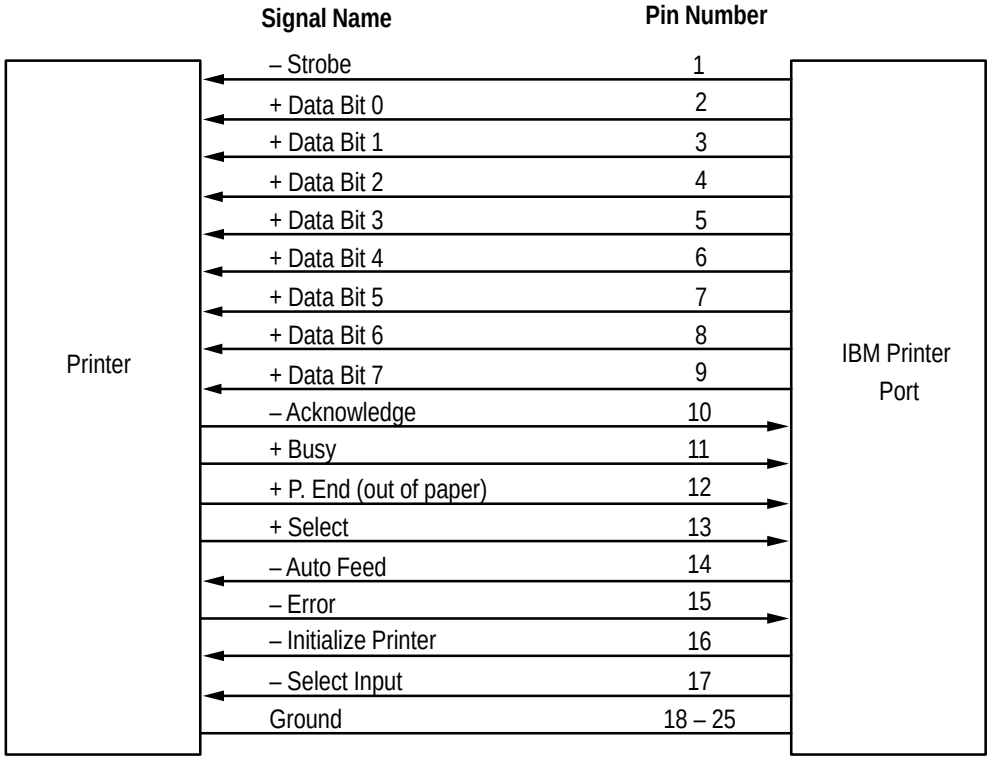

Figure 4. Printer Port Data Lines

Pin numbers for the port connector are shown in Figure 5.

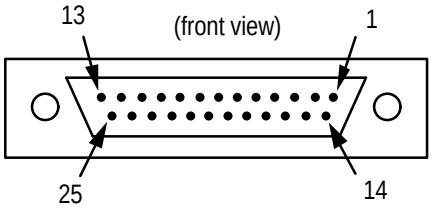

Figure 5. DB–25 Male Connector

SECTION 2 – SOFTWARE DESCRIPTIONS SUMMARY

INTRODUCTION

The MC145xxx EVK control program is used to program all PLL evaluation kits. It will simultaneoulsy control up to three different boards independently from one printer port. All features of the PLL device may be accessed. Default frequencies can be modified to allow use of different channel spacings and VCOs.

User input errors are detected and appropriate messages are displayed.

To show the format of the program, a sample screen is shown below:

‘Select from the available options’

```
                    Welcome to MC145xxx EVK Demonstration Program, rev 4.0
                              Select from the available options

Available Boards – Current target board is: A, MC145220 Dual
 Brd [A]!: MC145220 Dual    Brd [–]!: N/A            Brd [–]!: N/A
--------------------------------------------------------------------------------
MC145xxx Frequency Commands – Current Output Frequency is 70 MHz
 [L]! Set to low freq.     60 MHz [W] Change default low freq.
 [M]! Set to med. freq.    70 MHz [Y] Change default med. freq.
 [H]! Set to high freq.    80 MHz [Z] Change default high freq.
 [U]! Step frequency up by step size    [O] Set PLL output frequency
 [D]! Step frequency down by step size  [F] REFin freq. & channel spacing
MC145xxx Additional Commands
 [E]  Set function of output A          [N] Change C register and Prescale
 [R]  Set crystal/reference mode – Current mode is Ref. mode, REFout low


--------------------------------------------------------------------------------
Initialization/System Setup Commands:
 [P]  Set output port address – Current address is $278
 [G]  Change board definitions
 [I]  Initialize board(s), Write all registers

                [X]! Terminate demonstration program. [?]! View help screen.
```

APPENDIX

MC145220 PLL Evaluation Board

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MC145220EVK Signal Plot — Dual Loop Mode Output at 70 MHz

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MC145220EVK Signal Plot — Single Loop Mode PLL on 805 MHz

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MC145220EVK Signal Plot — Single Loop Mode PLL on 738 MHz

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