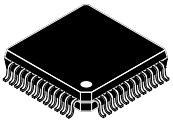
MC141622

Advance Information

Advanced Comb Filter-II (AFC-II)



P SUFFIX
48–LEAD QFP
CASE 898

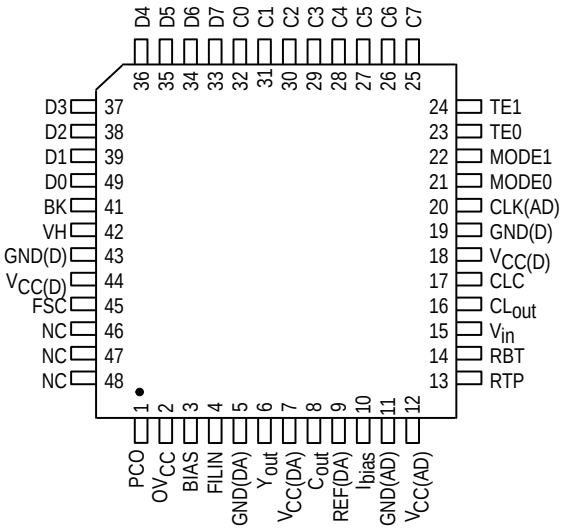
ORDERING INFORMATION

MC141622FU
Quad Flat Package (QFP)

The Advanced Comb Filter–II is a video signal processor for VCRs and TVs. It's function is to separate the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–II minimizes dot–crawl and cross–color. A built–in PLL provides a 4xfsc clock from either an NTSC subcarrier signal or a 4xfsc input. This allows a video signal input of an extended frequency bandwidth. The built–in vertical enhancer circuit improves the quality of the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

- Built–in High Speed 8–Bit A/D Converter
- Two Line Memories (1820 Bytes)
- Advanced Comb–II Process
- Vertical Enhancer Circuit
- Two High Speed 8–Bit D/A Converters
- 4xfsc PLL Circuit
- Built–in Clamp Circuit
- Digital Interface Mode
- On–Chip Reference Voltage Regulator for A/D Converter

PIN ASSIGNMENT



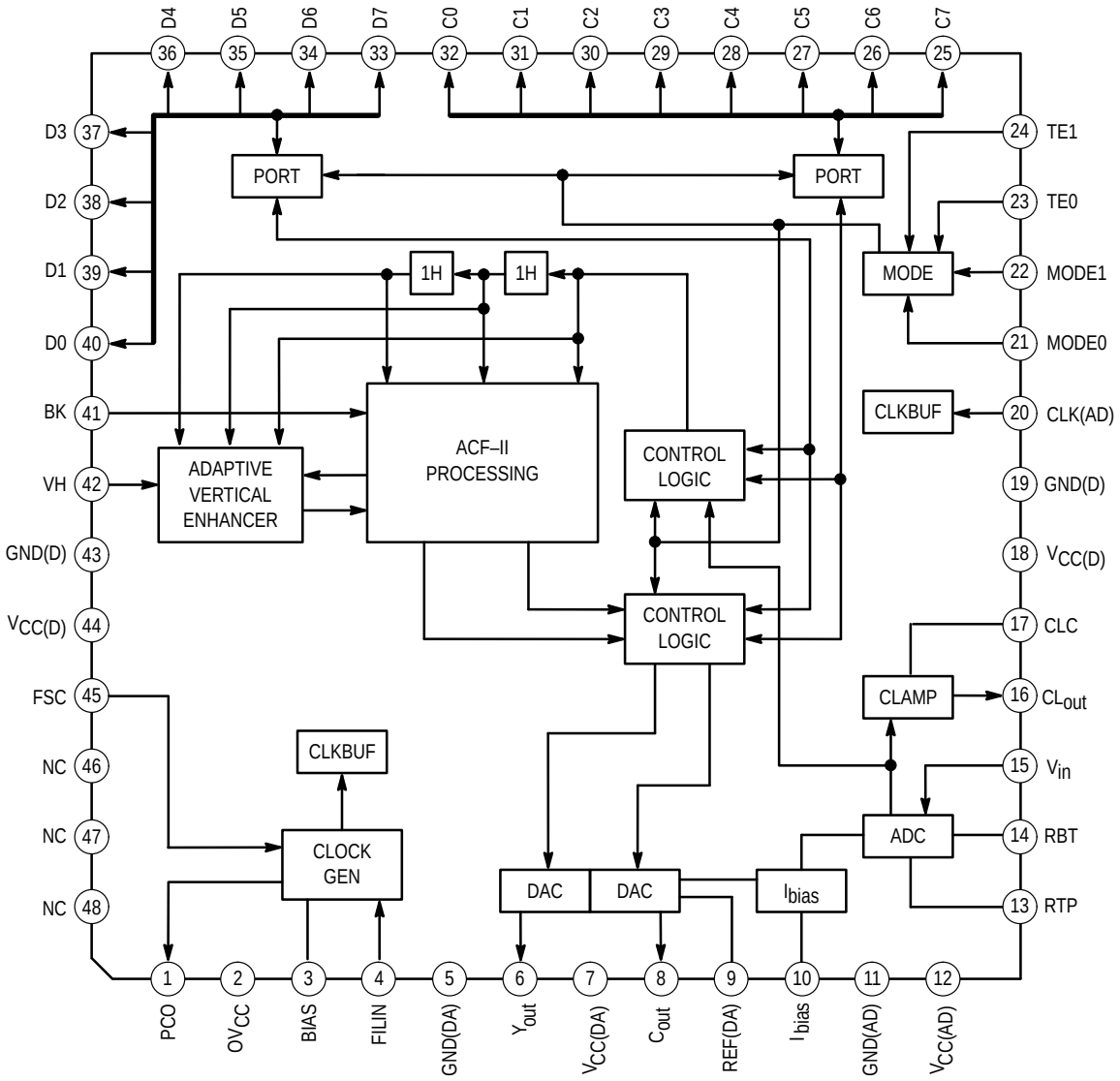
NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
1/97 TN97012000

MOTOROLA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND)	V_{CC}	– 0.5 to + 7.0	V
DC Input Voltage (Referenced to GND)	V_{in}	– 1.5 to V_{CC} + 1.5	V
DC Output Voltage (Referenced to GND)	V_{out}	– 0.5 to V_{CC} + 0.5	V
DC Input Current (per pin)	I_{in}	± 20	mA
DC Output Current (per pin)	I_{out}	± 25	mA
Power Dissipation	P_D	750	mW
Storage Temperature	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Operating Supply Current	I_{CC}	—	115	140	mA	1
Operating Power Dissipation	P_D	—	575	735	mW	1
Ambient Operating Temperature	T_A	– 20	—	75	°C	

NOTE:
1. At normal mode.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit	Notes
Subcarrier Input Frequency		f_c	—	3.579545	—	MHz	1
Clock Frequency		CLK	—	14.31818	—	MHz	2
FSC Clock Input Level		V_{fc}	1	—	—	V p-p	3
High Level Input Voltage	CLK(AD)	V_{ICH}	3.15	—	—	V	4
Low Level Input Voltage	CLK(AD)	V_{ICL}	—	—	1.1	V	4
Clock Duty Cycle	CLK/CLK(AD)	Dty	45	50	55	%	4

NOTES:
1. Color subcarrier input [FSC = (455/2)fh] locked on the burst signal of the input video signal. AC coupling input by external capacitor.
2. The internal circuit operates by four times clock using FSC–pin input at normal (FSC) mode.
3. Sine wave input.
4. CLK(AD) is available only during digital input comb filter mode.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	± 1.5	± 2.5	LSB
Differential Nonlinearity	DNL	—	± 0.5	± 1.0	LSB
Top Reference Level	V_{TPS}	4.5	4.6	4.7	V
Bottom Reference Level	V_{BTS}	1.45	1.55	1.65	V
Maximum Analog Input Range During Self Reference	V_{ins}	2.85	3.05	3.25	V p-p

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High Level Input Voltage	MODE0, MODE1, TE0, TE1, BK, C0 – C7, D0 – D7	V_{IH}	3.15	—	—	V
Low Level Input Voltage	MODE0, MODE1, TE0, TE1, BK, VH, C0 – C7, D0 – D7	V_{IL}	—	—	1.1	V
Input Leakage Current [V_{in} = $V_{CC(D)}$ or GND(D)]	MODE0, MODE1, TE0, TE1, BK VH C0 – C7, D0 – D7	I_{inl}	—	—	± 10	µA
Data Setup Time (at Digital Input Comb Filter Mode)	D0 – D7	t_{ds}	0	—	—	ns
Data Hold Time (at Digital Input Comb Filter Mode)	D0 – D7	t_{dh}	20	—	—	ns
Data Input Rise Time (at Digital Input Comb Filter Mode)	D0 – D7	t_r	—	—	10	ns
Data Input Fall Time (at Digital Input Comb Filter Mode)	D0 – D7	t_f	—	—	10	ns
Output Data Delay (at Digital Input/Output Comb Filter Mode)	C0 – C7, D0 – D7	t_{dl}	—	45	—	ns

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Y/C Separation	—	40	—	—	dB
Band-Pass Filter Bandwidth (at – 3 dB)	—	—	± 0.75	—	MHz

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	—	± 1	LSB
Differential Nonlinearity	DNL	—	—	± 0.5	LSB
Analog Output Voltage, Y_{out}	V_{YO}	1.1	1.2	1.3	V p-p
Analog Output Voltage, C_{out}	V_{CO}	1.1	1.2	1.3	V p-p
Full Scale Voltage, Y_{out}	V_{YFS}	1.3	1.5	1.7	V
Full Scale Voltage, C_{out}	V_{CFS}	1.3	1.5	1.7	V
Zero Scale Voltage, Y_{out}	V_{YZS}	0.1	0.3	0.5	V
Zero Scale Voltage, C_{out}	V_{CZS}	0.1	0.3	0.5	V
Output Impedance	Z_O	—	100	300	Ω

CLAMP CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clamp Mode Output Voltage*	V_{clys}	—	1.6	—	V

* At using the clamp circuit when connecting V_{in} – CL_{out}.

BK/VH CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
BK Switching Time, at Normal Mode		—	9	—	Clock
VH Switching Time, at Normal Mode		—	9	—	Clock

VERTICAL ENHANCER LEVEL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Noise Slice Level, at Normal Mode		0	—	15	bit
White Enhance Level, at Normal Mode		0	—	15	bit
Black Enhance Level, at Normal Mode		0	—	15	bit

GENERAL SIGNAL DELAY (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode, 938 Clock		—	65.511	—	μs

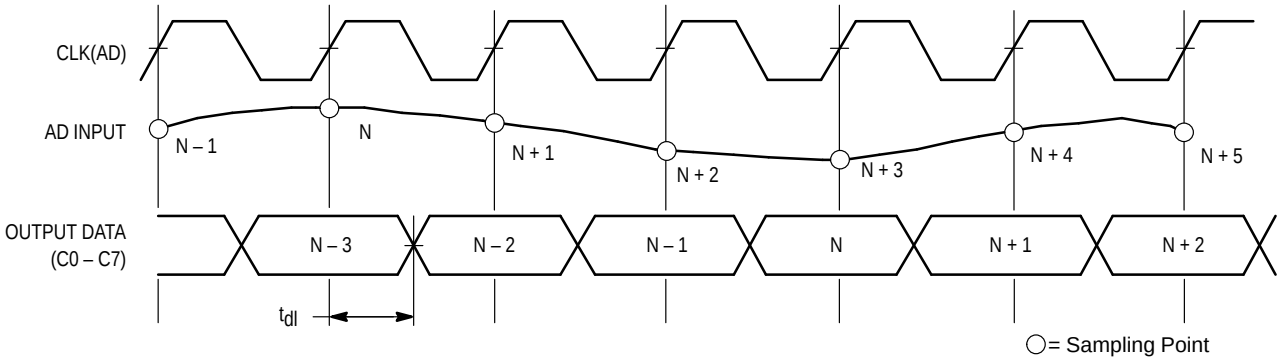


Figure 1a. A/D Converter Timing Diagram (During Digital Input Comb Filtering Mode)

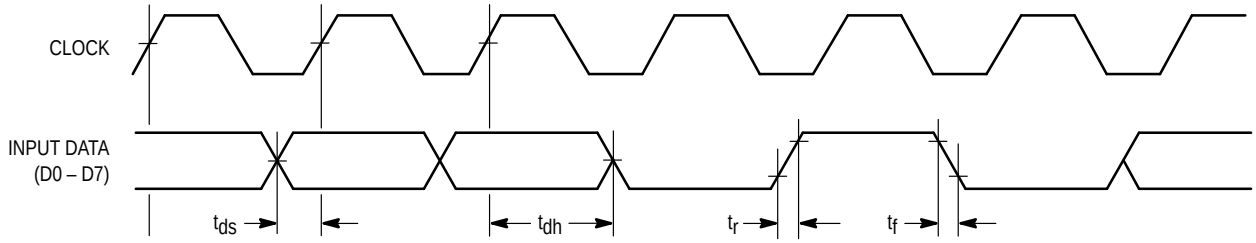


Figure 1b.Digital Signal Input Timing Diagram (During Digital Input Comb Filtering Mode)

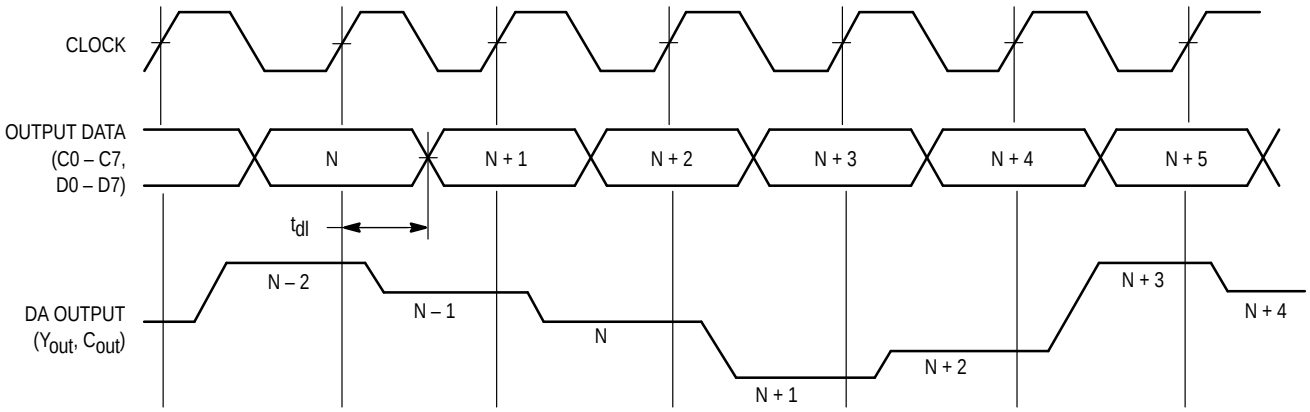


Figure 1c. Output Signal Timing Diagram (During Digital Output Comb Filtering Mode)

Figure 1. Timing Diagrams

Clamp Circuit Characteristics (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Clamp Mode Output Voltage, V_{cly} (Non-input when connecting V_{in} – CL_{out})

$V_{cly} = (V_{TP} - V_{BT})\ (N + 1) / 256 + V_{BT} \pm 50$ mV

where N = Clamp Code Input (N < 255)

- If the calculated value of the output voltage, $V_{cly} > V_{clys}$, then $V_{cly} = V_{clys}$
- Clamp Value N is fixed, N = 4.

PIN DESCRIPTIONS

Pin	Pin Name	Function
1	PCO	Phase comparator output.
2	OV_{CC}	Power supply for VCO.
3	BIAS	Reference for VCO. Generally connected to GND(D) through an external resistor.
4	FILIN	VCO controlled voltage input. Generally connected to PCO through an external loop filter.
5	GND(AD)	GND for D/A converter.
6	Y_{out}	Luminance signal output.
7	$V_{CC(DA)}$	Power supply for D/A converter.
8	C_{out}	Chrominance signal output.
9	REF(DA)	Reference for D/A converter. Generally connected to GND(DA) through a multilayer ceramic capacitor (0.1 μF).
10	I_{bias}	Bias circuit current control for A/D, D/A converters. Generally connected to GND(DA) through an external resistor.
11	GND(AD)	GND for A/D converter.
12	$V_{CC(AD)}$	Power supply for A/D converter.
13	RTP	Top reference for A/D converter. Supplies top reference voltage internally.
14	RBT	Bottom reference for A/D converter. Supplies bottom reference voltage internally.
15	V_{in}	A/D converter input.
16	CL_{out}	Voltage output for clamp. Clamps an input signal by connecting with V_{in} and inputting the video signal by ac coupling.
17	CLC	Clamp time constant setting pin.
18	$V_{CC(D)}$	Power supply for digital circuit.
19	GND(D)	GND for digital circuit.
20	CLK(AD)	CLK input for A/D converter. Available only during digital input comb filtering mode and a portion of test mode. Input level is CMOS level.
21, 22	MODE0, MODE1	Mode input. GND level during normal (FSC) mode.
23, 24	TE0, TE1	Test mode input. Generally GND level.
25	C7	Digital interface 1, input/output. Generally $V_{CC(D)}$ level.
26 – 28	C6 – C4	Digital interface 1, input/output. Generally GND(D) level.
29	C3	Digital interface 1, input/output. Generally $V_{CC(D)}$ level.
30 – 32	C2 – C0	Digital interface 1, input/output. Generally GND(D) level.
33	D7	Digital interface 2, input/output. Generally $V_{CC(D)}$ level.
34 – 40	D6 – D0	Digital interface 2, input/output. Generally GND(D) level.
41	BK	Non–color signal processing mode. Generally GND(D) level.
42	VH	Vertical enhancer circuit mode. Generally GND(D) level.
43	GND(D)	GND for digital circuit.
44	$V_{CC(D)}$	Power supply for digital circuit.
45	FSC	CLK input. AC coupling input by external capacitor. Normal (fsc) mode: Subcarrier. Normal (4xfsc) mode: 4* Subcarrier.
46 – 48	NC	No connection. Generally GND level.

Figure 2 shows the I/O signals of the Advanced Comb Filter–II.

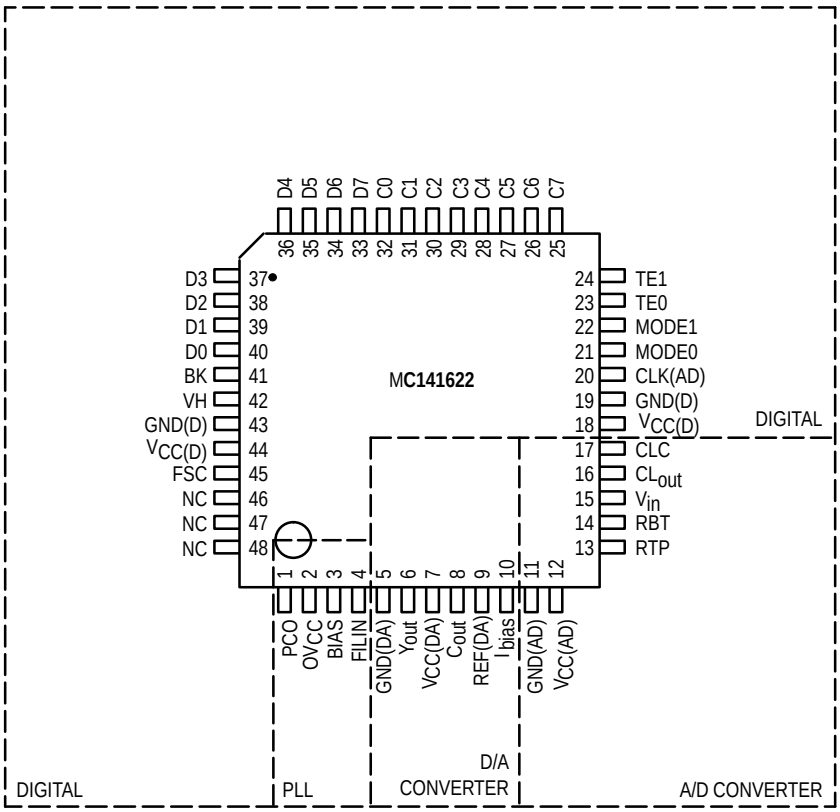


Figure 2. Pin Assignment

DEVICE DESCRIPTION

INTRODUCTION

The Advanced Comb Filter–II (ACF–II) is a high–performance HCMOS digital filter with built–in A/D and D/A converters. The basic function of the chip is the separation of the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–II minimizes the problems often generated by Y/C separation such as dot–crawl and cross–color. It uses a 14.3 MHz clock that allows an extended frequency bandwidth video signal to be input. This Y/C separation is realized by the digital advanced comb filters. The built–in 4xfsc PLL circuit allows a subcarrier signal input, from which a 4xfsc clock is generated for video signal processing. This allows a video signal input of an extended frequency bandwidth. The built–in vertical enhancer circuit can enhance the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

ADVANCED COMB FILTER–II DESCRIPTION

The simplified block diagram of the Advanced Comb Filter–II chip is shown at the beginning of this data sheet. There are five major functions represented in this block diagram. The first block is the A/D conversion block. The high speed 8–bit binary analog–to–digital converter converts the incoming analog video signal to an 8–bit binary data stream. The conversion frequency is 14.3 MHz which is four times the color subcarrier frequency.

The second block contains the Advanced Comb Filter–II algorithm. The digital data from the A/D converter is processed by the algorithm of the Advanced Comb Filter–II. The composite video is filtered by the band–pass filter (BPF) and separated into the Luminance Y and Chrominance C signals.

The third block is the vertical enhancer circuit block. This vertical enhancer emphasizes the picture outline of the vertical direction.

The fourth block is the digital–to–analog conversion block. Two 8–bit D/A converters convert the luminance and chrominance into analog outputs. The conversion frequency is four times the subcarrier signal (14.3 MHz). The chrominance analog output is biased with a dc offset of half the value of the DA converter reference.

The fifth block is a 4xfsc CLK generation circuit. This block generates four times the subcarrier signal and phase locks the inputting subcarrier on FSC pin.

A/D Converter

The composite video signal input is converted to the digital code by the high speed 8–bit A/D converter. The A/D converter reference has a self–bias function which generates V_{TP} = 4.6 V, V_{BT} = 1.55 V. This allows the A/D converter to function without an external reference circuit.

Clamp Voltage Regulating Circuit

The clamp voltage regulating circuit sync tip clamps the input signal when the V_{in} pin is connected to the CL_{out} pin and the video signal is input using ac coupling. It compares the

digital value of the clamp level ($04) with the A/D converter output code. The clamp voltage from CL_{out} is then output.

Advanced Comb Filter–II

The Advanced Comb Filter–II is a digital comb filter developed for use in the NTSC system. The vertical correlation circuit provides high picture quality and high resolution and requires no adjustment for its Y/C separation. The clock frequency is 14.3 MHz, which is four times the NTSC subcarrier.

The BK pin can be used to select between the composite signal output without Y/C separation and the Y/C signal output. Table 1 shows the relationship of the BK pin and each output.

Table 1. BK Function

BK Pin	Y_{out}	C_{out}
L	Luminance	Chrominance
H	Composite	Chrominance

Adaptive Vertical Enhancer Circuit

The vertical enhancer circuit is used the adaptive enhanced processing using two line memories. The adaptive LPF of the vertical enhancer circuit minimizes noise and dot–crawl. This block does not emphasize horizontal and vertical sync signals. Table 2 shows the relationship of the VH pin and the vertical enhancer function. The coring characteristics of the vertical enhancer circuit can be set up on the digital port at the normal mode.

Table 2. VH Function

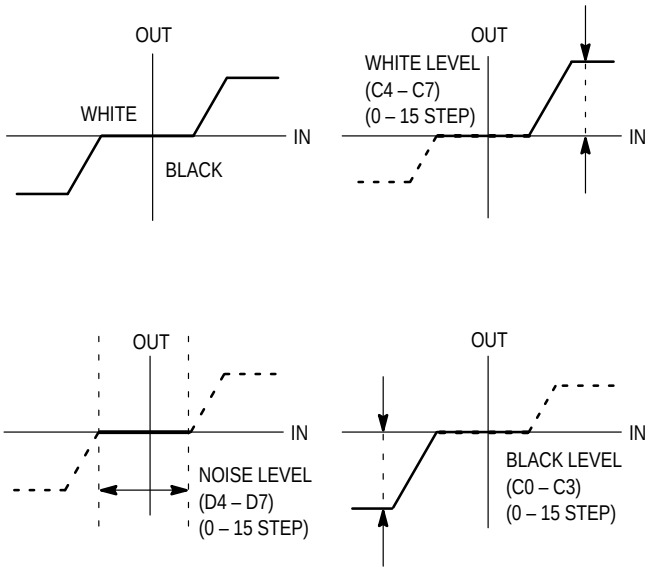
VH Pin	Vertical Enhancer
L	On
H	Off

D/A Converter

The luminance and chrominance signals separated in the advanced comb filtering portion are converted to analog signals by two 8–bit D/A converters. The output voltage range is from 0.3 V to 1.5 V, 1.2 Vp–p. The sampling clock of the D/A converter is 14.3 MHz.

Clock Generation Circuit

The internal PLL can be selected to operate in either of two modes; an X4 mode used to generate a 4xfsc clock from a normal NTSC color subcarrier, and an X1 mode when a 4xfsc signal is available.



C7	C6	C5	C4	
C3	C2	C1	C0	
D7	D6	D5	D4	Level
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

Figure 3. Coring Characteristics

OPERATING MODES

The Advanced Comb Filter–II can be operated in any of four modes. These modes are fixed by a digital code input into MODE0 and MODE1. The descriptions of the four types of operating modes are:

Normal (fsc) Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the fixed value $04. The coring characteristics of the vertical enhancer circuit can be set up on the digital port. This mode is used when an NTSC color subcarrier is used to generate a 4xfsc using the internal PLL.

Normal (4xfsc) Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the fixed value $04. The coring characteristics of the vertical enhancer circuit can be set up on the digital port. In this mode an external 4xfsc CLK is input on the FSC pin.

Digital Input Comb Filtering Mode

In this mode, the comb filter is used as two separate blocks; the A/D converter portion, and the filter and D/A portion. This mode can re–input and filter converted digital data outputs by the A/D converter after arbitrarily being digitally processed by external circuits. The converted digital data outputs into C0 – C7. Moreover, the data input into D0 – D7 is filtered by the ACF–II algorithm, and is output as an analog signal from Y_{out} and C_{out}. The two blocks can operate independently with different frequency and phase clock signals. The CLK(AD) pin is the clock input to the A/D converter block and the CLK pin the clock source (4xfsc) for the filter and D/A converters. At this time, the clamp circuit works as sync tip clamp when CL_{out} is connected to V_{in}, and clamps the input video signal to the internally fixed digital value ($04).

Digital Output Comb Filtering Mode

This mode outputs digital values of the luminance and chrominance signals in addition to functioning as a standard analog output Y/C separator. This allows arbitrary digital processing of the filter–processed Y and C digital outputs by an external circuit. It interfaces with an analog circuit easily, since both analog Y and C signals are output at the same time.

The video signal input to the A/D converter is converted to digital data, and forwarded to the filter portion. The Y/C separated data from the filter portion is output from Y_{out} and C_{out} after the D/A conversion. At the same time, the filter portion output is also forwarded to the digital interface and the luminance digital value is output from C0 – C7 and the chrominance digital value is output from D0 – D7. With this mode, the clamp circuit works as a sync tip clamp with CL_{out} connected to V_{in}, and clamps the input video signal internally to the fixed digital value ($04). This mode operates with an external 4xfsc CLK which is input on the FSC pin.

Table 3 shows the relationship between the MODE pin and MODE condition.

Table 3. Operating MODE Switching Function

Mode	MODE1	MODE0
Normal (fsc) Mode	L	L
Normal (4xfsc) Mode	L	H
Digital Input Comb Filtering Mode	H	L
Digital Output Comb Filtering Mode	H	H

APPLICATION DESIGN CONSIDERATIONS

V_{CC}, GND

To maximize the performance of the MC141622, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC141622. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC141622, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

A 1–inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 μF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high–capacity and high–frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

V_{in}

In order to prevent flyback noise on the video input, it is necessary to keep the bandwidth to less than 1/2 the clock frequency by using an area filter. Here the amplifier used as an input buffer needs a wide bandwidth and driving capability. Moreover, to minimize external noise effects, drive the V_{in} pin with a low impedance amplifier and keep the V_{in} pin as close as possible to the amplifier output.

When using the built–in clamp circuit, connect CL_{out} with V_{in} and input signals after ac coupling by using a high–performance, high frequency capacitor of 1 to 0.1 μF. In this case, keep the V_{in}, CL_{out}, coupling capacitor, and buffer–amplifier wiring as short as possible. Pay attention to the external noise and parasitic impedance.

AD Reference Pin

The RTP and RBT pins have a self–bias function that internally generates V_{TP} = 4.6 V and V_{BT} = 1.55 V. It acknowledges the AD converter analog input dynamic range. A stable performance can be achieved by applying a high–performance frequency capacitor as close as possible to the RTP and RBT pins and bypassing to GND(AD). A 0.1 μF multi-layer ceramic capacitor and a 10 μF tantarum capacitor are recommended.

CLC

The CLC pin sets the clamp circuit speed with an external capacitor and resistor.

Generally, the capacitor and resistor are arranged in a row and connected with GND(AD). Select a capacitor that minimizes the dielectric absorbing error. When the capacitor capacity is reduced, the shift speed of the video signal to $V_{CC(AD)}$ side is accelerated. If the resistor value is too small at this point, sagging will appear in the video signal. Also, if the capacitor's capacity is too large, the clamp speed will slow down; therefore, it is very important to pay attention to the setup of the resistor capacitor values.

DA Reference

REF(DA) is a DA converter reference decoupling pin for both the Y_{out} and C_{out}. Bypass to GND(DA) by applying a high–performance, high–frequency capacitor as close to the pin as possible. A 0.1 μF multilayer ceramic capacitor is recommended.

Clock Input

The clock frequency input is 3.58 MHz during normal (fsc) mode, and 14.31818 MHz during the other modes. The minimum input level is 1.0 Vp–p. It should be phase locked to the subcarrier of the video signal.

The clock line should be wired with the shortest wire and be separated from other circuits to minimize cross coupling to other signals. The CLK(AD) pin is used only during digital input comb filtering mode; therefore, it should be at GND level unless the device is used in the digital input comb filtering mode.

I_{bias}

The I_{bias} pin is used to set up the bias current for the AD and DA converters. Connect an external resistor between the I_{bias} and GND(DA).

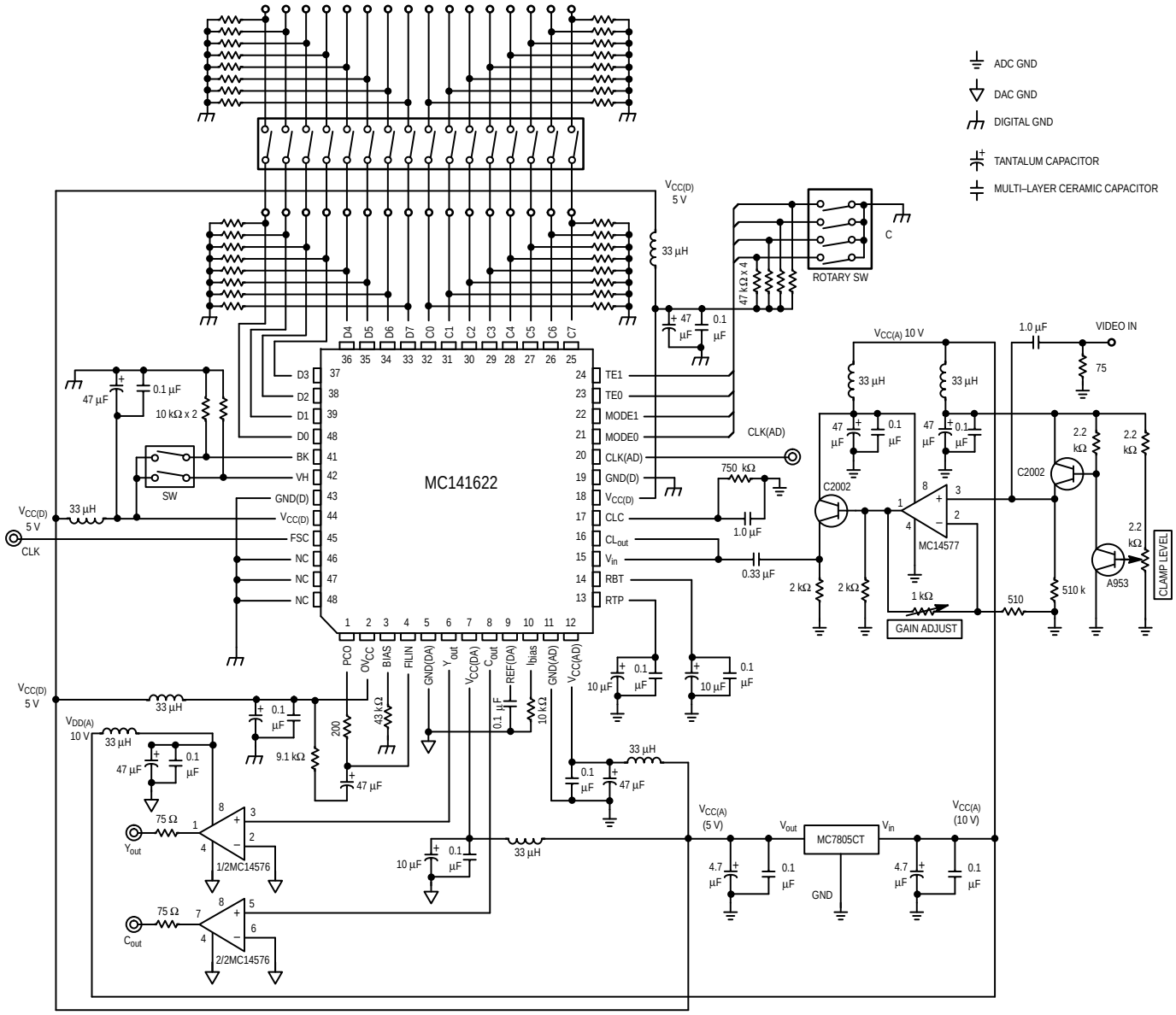
Digital Input Comb Filtering Mode

Connect CLK(AD) with the GND(D) when the AD converter is not being used. Connect D0 – D7 with GND(D), when the DA converter and filter are not being used. This is to eliminate any unnecessary operation of blocks which are not being used. At this point, make sure voltage is supplied to the $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$. This eliminates latch–up during operating.

Latch–Up

The $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins connect to power supplies that are independent from each other. Therefore, latch–up may occur when the power is applied. To eliminate latch–up, apply power to $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins simultaneously.

APPLICATION CIRCUIT



EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 4 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over–etching and process errors may remove ground between pins. If sufficient ground around enough pins is removed, the ground system can become isolated or nearly isolated “patches” which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a “L”, “T” or “PI” arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An “island” is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 5. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 5. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

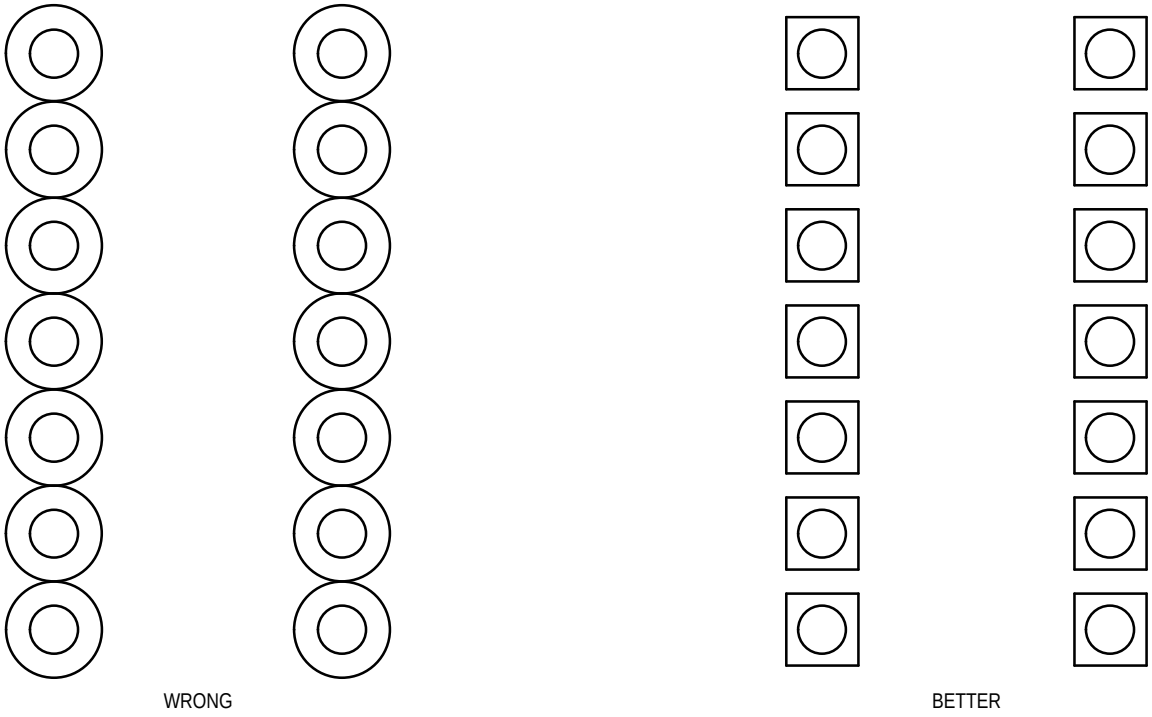


Figure 4.

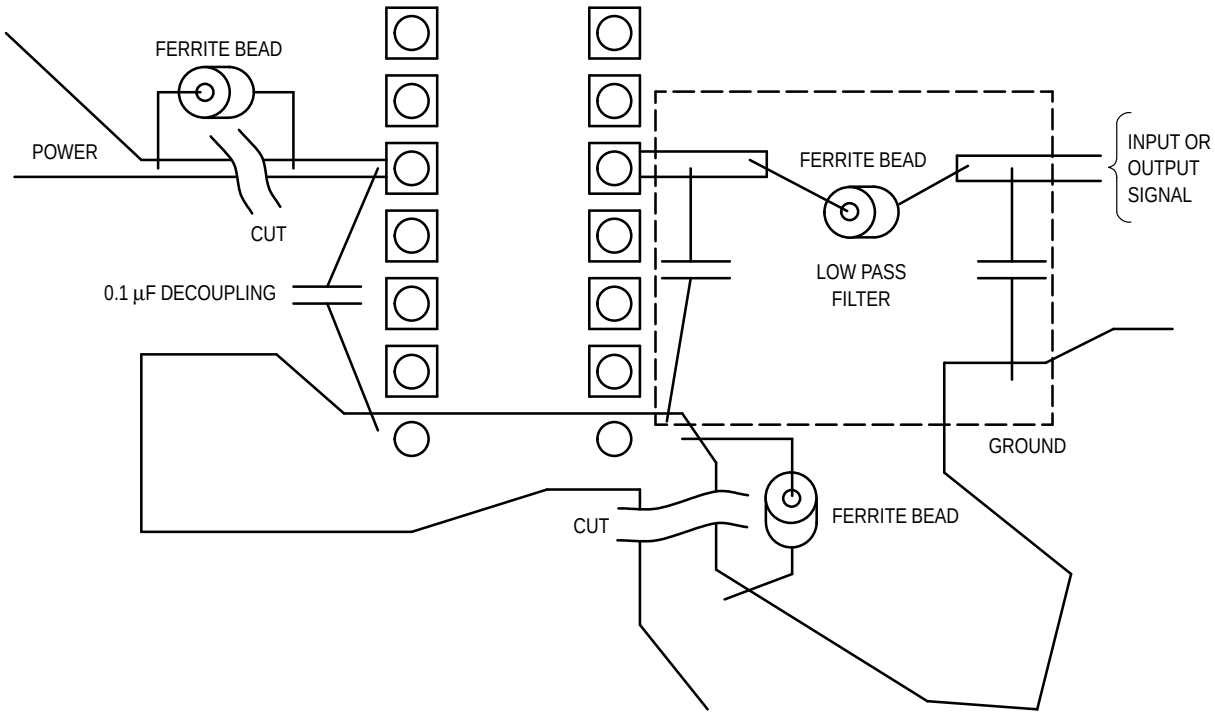
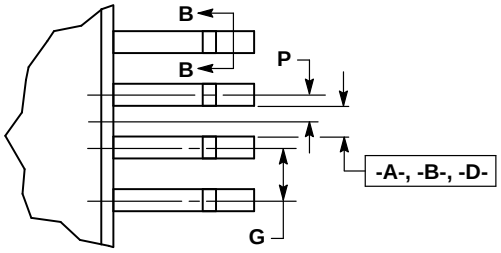


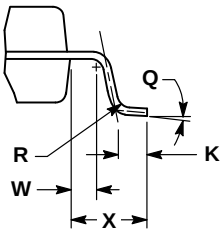
Figure 5.

PACKAGE DIMENSIONS

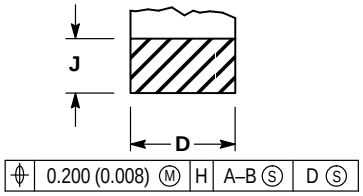
FU SUFFIX
48-LEAD QFP
CASE 898-01



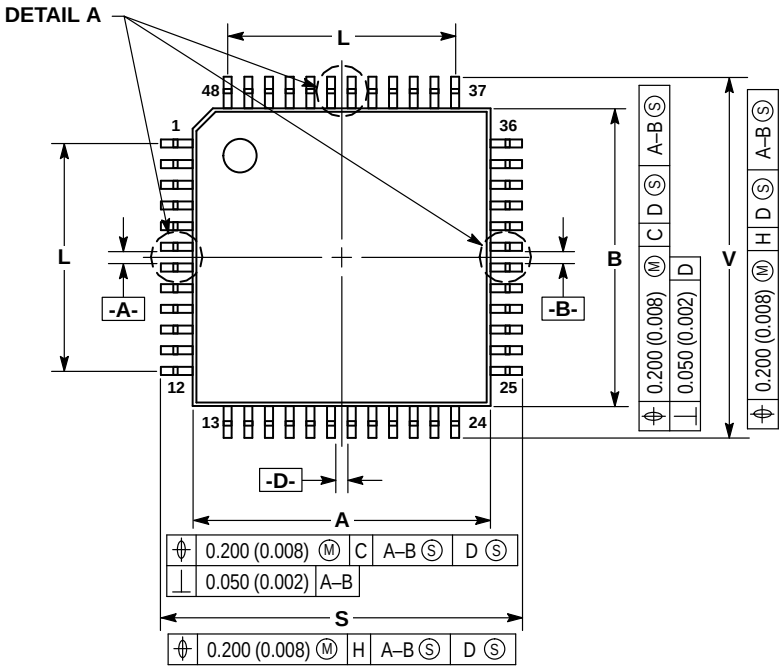
DETAIL A

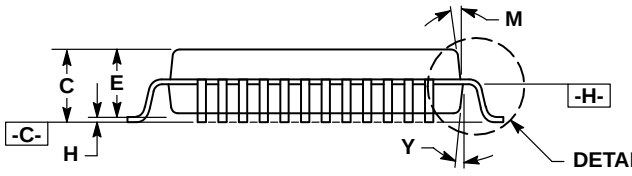


DETAIL B



SECTION B–B
ROTATED 90°





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.48 (0.019).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.90	12.10	0.469	0.476
B	11.90	12.10	0.469	0.476
C	2.05	2.55	0.026	0.041
D	0.20	0.40	0.081	0.100
E	2.00	2.30	0.079	0.091
G	0.80 BASIC		0.031 BASIC	
H	0.00	0.30	0.000	0.011
J	0.10	0.20	0.005	0.008
K	0.65	1.05	0.026	0.041
L	8.80 BASIC		0.346 BASIC	
M	13° REF		13° REF	
P	0.40 BASIC		0.016 BASIC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.006	0.011
S	14.90	15.70	0.587	0.618
V	14.90	15.70	0.587	0.618
W	0.65 REF		0.026 REF	
X	1.60 REF		0.063 REF	
Y	5° REF		5° REF	

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://www.mot.com/SPS/

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298