MC141622EVK

ACF-II Evaluation Board Operating Manual

1. SUMMARY

The MC141622EVK is a development board for evaluation of the MC141622. In addition to the MC141622, the MC141622EVK contains all the analog circuit that is necessary for buffering both the input and output video signal and generation of the 4xfsc clock. By connecting an external signal source, monitor, and power supply, it is possible to evaluate all the operating modes on the MC141622.

2. SPECIFICATION

Board Dimensions	100 mm (Length) x 150 mm (Width)
Y/C Separation LSI	MC141622FU Mount
Video Input Amplifier	MC14577 2SC2002 Use
Video Output Amplifier	MC14576 Use
Clamp Circuit	2SC2002 2SA953 Use
Clock Generator	MC1378P Use
Clock Buffer Amplifier	MC14576 Use
Analog Input/Output Interface	BNC Connector x3, S Terminal Output Mount
Digital Input/Output Interface	16 Pin Header Mount
Action Mode	MC141622 Supports All Operating Modes
Regulator	MC7805CT Use
Recommended Supply Voltage	+ 10 V
Operating Temperature	0 to 50°C
Supply Current	350 mA

REV 3
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3. BOARD OPERATION

3.1 ACF–II Operating Mode

AFC–II has four operating modes. Any one of these modes can be selected using the digital code input to MODE 0 and MODE 1 using ROTARY SW. The function of each mode is as follows.

(1) Normal fsc Mode

This is the mode for usual Y/C separation. It separates Y/C from the video signal that is input to the A/D converter.

The coring parameter of the vertical enhancer can be set up by the digital code that is input to C0 – C3 (block level parameter), C4 – C7 (white level parameter), and D4 – D7 (noise slice level parameter).

The clock is a 3.579545 MHz subcarrier input to the CLK connector; the built–in 4x PLL generates 4xfsc clock.

(2) Normal 4xfsc Mode

This mode is used for Y/C separation. It separates Y/C from the video signal that is input to the A/D converter.

The coring parameter of the vertical enhancer can be set up by the digital code that is input to C0 – C3 (block level parameter), C4 – C7 (white level parameter), and D4 – D7 (noise slice level parameter).

The clock is 14.31818 MHz which is a 4x subcarrier input to the CLK connector.

(3) Digital Input Comb Filter Mode

This mode uses the A/D converter, filter, and D/A converter as two independent blocks. The digital data converted by the A/D converter is output on C0 – C7. Data input on D0 – D7 is processed by the ACF–II. Filtering is performed by the algorithm of ACF–II and the Y/C video is output as analog signals from Y_{out} and C_{out}. These two blocks can operate with input clock signals that have different frequencies or phases and can be operated independently by using the CLK(AD) for the A/D converter, and the CLK input for the D/A converter.

The clock is 14.31818 MHz which is a 4x subcarrier input to the CLK connector and the CLK(AD) connector.

(4) Digital Output Comb Filter Mode

In addition to the normal Y/C analog outputs, the MC141622EVK can provide the Y/C signals as digital luminance and chrominance signals. The digital luminance data is output on C0 – C7 and the digital chrominance data is output on D0 – D7. This digital data can be modified by other digital processing.

The following table is the assignment for the operating mode.

MODE Switching Function

Mode	MODE1	MODE0	Rotary SW
Normal fsc Mode	L	L	0
Normal 4xfsc Mode	L	H	1
Digital Input Comb Filtering Mode	H	L	2
Digital Output Comb Filtering Mode	H	H	3

4. BK FUNCTION

By setting the BK pin (toggle SW1) to the H level, composite video is output on the Y_{out} pin and the chrominance signal on the C_{out} pin.

The following table is the function of the BK pin.

BK Function

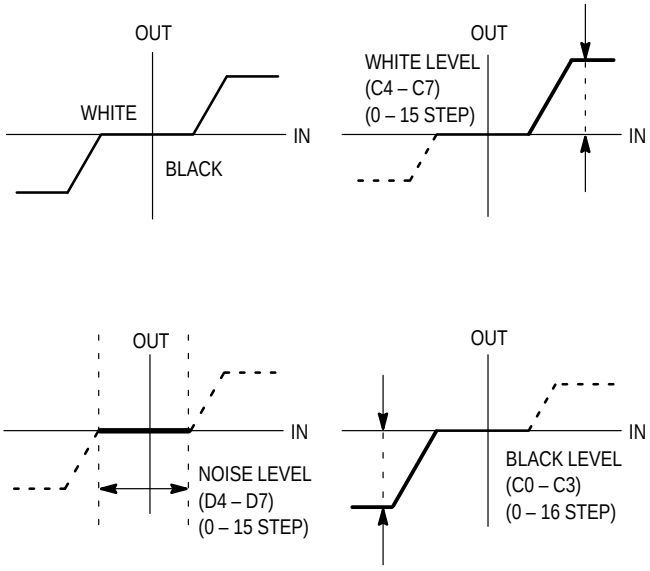
BK Pin	Y_{out} Pin	C_{out} Pin
L	Luminance	Chrominance
H	Composite	Chrominance

4.1 Vertical Enhancer Function

By setting the VH pin (toggle SW2) to the L level, the vertical enhancer feature is enabled. The coring parameter of the vertical enhancer can be set up every 1 LSB by the digital code that are input to C0 – C3 (black level parameter), C4 – C7 (white level parameter), and D4 – D7 (noise slice level parameter.

The set up level of the coring parameter and characteristics are as follows.

Coring Characteristics



Vertical Enhancer Function

VH Pin	Vertical Enhancer
L	On
H	Off

Coring Parameter Set Up

C7	C6	C5	C4	Level
C3	C2	C1	C0	
D7	D6	D5	D4	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	A
H	L	H	H	B
H	H	L	L	C
H	H	L	H	D
H	H	H	L	E
H	H	H	H	F

4.2 Clock Generator Compounding

The clock generator (MC1378P) provides the necessary reference oscillator and phase locks the clock to the color subcarrier by inputting the composite video signal.

VC1 adjusts the horizontal VCO to synchronize the output of the burst gate (pin 5 on the MC1378P) with the input video signal. VC2 adjusts the chroma VCO for maximum amplitude output from the clock buffer (pin 1 on the MC14576).

VR3 adjusts pull–in of the chroma PLL filter. This is usually fixed to the center position. VR4 selects the dc bias for the clock buffer output and is usually 2.25 V.

4.3 Video Amplifier Adjustment

On the video amplifier (MC14577), the gain is adjusted by VR1. This sets the input range (3.0 Vp–p) of the A/D converter in MC141622FU.

VR2 is the clamp level adjustment. This adjusts the sync tip clamping of the input video signal to the video amplifier.

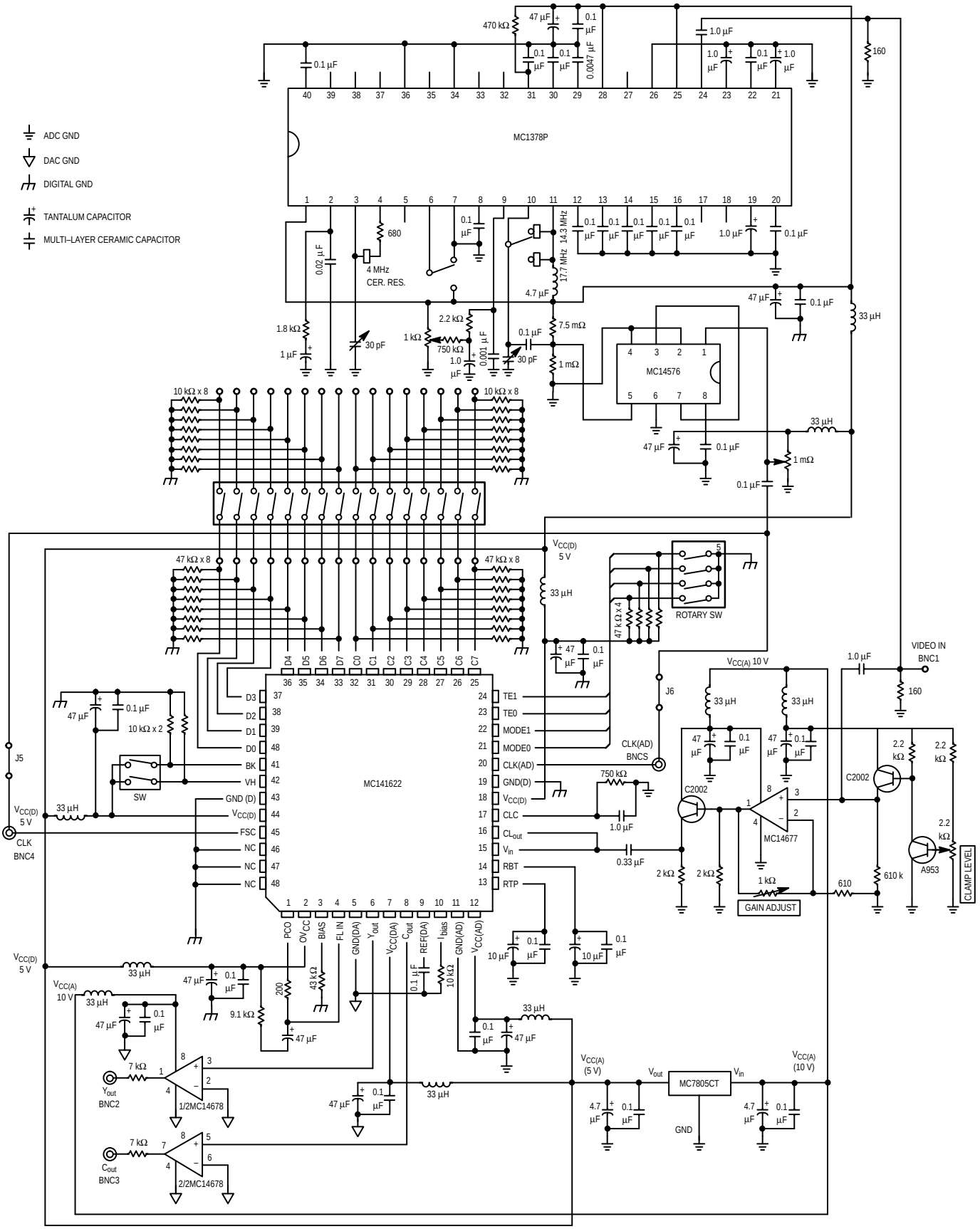
4.4 Outside Interface

The outside interface should provide a composite video input signal to BNC1. The MC141622EVK provides Y/C separation and outputs the luminance from BNC2 and the color signal from BNC3. There is an S output connector on this board for easy connection to instruments having an S input connector.

BNC4 and BNC5 are for the external input of each CLK and CLK(AD). However, when using these, it is necessary to modify the board pattern; i.e., cut (J5, J6).

There is no filter for bandwidth limitations on this board beyond that imposed by the bandwidth limitations of the MC14577 buffer amplifier. To minimize noise resulting from excessive bandwidth, the bandwidth of input video signal should be limited to no more than one half of the clock frequency.

5. MC141622EVK CIRCUIT

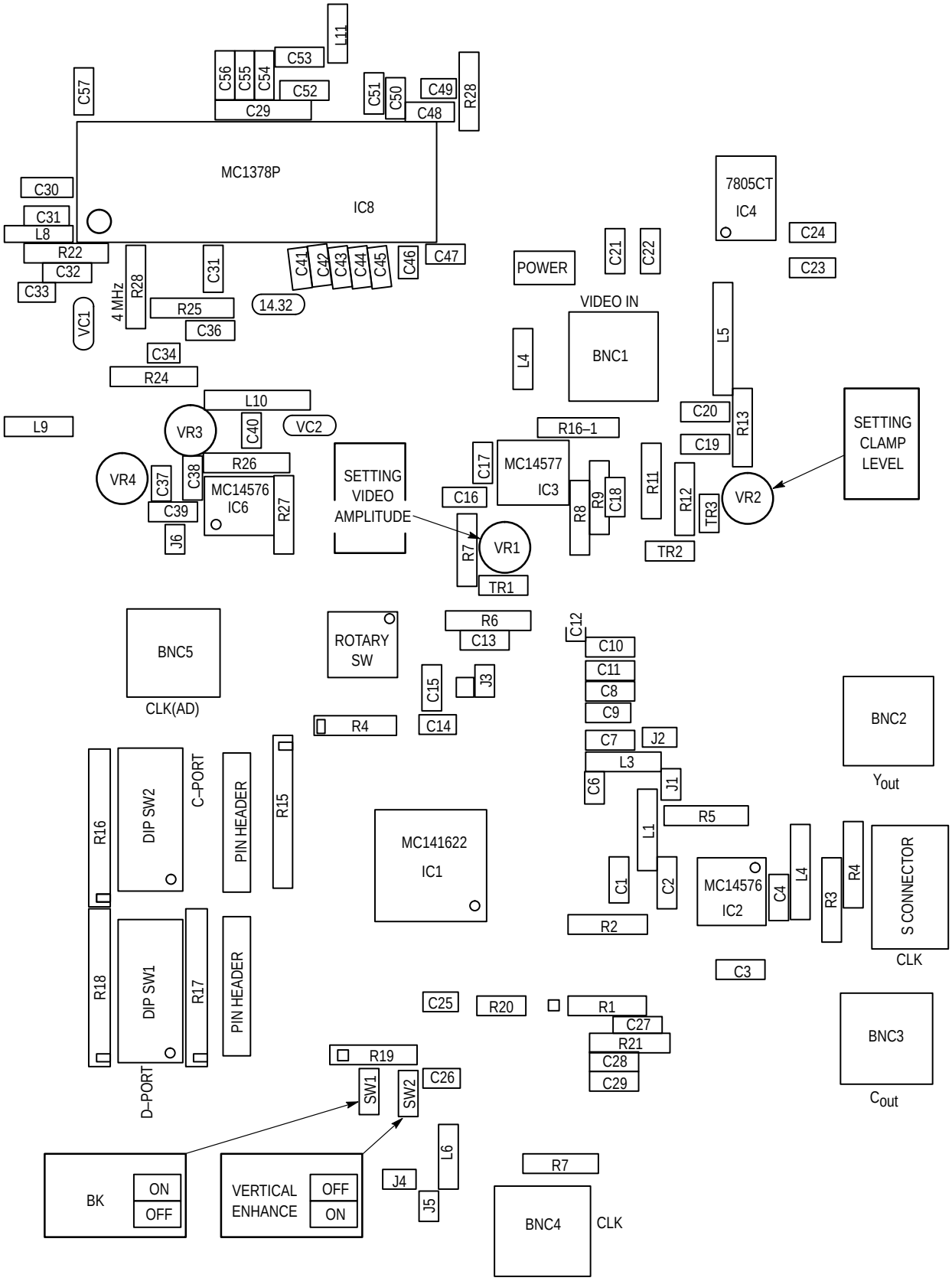


6. MC141622EVK PARTS LIST

Reference Designation	Description
IC1	MC141622FU
IC2	MC14576CP
IC3	MC14577CP
IC4	MC7805CT
IC5	MC14576CP
IC6	MC1378P
TR1	2SC2002
TR2	2SC2002
TR3	2SA953
R1	9.1 kΩ
R2	62 kΩ
R3, R4	75 Ω
R5	3.6 kΩ
R6	750 kΩ
R7, R8	2.0 kΩ
R9	510 Ω
R10	150 Ω
R11	510 kΩ
R12, R13	2.2 kΩ
R14	47 kΩ x 4
R15	47 kΩ x 8
R16	10 kΩ x 8
R17	47 kΩ x 8
R18	10 kΩ x 8
R19, R20	10 kΩ x 4
R21	200 Ω
R22	1.8 kΩ
R23	680 Ω
R24	750 kΩ
R25	2.2 kΩ
R26	7.5 mΩ
R27	1.0 mΩ
R28	150 Ω
R29	470 kΩ
L1 – L9	33 µH
L10	4.7 µH
L11	33 µH
VR1	1 kΩ
VR2	2.2 kΩ
VR3	1 kΩ
VR4	1 mΩ
VC1, VC2	30 pF
SW1, SW2	Toggle Switch
DIP SW1, DIP SW2	8 Channel Dip Switch
ROTARY SW	16 Channel Switch
	4 MHz Cer. Res
	14.32 MHz Crystal

Reference Designation	Description
C1	0.1 µF
C2, C3	47 µF
C4, C5, C6	0.1 µF
C7	47 µF
C8	0.1 µF
C9	10 µF
C10	0.1 µF
C11	10 µF
C12	0.33 µF
C13	1.0 µF
C14, C15	0.1 µF
C16	47 µF
C17	0.1 µF
C18	1.0 µF
C19	47 µF
C20, C21	0.1 µF
C22	47 µF
C23	0.1 µF
C24	47 µF
C25	0.1 µF
C26	47 µF
C27	10 µF
C28	0.1 µF
C29, C30	47 µF
C31	0.1 µF
C32	0.022 µF
C33, C34	1.0 µF
C35	0.1 µF
C36	0.001 µF
C37	47 µF
C38 – C45	0.1 µF
C46	1.0 µF
C47, C48	0.1 µF
C49 – C51	1.0 µF
C52	0.1 µF
C53	47 µF
C54	0.047 µF
C55 – C57	0.1 µF

7. MC141622EVK LAYOUT



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