



MOTOROLA

SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

Order this data sheet by MC1384/D

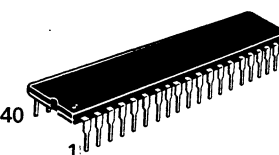
MC1384

Product Preview

MULTIMODE MONITOR HORIZONTAL, VERTICAL, AND VIDEO COMBINATION PROCESSOR

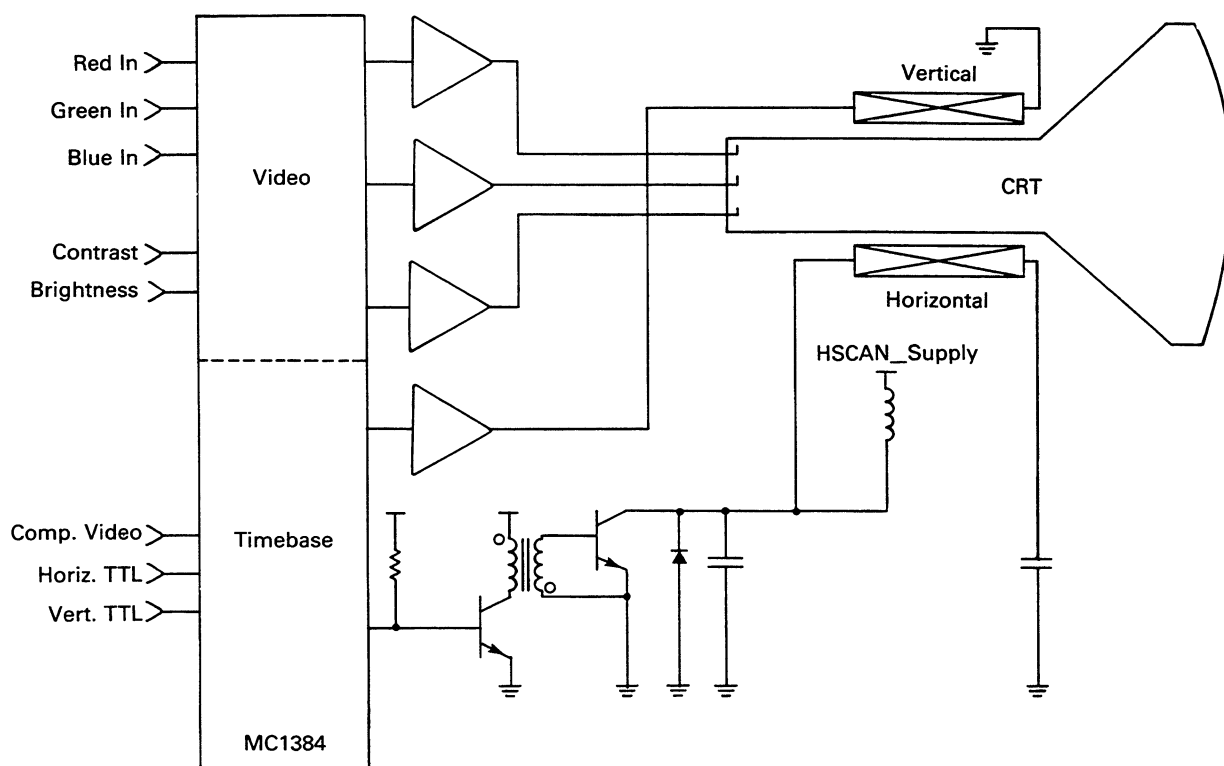
The MC1384 includes all the signal processing functions for a resistor programmable fixed frequency and multiple sync source RGB monitor and includes the following functions:

- Automatic horizontal frequency tracking of all commonly used personal computer and broadcast standards, resistor programmable from 15.5 to 40 kHz.
- The vertical timebase operates from 45 to 80 Hz.
- The 50 MHz video system includes contrast and brightness controls with automatic beam limiter. The video drivers can be used as the lower device in a cascode output stage.



P SUFFIX
PLASTIC PACKAGE
CASE 711-03

APPLICATION BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Pin	Value	Unit
Supply Voltage	20,31	10	V
Operating Temperature Range		- 10 to + 60	°C
Storage Temperature Range		- 65 to + 150	°C
Junction Temperature		+ 150	°C

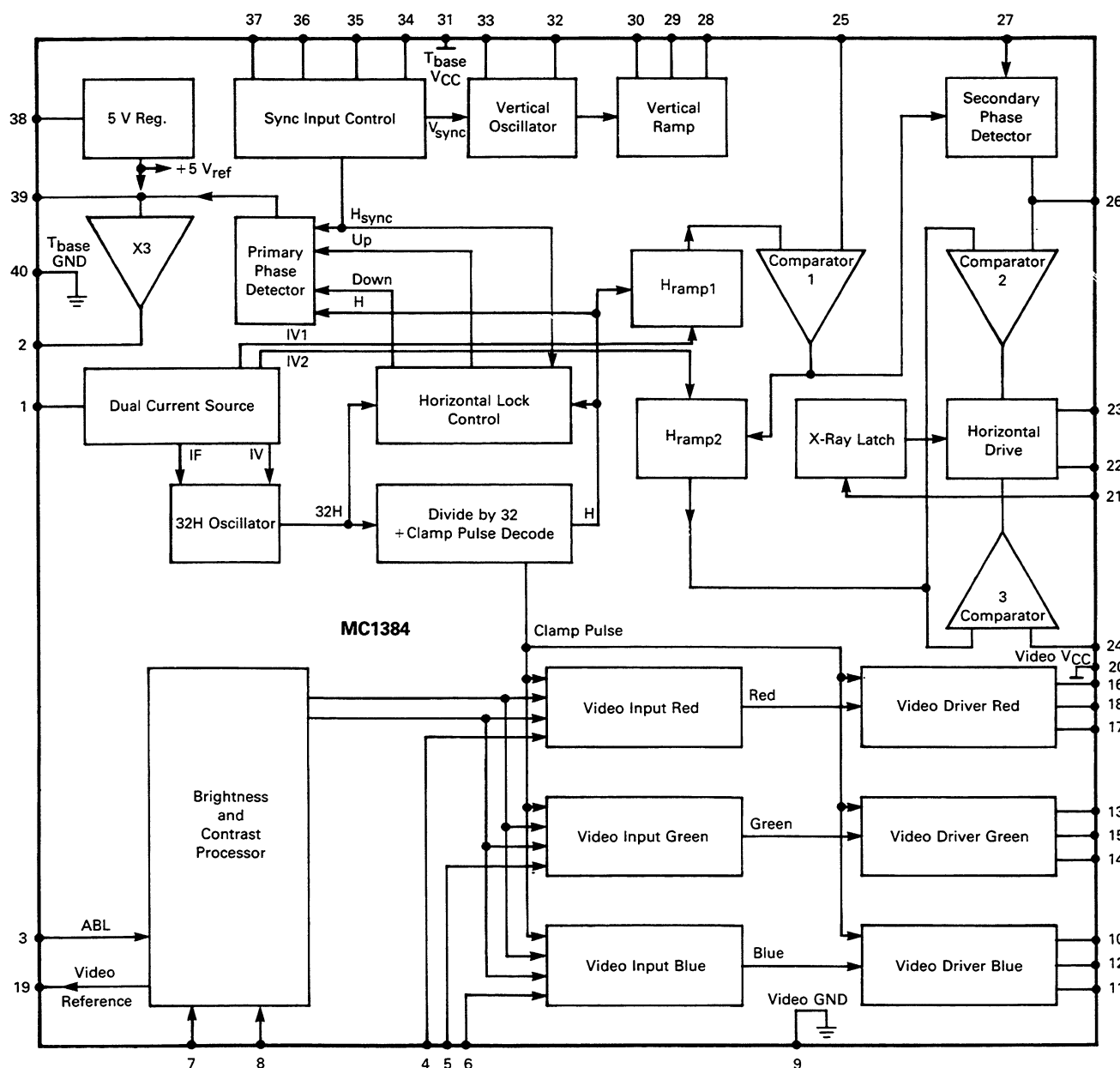
NORMAL OPERATION ($T_A = 25^\circ\text{C}$, $V_{CC} = 8.0\text{ V}$, using application circuit)

Characteristic	Condition	Min	Typ	Max	Unit
Supply Voltage Pins 31, 20		7.6	8.0	8.4	Volts
Supply Current Pins 31, 20	Excluding current at Pins 12, 15, 18	—	40	—	mA
Internal Regulator Pin 38		0.57	0.625	0.68	XV_{CC}
Horizontal Frequency Range	(With components shown, FH = 31.5 kHz)	15.5	—	40	kHz
Horizontal Pull-In Range		—	± 5.0	—	%FH
Horizontal Picture Position Adjustment Range	$V_{25} = 0-8.0\text{ V}$	- 20	—	+ 20	%TH
Horizontal Output Duty Cycle Adjustment	$V_{24} = 0-8.0\text{ V}$	2:1	—	1:2	
X-Ray Horizontal Shutdown Threshold		0.4	0.6	0.9	V
Vertical and Horizontal TTL Input Threshold		1.5	2.0	2.5	V
Comp. Video Sync. Sep. Input Level	Blanking to sync tip	0.1	—	2.0	V
Comp. Video Sync. Sep. Drive Impedance		—	—	1.0 k	Ohms
Horizontal Oscillator Free Run Temperature Drift	Pin 2 open circuit	—	—	300	ppm/°C
Source Current for 15.5 kHz FH	I_{source} Pin 1	—	120	—	μA
Source Current for 40 kHz FH	I_{source} Pin 1	—	320	—	μA
Horizontal Drive Output Current	V_{23} low	—	—	40	mA
Horizontal Drive Output Voltage	$I_{23} = 40\text{ mA}$	—	—	0.3	V
Vertical Synchronization Range	$FV_{\text{nom}} = 60\text{ Hz}$	—	12	—	Hz
Vertical Ramp Amplitude		—	—	3.0	Vp-p
Vertical Ramp Output Current		—	—	2.0	mA _{p-p}
Vertical Ramp Nonlinearity		—	—	1.0	%
Vertical Ramp Frequency Range		45	—	80	Hz
Vertical Free Run Temperature Drift	$FV = 60\text{ Hz}$	—	0.01	—	Hz/°C
Vertical Free Run Drift with V_{CC}	$FV = 60\text{ Hz}$	—	0.5	—	Hz/V
Video Source Impedance Pins 4, 5, 6		—	—	100	Ohms
Video Input Level Pins 4, 5, 6		0.5	0.7	1.2	Vp-p
Video Output Current Pins 12, 15, 18	Peak white with nominal black level	—	—	60	mA



NORMAL OPERATION — continued ($T_A = 25^\circ\text{C}$, $V_{CC} = 8.0\text{ V}$, using application circuit)

Characteristic	Condition	Min	Typ	Max	Unit
Video Bandwidth -3.0 dB Pins 4-17, 5-14, 6-11	$A_V = 4.5$	50	—	—	MHz
Brightness Control Range	$V_8 = 0-5.0\text{ V}$ (Measured at Pins 11, 14, 17)	—	± 0.5	—	V
Contrast Control Range	$V_7 = 0-5.0\text{ V}$	—	26	—	dB
Nominal Video Voltage Gain Pins 4-17, 5-14, 6-11	$V_7 = 5.0\text{ V}$	—	4.5	—	
Video Clamp Reference Voltage Pin 19		—	2.5	—	V
Video Output Clamp Voltage	$V_8 = 2.5\text{ V}$	—	2.5	—	V

INTERNAL BLOCK DIAGRAM

SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

5.0 Volt Regulator — The regulator reference is derived from the V_{CC} . This is buffered and used as an internal voltage source for many functions within the device.

Sync Input Control — In this block the polarity of the TTL sync inputs is monitored and corrected automatically. In the absence of horizontal or composite TTL sync the default input becomes the composite sync separator. The integrator that forms part of the vertical polarity correction has an external capacitor, the voltage at which can be used to determine the polarity of the vertical TTL sync and therefore the mode of certain PC graphics standards. The MC1382 uses this pin for mode control.

Vertical Oscillator — This oscillator is injection-locked by the signal from the sync input control and provides a drive for the vertical ramp generator.

Vertical Ramp Generator — An adjustable linearity and amplitude vertical rate ramp is generated-locked to the vertical oscillator.

32H Oscillator — A current controlled oscillator running at 32 times horizontal rate is locked to the external horizontal sync using a PLL.

Divide by 32 and Clamp Pulse Decoder — The 32H oscillator frequency is divided down to H frequency and a pulse decoded for back porch clamping of the video.

Dual Current Source, I_{fix} I_{var} — The fixed and variable current sources control the 32H oscillator as part of the phase-locked loop. The variable source is used elsewhere in the device for various horizontal frequency dependent functions.

Primary Phase Detector and Unity Gain Buffer — The H_{sync} and H signals are phase compared and used to drive a unity gain buffer the output of which is used to control I_{var} , thus completing the PLL.

Horizontal Lock Control — This block provides frequency agility to the horizontal PLL.

H_{ramp1} and Comparator 1 — The picture position is controlled by slicing the output of H_{ramp1} .

H_{ramp2} , Comparator 2 and Comparator 3 — These blocks control the duty cycle and position of the horizontal drive pulse.

Secondary Phase Detector — Horizontal flyback is compared with Comparator 2 output to provide automatic compensation for horizontal output stage turn-off delay.

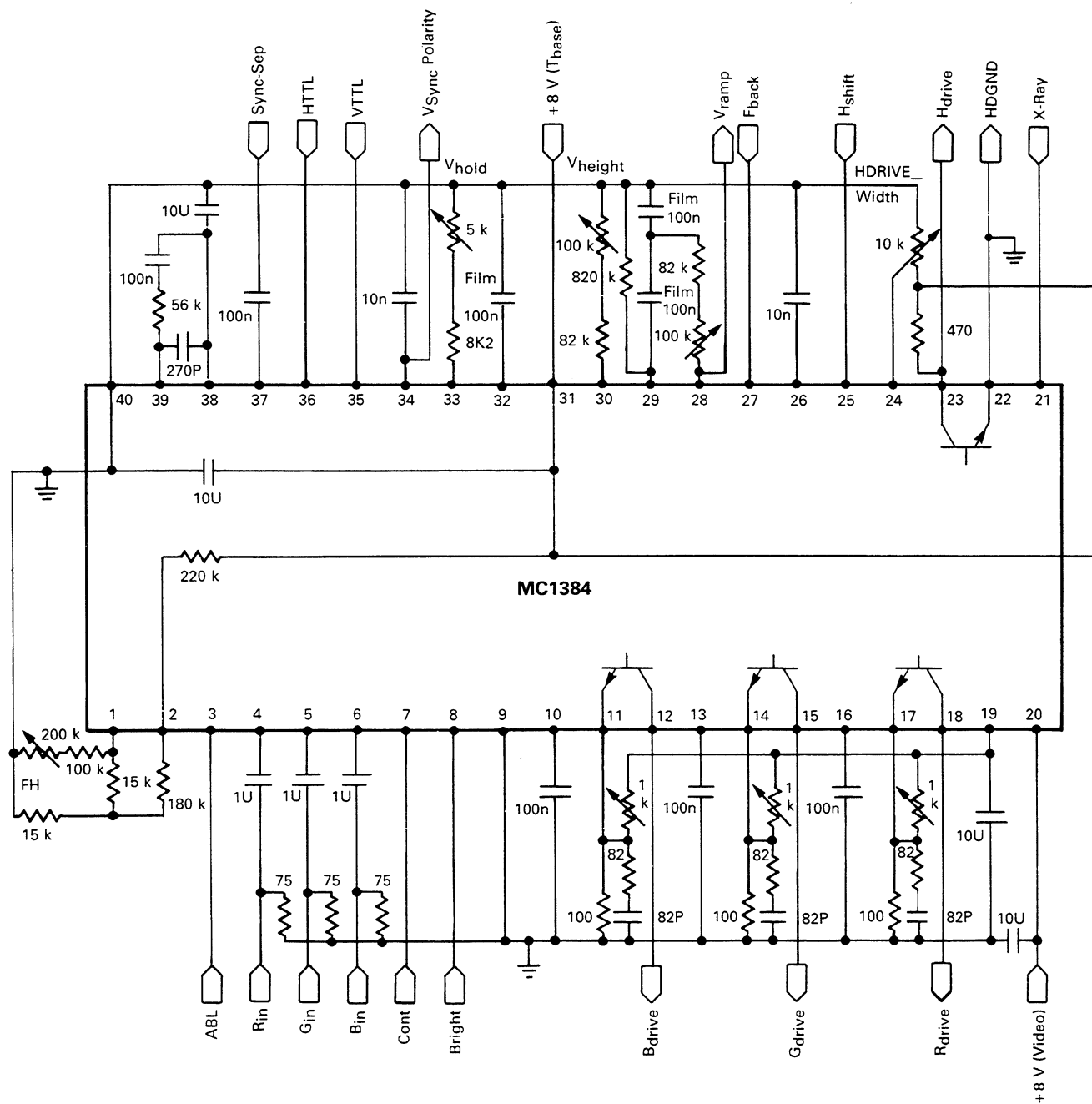
X-Ray Latch and Horizontal Drive — If the threshold of the latch is exceeded the horizontal drive is permanently on until the V_{CC} is removed.

Brightness and Contrast Processor — The dc video controls are distributed to the video stages and a clamp reference voltage is developed for the output stages.

Video Input and Video Drivers — The video signals are processed clamped and amplified to provide either an emitter follower or lower stage of a cascode amplifier to drive the high voltage output stage.

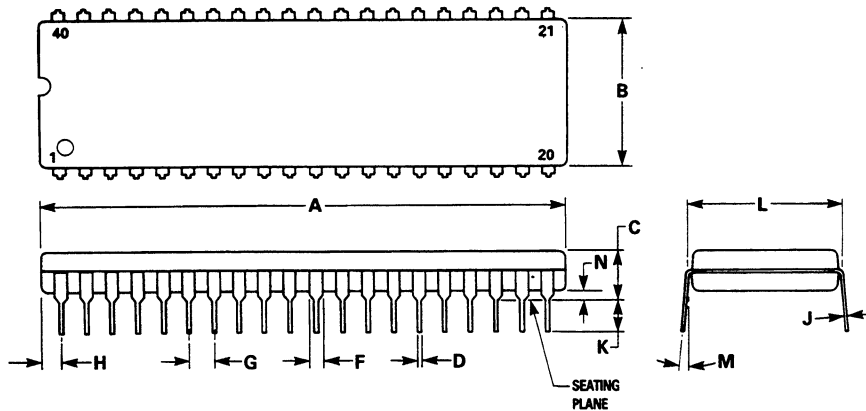


APPLICATION CIRCUIT DIAGRAM



OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 711-03




NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040



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