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MOTOROLA

MC13173

Infrared Integrated Transceiver IC

The MC13173 is a low power infrared integrated system (IRIS). It is a unique blend of a split IF wideband FM receiver and a specialized infrared LED transmitter. This device was designed to provide communications between portable computers via a half duplex infrared link at data rates up to 200 kbps.

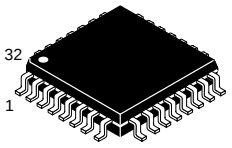
The receiver includes a mixer, IF amplifier and limiter and data slicer. The IF amplifier is split to accommodate two low cost cascaded filters. The RSSI output is derived by summing the output of both IF sections.

The transmitter section includes a frequency synthesizer, FSK modulator, harmonic low pass filter and an IR LED driver.

- Transmitter Operates in Two Modes:
  - On/Off Pulsing for Remote Control
  - FSK Modulation at 1.4 MHz for Data Communications
- Over 70 dB of RSSI Range
- Split IF for Improved Filtering and Extended RSSI Range
- Digitally controlled Via a Six Line Interface Bus
- Individual Circuit Blocks Can Be Powered Down When Not In Use for Power Conservation

INFRARED TRANSCEIVER

SEMICONDUCTOR TECHNICAL DATA

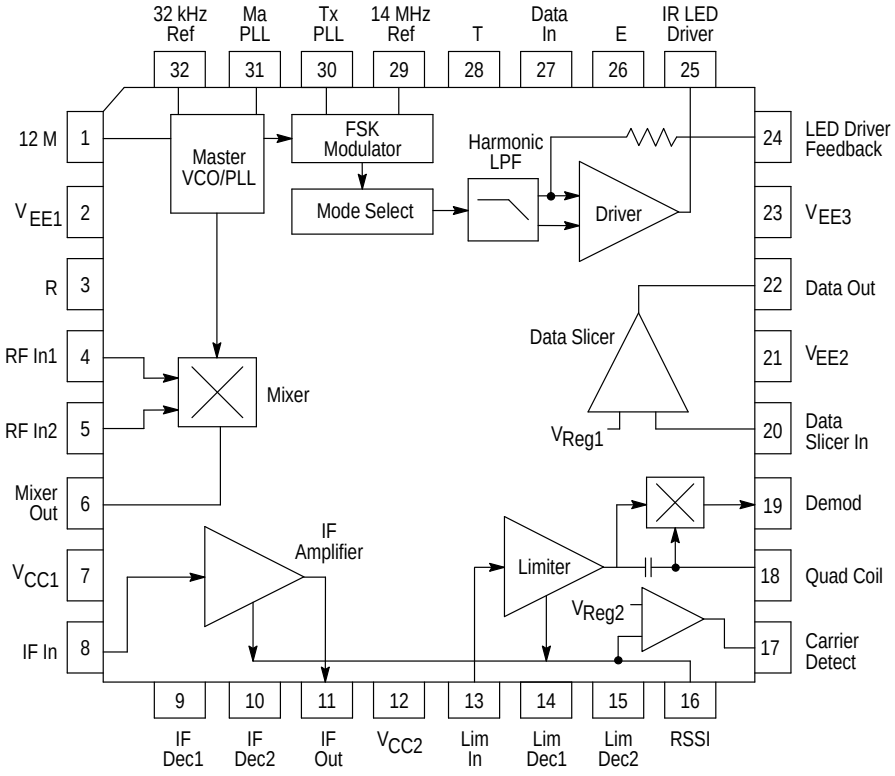


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13173FTB	T_A = – 40° to +85°C	TQFP–32

Simplified Block Diagram



This device contains 914 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC} - V_{EE}$	6.0	Vdc
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	$V_{CC} - V_{EE}$	2.7 to 5.5	Vdc
Ambient Temperature Range	T_A	– 40 to +85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Control Pin Logic State T	R	E	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (See Table 2)				7, 12	I_{CC}				
Receive Mode	0	1	0			–	6.5	9.0	mA
Communications Mode	1	0	0			–	4.75	8.0	
A/V Mode	1	0	1			–	1.5	–	
Standby Mode	0	0	0			–	<10	–	nA
Master PLL Charge Current				31	I_{MA}	–	±25	–	µA
DATA SLICER									
Data Slicer Threshold Voltage				20	V_{TH1}	0.85	1.1	1.4	Vdc
Maximum Pull–Down Current				22	I_{DS}	1.0	1.8	–	mA
CARRIER DETECT									
Carrier Detect Threshold Voltage				16	V_{TH2}	1.0	1.15	1.3	Vdc
Maximum Pull–Down Current				17	I_{CD}	1.1	3.0	–	mA
TRANSMITTER									
Maximum Pull–Up Current				25	I_{OH}	5.8	7.0	–	mA
Maximum Pull–Down Current				25	I_{OL}	–	150	700	µA
DC Output Voltage				24	V_O	–	200	–	mV
Transmit PLL Charge Current				30	I_{TX}	–	±25	–	µA

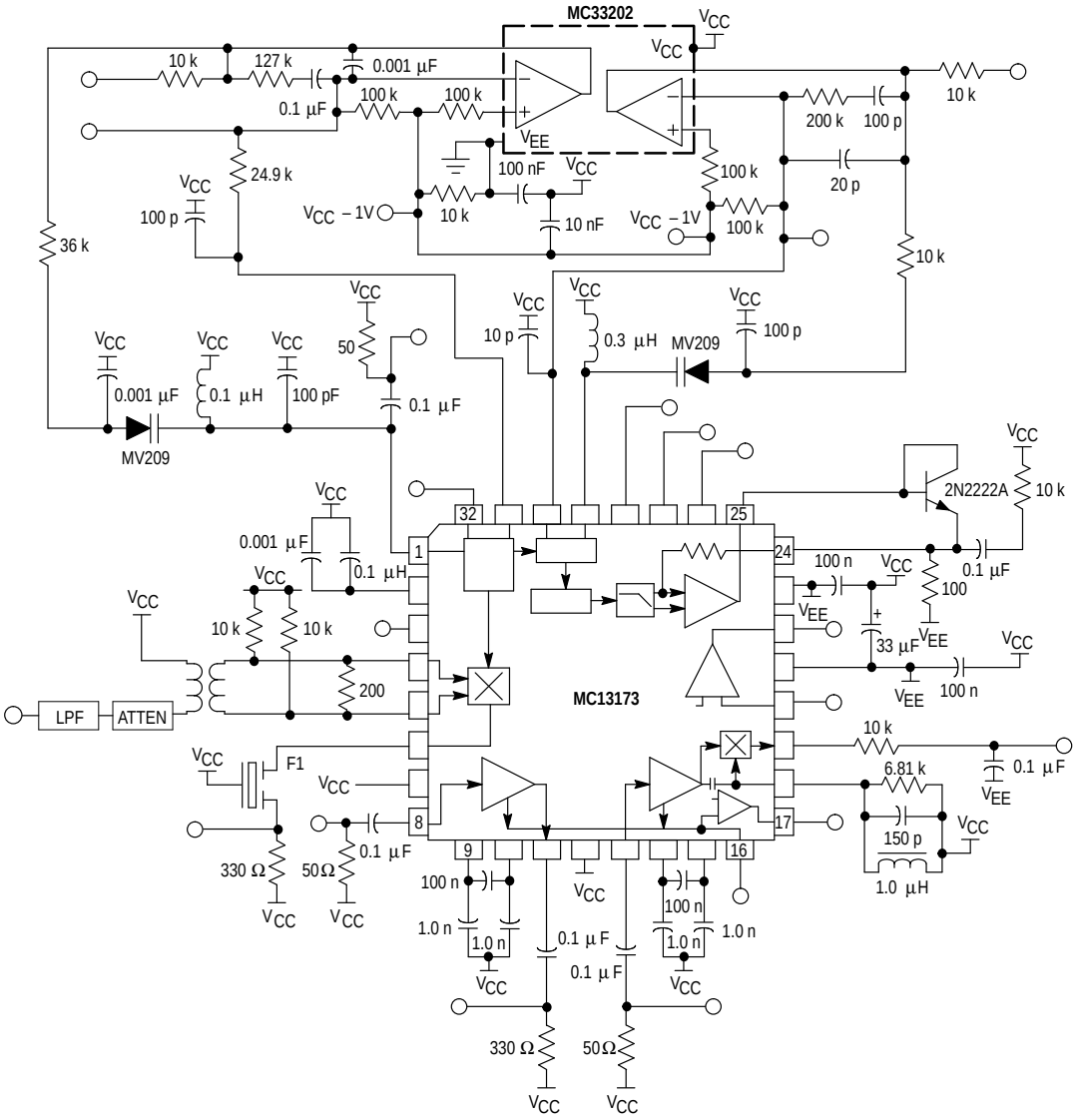
AC ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
TRANSMITTER						
Upper Sideband Frequency (Mark)	24	f_{HI}	–	1.427	–	MHz
Lower Sideband Frequency (Space)	24	f_{LO}	–	1.317	–	MHz
Upper and Lower Sideband Amplitude	24	V_{SB}	40	54	70	mVrms
RECEIVER						
Receiver Sensitivity – 12 dB SINAD	4, 19	V_{SIN}	–	5.0	–	µV
MIXER						
Mixer Conversion Gain	4, 5, 6	$AV_{(Mix)}$	–	23.5	–	dB
Mixer Output Impedance	6	Z_O	–	330	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER						
IF Amplifier Gain	8, 11	–	–	54	–	dB
IF Amplifier RSSI Slope	16	–	–	275	–	nA/dB
Input Impedance	8	Z_{IN}	–	330	–	Ω
Output Impedance	11	Z_O	–	330	–	Ω
RSSI Current Range	16	–	–	20	–	μA
RSSI Dynamic Range	16	–	–	70	–	dB
LIMITING AMPLIFIER						
Input Impedance	13	Z_{IN}	–	330	–	Ω
Limiter RSSI Slope	16	–	–	360	–	nA/dB
RSSI Current Range	16	–	–	20	–	μA
RSSI Dynamic Range	16	–	–	58	–	dB

Figure 1. Test Circuit



CIRCUIT DESCRIPTION

General

The MC13173 infrared transceiver integrates a split IF wideband FM receiver and an IR LED transmitter into a single IC. The transmitter is comprised of an FSK modulator, harmonic low pass filter, and IR LED driver. The receiver consists of a mixer, IF amplifier and limiting IF, detector, and data slicer. It includes RSSI and carrier detect functions.

The transmitter is capable of two modes of operation. It was primarily designed for use in the Communications Mode, which enables point–to–point data links, such as the communication from keyboard to computer, or for the exchange of data between portable computers. In this mode it is capable of 200 kbps half duplex FSK operation.

The transmitter can also operate in an “A/V” Mode, which pulses the LED on and off with no carrier. (See Figure 11).

Digital Interface Bus

The MC13173 is controlled via a six line 3.3 V digital interface bus. That includes three control pins, data in and out pins, and a carrier detect pin. Listed below is a brief description of each pin and its function.

Table 1. Digital Interface Pin Descriptions

Pin	Pin Name	Symbol	I/O	Description
28	Transmit Enable	T	I	High – Transmitter is enabled Low – Transmitter is disabled
27	Data In	DI	I	Data Input – 38.2 kbps Communication Mode
3	Receive Enable	R	I	High – Receiver is enabled Low – Receiver is disabled
22	Data Out	DO	O	Demodulated Output Signal
17	Carrier Detect	CD	O	High – Carrier is present Low – Carrier is not present
26	Transmit Modulation Enable	E	I	High – Transmitter is in A/V Mode Low – Transmitter is in Communications Mode

This transceiver was designed for use in battery powered, hand–held consumer products. To minimize power consumption, the digital interface enables individual system blocks to be powered down while not in use. The following diagram shows the mode of the IC and the power state of each circuit block for a given set of control levels.

Table 2. Power State Table

Control Pins*				Circuit Block Power States (See Figures 2 and 3)				Supply Current (Typical)
T	R	E	Mode	Master VCO	FSK Modulator	Receiver	LED Driver	
0	0	0	OFF	Off	Off	Off	Off	10 nA
0	0	1	OFF	Off	Off	Off	Off	70 μA
0	1	X	Receive	On	Off	On	Off	6.5 mA
1	1	1	Receive	On	Off	On	On	7.5 mA
1	1	0	Transmit – Comm Mode	On	On	On	On	9.0 mA
1	0	0	Transmit – Comm Mode	On	On	Off	On	4.75 mA
1	0	1	Transmit – A/V Mode	Off	Off	Off	On	1.5 mA

* With Data In Pin Low

Master VCO/PLL

The master VCO provides the reference frequency for the FSK modulator and the LO frequency for the receiver downconverter. With a 32.768 kHz input frequency to the master VCO on Pin 1, the LO frequency for the receiver will be at 12.075 MHz. The reference frequency for the FSK modulator will be at approximately 1.1 MHz. The master VCO and FSK modulator are not used when the transmitter is used in A/V mode, and both are powered down.

Receiver Description

The single conversion receiver portion of the MC13173 is low power and wideband, and incorporates a split IF. This section includes a mixer, IF amplifier, limiting IF, quadrature detector and data slicer.

Mixer

The mixer is a double balanced four quadrant multiplier. It can be driven either differentially or single–ended by connecting the unused input to the positive supply rail.

The buffered output is internally loaded for an output impedance of 330 Ω for use with a standard ceramic filter.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB. The fixed internal input impedance is 330 Ω for use with a 10.7 MHz ceramic filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

Limiter

The limiter section is similar to the IF amplifier section, except that four stages are used with the last three contributing to the RSSI. This IF limiting amplifier section drives the quadrature detector internally.

RSSI/Carrier Detect

The received signal strength indicator (RSSI) outputs a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor sets the output voltage range.

The carrier detect threshold is set at approximately 1.2 Vdc. When the RSSI level exceeds that threshold, the carrier detect output will go high. A large resistor may be added externally between the comparator output and the positive input for hysteresis.

Quadrature Detector

The demodulator is a conventional quadrature type with an external LC tank driven through an internal 5 pF capacitor. The output is buffered to give an output impedance of less than 1.0 kΩ at an average DC level of around 1.1 V.

Data Slicer

The data slicer is designed to square up the data signal. It is self centering at about 1.1 V, and clips at about 0.75 V and 1.45 V. There is a short time constant for large peak–to–peak voltage swings or when there is a change in DC level at the detector output. The time constant is longer for small signals or for continuous bits of the same polarity which drift close to the threshold voltage.

Transmission Description

The MC13173 uses a dual modulus PLL to frequency shift key (FSK) modulate the baseband digital input signal, producing the necessary logic high and low frequencies for transmission. The transmit frequency for a logic high is 1.427 MHz, and the frequency for a low is 1.317 MHz with a 32.768 kHz reference frequency.

FSK Modulator

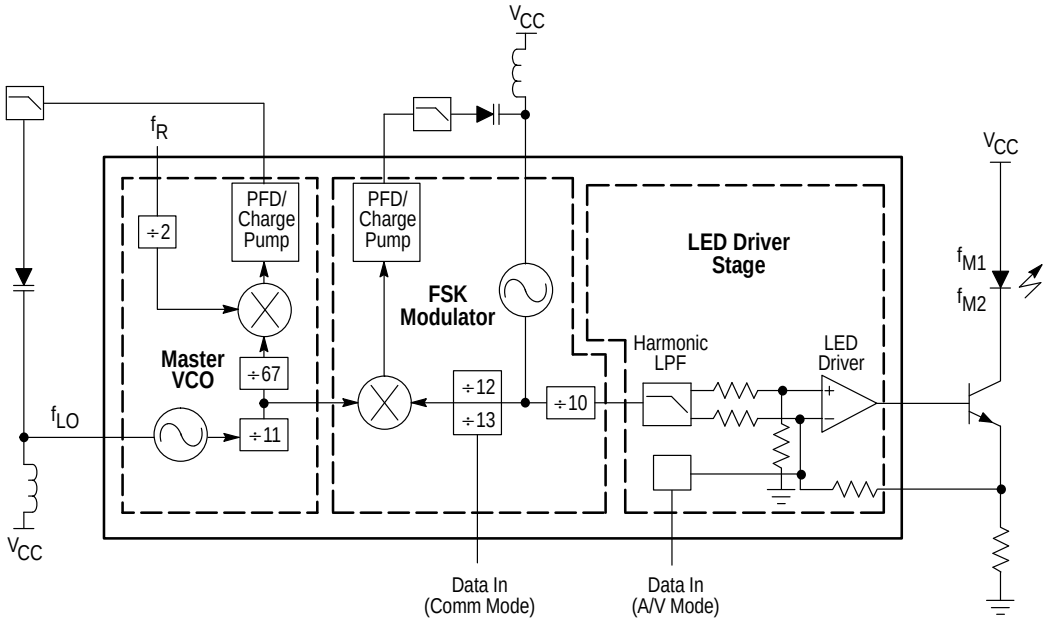
In the communications mode, the FSK modulator uses the reference frequency from the Master VCO to produce the two frequencies required for a logic high and a logic low. In the A/V mode, the FSK modulator is not used and is powered down.

LED Driver Stage

A low pass filter following the FSK modulator removes the undesired harmonic frequencies from the square–wave output of the divider circuits in PLLs. The resulting sinusoidal waveforms are fed into a unity gain difference amplifier, which drives the base of an external transistor, modulating the IR LED.

In A/V mode, the data is input directly into the inverting input of the op amp, and the low pass filter is not used.

Figure 2. Transmitter Block Diagram



f_R = 32.768 kHz

$f_{LO} = \frac{67 \times 11}{2} f_R$

Data High: $f_{M1} = \frac{13}{11 \times 10} f_{LO}$

Data Low: $f_{M2} = \frac{12}{11 \times 10} f_{LO}$

Figure 3. Receiver Block Diagram

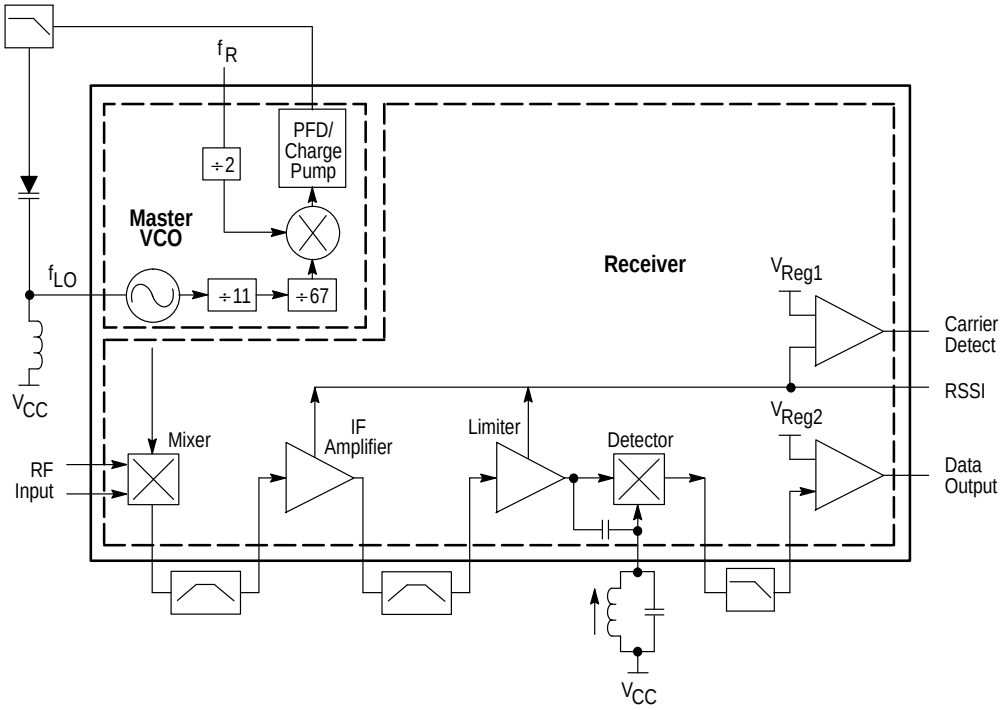


Table 3. PIN FUNCTION DESCRIPTION (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

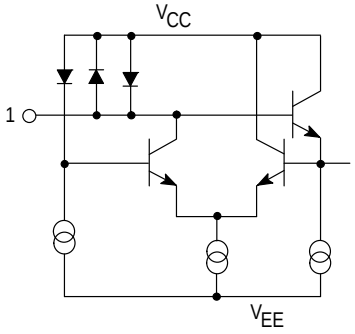
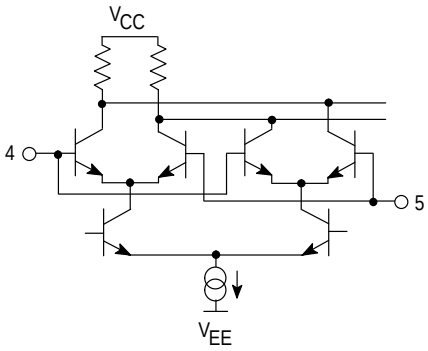
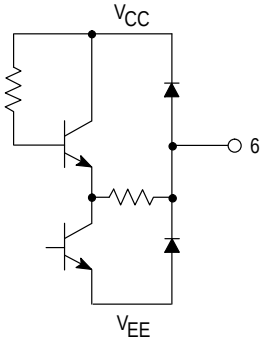
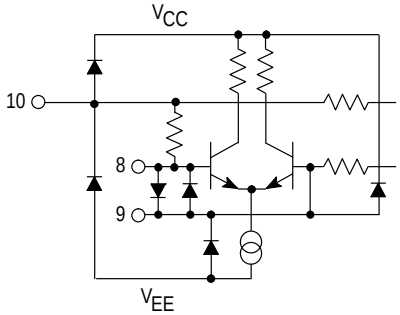
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
1	12 M	VCO for Master PLL. (Measured using a low capacitance FET probe. Standard oscilloscope probes can pull oscillator off frequency. See Figure 14.)		
2, 21, 23	V_{EE}	DC ground. Should be connected to a continuous ground plane on the PCB.		
3	R	Receive Enable Pin. See Tables 1 & 2.		
4, 5	RF In1 RF In2	RF Input to the mixer. 1.375 MHz average carrier frequency with ± 50 kHz deviation.		
6	Mixer Out	10.7 MHz IF Z_O = 330 Ω RF In = – 20 dBm Modulation = 32.768 kHz		
7, 12	V_{CC}	Supply voltage and RF ground, should be decoupled to V_{EE}.		
8	IF In	IF input impedance is 330 Ω. RF In = – 20 dBm Modulation = 32.768 kHz		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

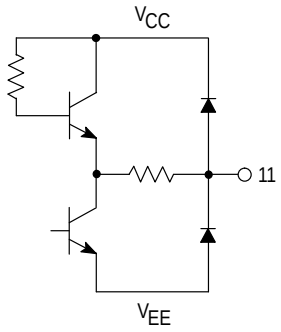
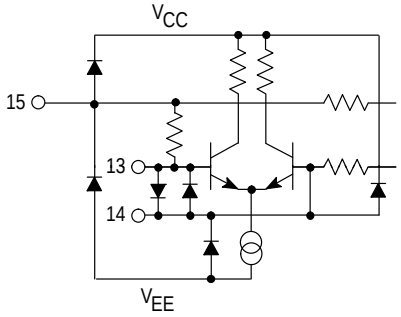
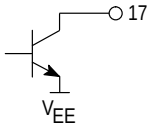
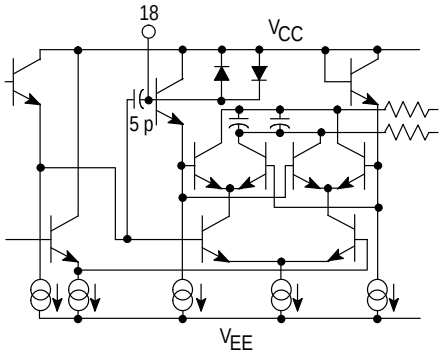
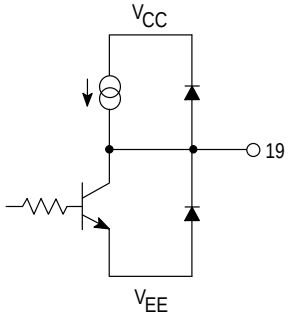
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
9, 10	IF Dec	IF decoupling as shown in Figure 15.	See Circuit for Pin 8.	
11	IF Out	IF Output. Z_O = 330 Ω. –20 dBm RF input level. Output is sinusoidal with lower drive levels.		
13	Lim In	Limiter input. Z_{In} = 330 Ω.		
14, 15	Lim Dec	External limiter decoupling as shown in application circuit.		
16	RSSI	Received Signal Strength Indicator Output. (See Figure 13)		
17	Carrier Detect	Logic output of the carrier detect comparator.		
18	Quad Coil	Quadrature tuning circuit. Modulated 10.7 MHz IF. Measured with a low capacitance FET probe.		
19	Demod	Demodulated signal output measured at the pin (before filtering). Modulation = 32.768 kHz sine wave.		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

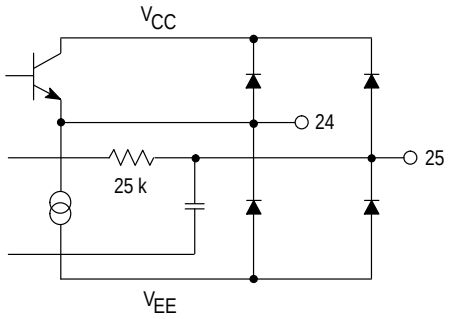
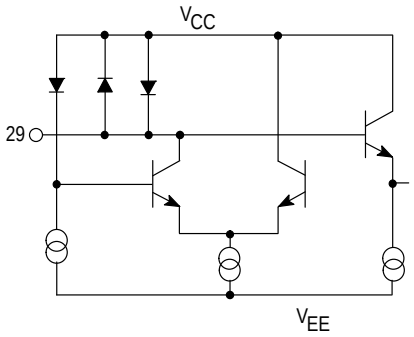
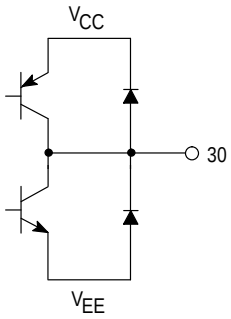
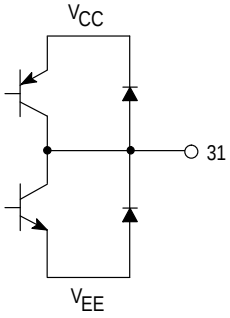
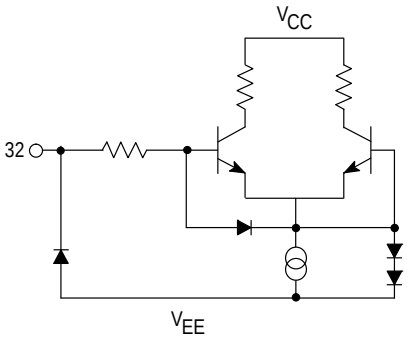
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
20	Data Slicer In	Input from the receiver demodulated output.		
22	Data Out	Output from the receiver data slicer. Modulation = 32.768 kHz sine wave. RF input driven by frequency generator. See also Figure 10.		
24	LED Driver Feed-back	Feedback for the LED driver op amp.		
25	IR LED Driver	Output of the unity gain output buffer in Communications Mode. See Figure 11 for transmit output in A/V mode. Modulation = 32.768 kHz square wave. .		
26	E	Transmit Modulation Enable. See Tables 1 & 2.		
27	Data In	Modulation input for transmit data.		
28	T	Transmit Enable pin. See Tables 1 & 2.		
29	14 MHz Ref	VCO for FSK Modulator phase locked loop. (Measured using a low capacitance FET probe. Standard oscilloscope probes can pull oscillator off frequency. See Figure 14.) No modulation (Data In low).		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
30	Tx PLL	Phase detector output for the FSK Modulator. (With loop closed and locked.) No modulation (Data In low).		
		With 32.768 kHz square wave modulation. Note: Probing the output of the phase detectors directly may disturb the loop. It is best to probe the output of the op amp when evaluating loop response.		
31	Ma PLL	Output of the phase detector charge pump for the Master PLL. (With loop closed and locked.)		
32	32 kHz Ref	Input to 32.768 kHz reference. Filtered from TTL oscillator using application circuit in Figure 15. Approximately 1.0 Vp–p triangle wave at 32.768 kHz.		

Typical Performance Over Temperature

(Measured using test circuit in Figure 1)

Figure 4. Normalized Mixer Gain versus Temperature

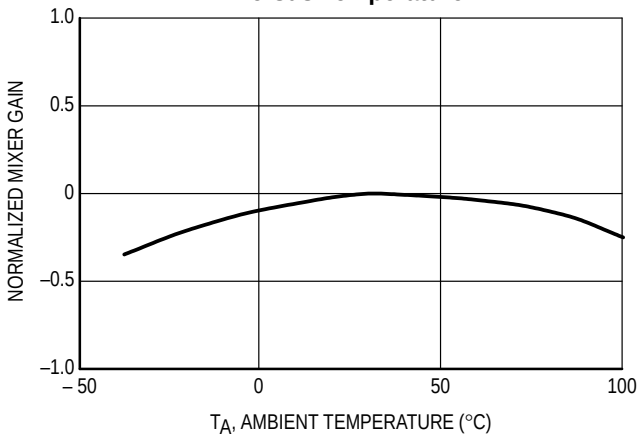


Figure 5. Normalized IF Amp Gain versus Temperature

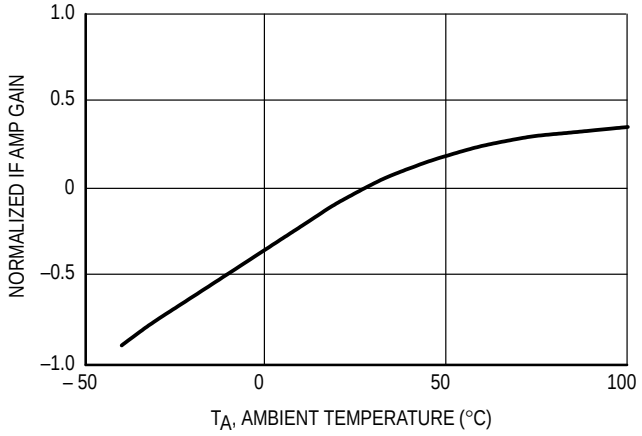


Figure 6. Maximum Pull–Up Current versus Temperature (Pin 25)

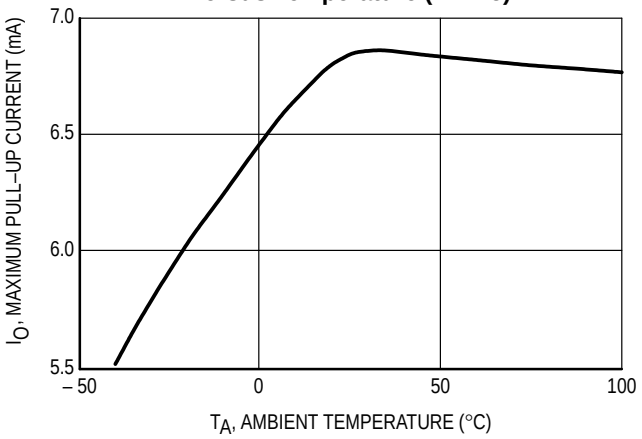


Figure 7. Maximum Pull–Down Current versus Temperature (Pin 25)

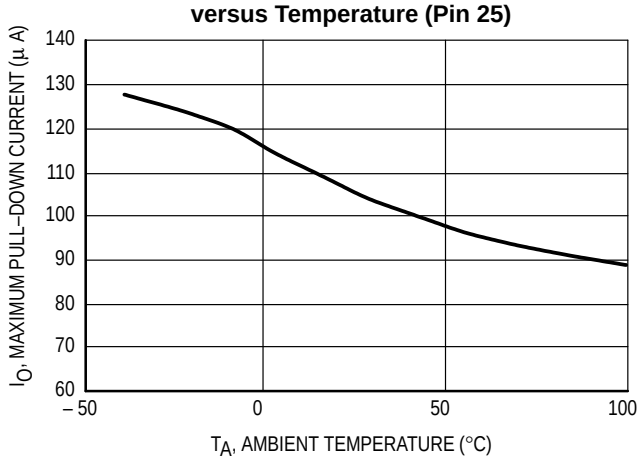


Figure 8. Supply Current versus Temperature

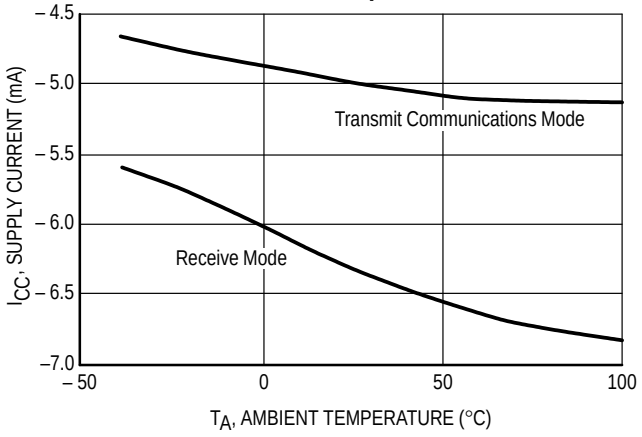
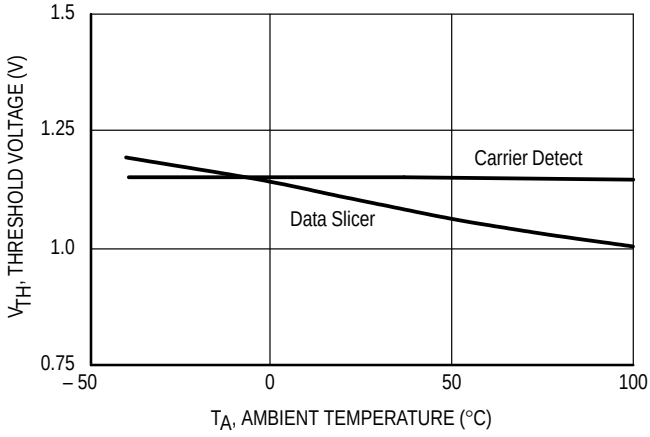


Figure 9. Data Slicer and Carrier Detect Threshold Voltages versus Temperature



APPLICATIONS INFORMATION

The MC13173 transceiver is specially designed to operate from a 32.768 kHz reference which is readily available in most computer applications. The frequency synthesizer on chip generates a receiver local oscillator frequency and the transmit mark and space frequencies from this fixed reference frequency, eliminating the need for additional crystals or manual tuning.

Large divide ratios are needed to generate these frequencies, however. For example, the receiver LO frequency is 368.5 times the 32.768 kHz reference frequency. This requires that the reference frequency be both accurate and stable. A two percent error in the reference frequency would pull the LO off frequency by over 240 kHz, putting the IF frequency out of the usable bandwidth of the filters and discriminator. For this reason, a 32.768 kHz oscillator circuit has been included on the demonstration board design. Although TTL crystal oscillators are available, this oscillator circuit uses an inexpensive tuning fork crystal and a hex inverter to generate a square wave reference frequency, which is then filtered and level adjusted to a 1.0 Vp–p triangle wave to drive pin 32. A TTL Clock Oscillator could also be used with the filter circuit as shown.

Frequency Synthesizer

The recommended op amp for the external loop filter is the MC33202. For low voltage operation, ($V_{CC} \leq 3.3$ V) an op amp that is rail–to–rail on both the input and output is advisable to obtain the widest possible output voltage range without distortion. Sufficient distortion from the op amp such as phase reversal on the output caused by overdriving the inputs could prevent the loop from locking to the reference.

In debugging the loop filter, it is important to note that the FSK Modulator phase locked loop will not lock until the Master VCO is locked to the reference. If the application circuit in Figure 15 is used, both loops should lock without the need for any additional tweaking. Since the VCO has ±2.0 MHz of range using the MV209 varactor diode (see Figure 11), neither precision components nor tuning should be required. To ensure both loops are operating properly, first evaluate each VCO with the loop open and a voltage equal to $V_{CC}/2$ applied to the resistor in series with the varactor. Since there is a relatively small capacitance (<40 pF) in series with the LC tank circuit, the VCO pin is sensitive to any parasitic capacitance. Thus when using a standard oscilloscope probe having 10 to 20 pF capacitance it is difficult to measure the VCO frequency without shifting its frequency. A low capacitance FET probe used with a frequency counter will enable you to accurately measure the VCO frequency without altering it in the process.

The free running frequency of the VCO should be approximately on frequency when the loop is open and the varactor is biased at mid–supply. The VCO for the Master PLL should run at 12.05 MHz. The free running frequency of the FSK Modulator should be at 13.72 MHz, midway between the two VCO frequencies needed to generate the transmit mark and space frequencies. The FSK Modulator loop is only active when the transmitter is enabled and the device is in the communications mode (see Tables 1 & 2). **If either the "T" pin is low or the "E" pin is high, the VCO will be off and you will see no oscillation on Pin 29.**

Once the loops are closed, the VCO frequencies should track the reference frequency within the hold–in range of the loop. Although the FSK Modulator loop is dependent on the Master VCO, the Master VCO is completely independent of the FSK Modulator. In fact, the FSK Modulator can be powered down (see Table 2) without affecting the Master VCO operation. In the application circuit in Figure 15 a single reference voltage for both op amps in the loop filters is provided by two diodes to V_{CC}. If the Master VCO is affected by the FSK Modulator loop, this generally indicates a problem with the common reference voltage to the op amp, and may mean the diodes are in backwards.

Once the loops are closed you should see a phase detector output such as is shown in the Pin Function Description in Table 3. If the VCO was on frequency when the loop was open, the phase detector outputs should swing around mid supply and not hit against either the positive or negative rail. Latching to V_{CC} or V_{EE} may indicate the loop filter circuitry is not implemented correctly.

Due to the digital design of the phase detectors, the transmitter can only transition between mark and space frequencies on a clock edge. On the receive side this may be seen as a double image on the detector output, with a discrete time delay which does not vary with the frequency of the data input (see Figure 10). This is a normal consequence of using a digital phase detector and should not be confused with jitter from the data slicer.

Figure 10. Receive Data Output
(Data Transmitted from Companion MC13173)

Transmitter

The light emitting diode (LED) driver in the transmitter is capable of 6.0 to 10 mA of pull–up current. Selection of the external transistor and biasing resistor will depend on the LEDs used. Typical infrared LEDs require 50 to 100 mA of current and have a forward voltage of 1.5V. Sufficient current is needed to obtain the maximum power output without distorting the output by overdriving the LED. Key specifications include rise and fall time, wavelength, beam width (generally given in half–angle), maximum power output and efficiency. Choice of wavelengths is generally determined by cost and power efficiency, which may vary between vendors. The LEDs used in this application are at 880 nm and were chosen for best efficiency. However LEDs in general are very inefficient, converting only 1 or 2 percent of the electrical power into optical power. Multiple LEDs can be used to increase transceiver range.

Disabling the transmitter via the data bus turns off the output of the LED driver, removing the base current from the external transistor and thereby turning off the IR LED. Because of the high current drawn by the LED, this offers considerable power savings when the transmitter is not in use and can be easily controlled by a microcontroller with no additional circuitry.

In the “A/V” transmit mode, the data output is on/off keyed, with the LED on for a data high, and off for a data low. It is a baseband signal, with no carrier present (see Figure 11).

Figure 11. LED Driver Output in A/V Mode

Receiver

The receiver portion of the MC13173 is similar to the design of Motorola’s MC13156 Wideband FM Receiver. Instead of using the mixer to downconvert from a higher RF frequency, this application is designed to upconvert the 1.372 MHz input to a 10.7 MHz IF. The wide deviation, relative to the RF input frequency, requires a low Q tuned circuit to recover this bandwidth:

$$Q \approx \frac{f_c}{BW_{3\ dB}}, \text{ where } f_c = 1.372 \text{ MHz}$$

By Carson’s Rule, the BW = 2(fdev + fmod). Since for mark/space frequencies of 1.317 MHz and 1.427 MHz the deviation is fixed at ±50 kHz, the bandwidth for a 50 kHz square wave (100 kbps) would be 200 kHz, and the tuned input requires a Q of less than 7. The low Q of the tank circuit reduces both the selectivity and the sensitivity of the receiver. For a Q of 7, the resistor required across the 56 μH inductor can be calculated:

$$R = QX_L = (7) \bullet (2\pi) \bullet (1.372\ E6) \bullet (56\ E{-}6)$$
$$R = 3.3\ k\Omega$$

The 10.7 MHz ceramic filters also need to be wide enough to pass the full frequency range which will include some harmonics. In the application circuit in Figure 15, Toko filters with a bandwidth of 330 kHz or 360 kHz are recommended to accommodate higher data rates. If the IF filters are too narrow, the recovered signal may have noise on the peaks (see Figure 12).

Figure 12. Receive Data Output

The RSSI has over 70 dB of dynamic range and 20 μA of current range. The RSSI output provides the input to the carrier detect comparator (see Figure 13) and a logarithmic output proportional to the input signal level. It can, therefore, be used to recover amplitude shift keyed (ASK) data.

The key specifications for the infrared detectors are response time, sensitivity, acceptance angle, and wavelength. Some vendors offer detectors in a black package with a built–in daylight filter. Although the transparent packages offer better sensitivity, the detectors with the daylight filter offer a much better signal to noise ratio. Response time (or maximum frequency) of the system is generally limited by the capability of the emitters rather than the detectors. For this application, a rise and fall time of 500 ns is sufficient.

Design and Layout Considerations

Although the frequencies in this design are low by RF standards, careful layout and good decoupling are still good practice. The high gain limiter and IF blocks should be decoupled as shown in the application circuit as near the IC as possible for best receiver performance. Also the TTL levels from the reference oscillator and the wide current swing applied to the IR LEDs can easily be picked up on V_{CC}, creating problems for the sensitive phase detector circuits and receiver RF inputs. Avoid long parallel traces and use plenty of decoupling to keep the supply rail clean.

Typical Performance

(Measured using Application Circuit in Figure 15)

Figure 13. RSSI Output Current versus RF Input Level

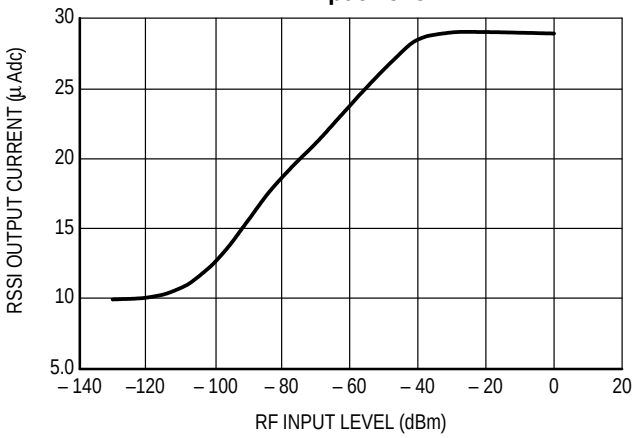


Figure 14. VCO Frequency versus Varactor Voltage

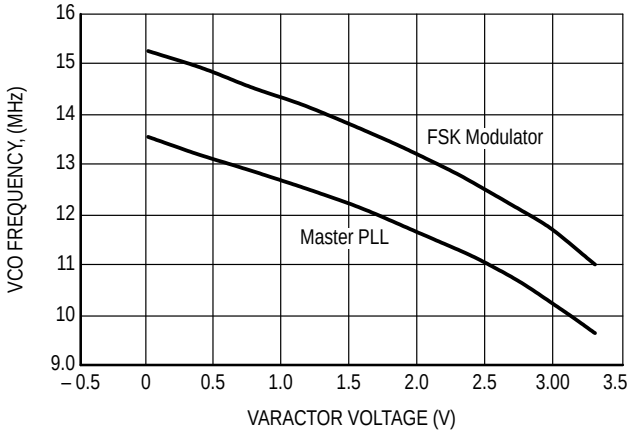
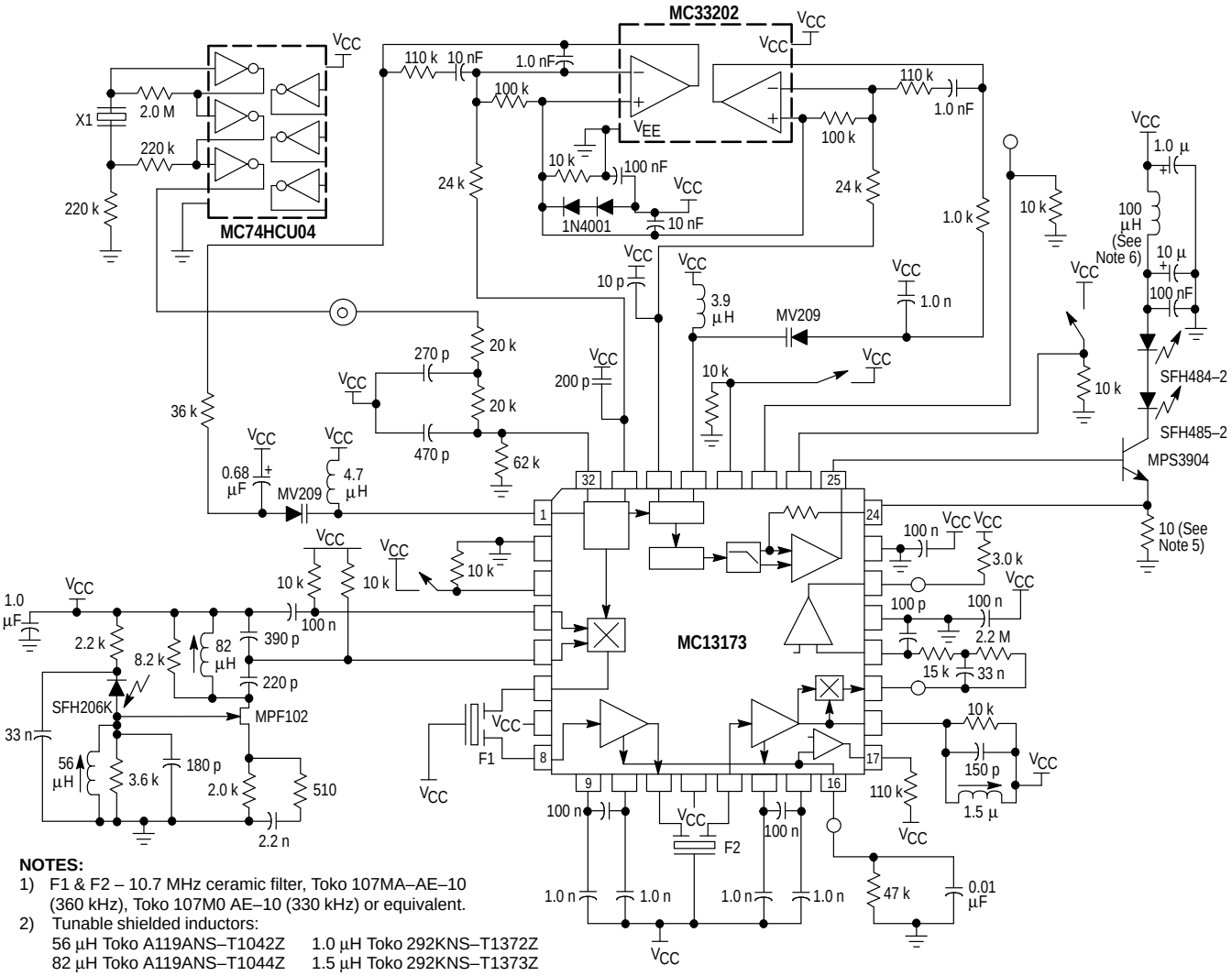


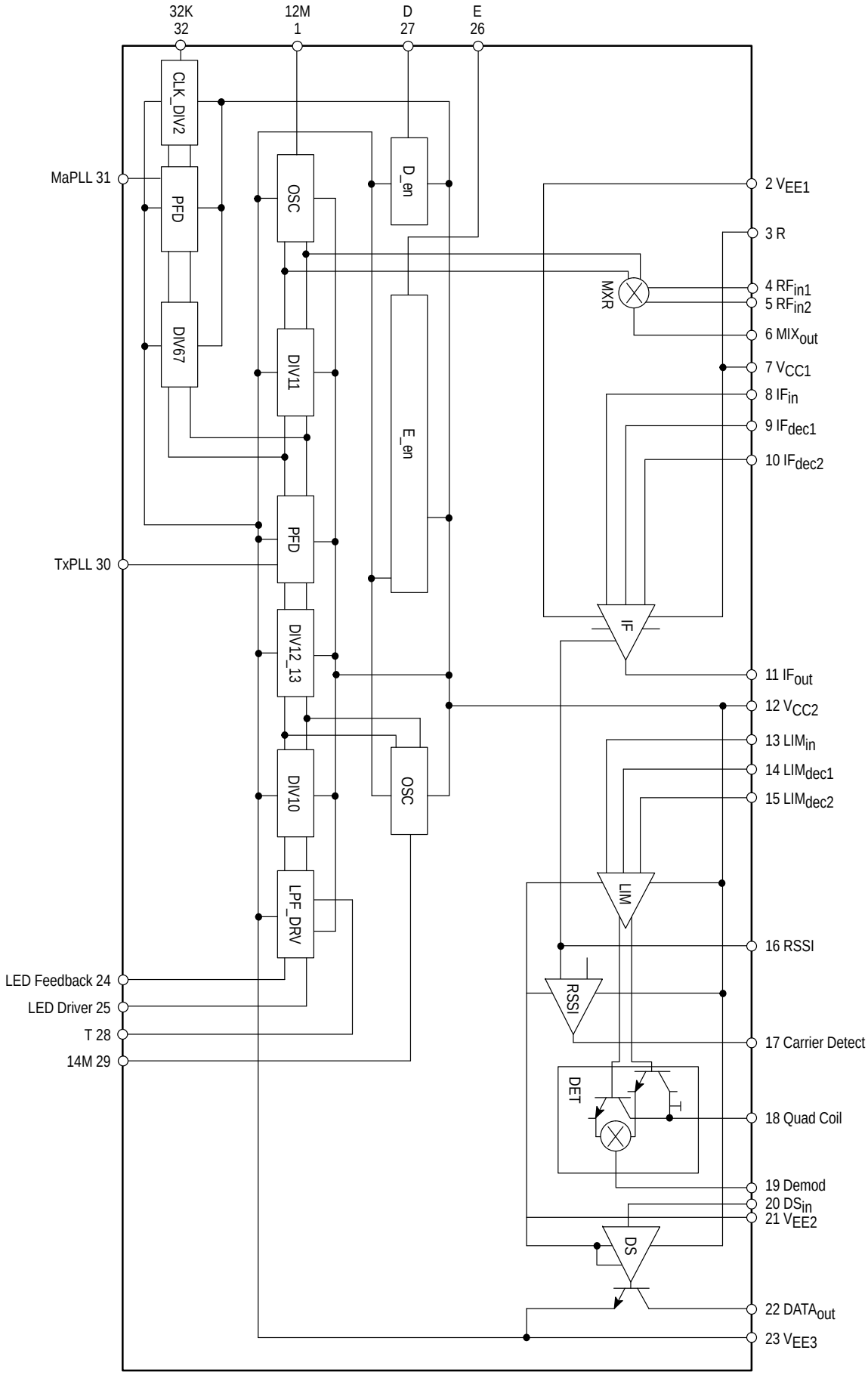
Figure 15. Application Circuit



NOTES:

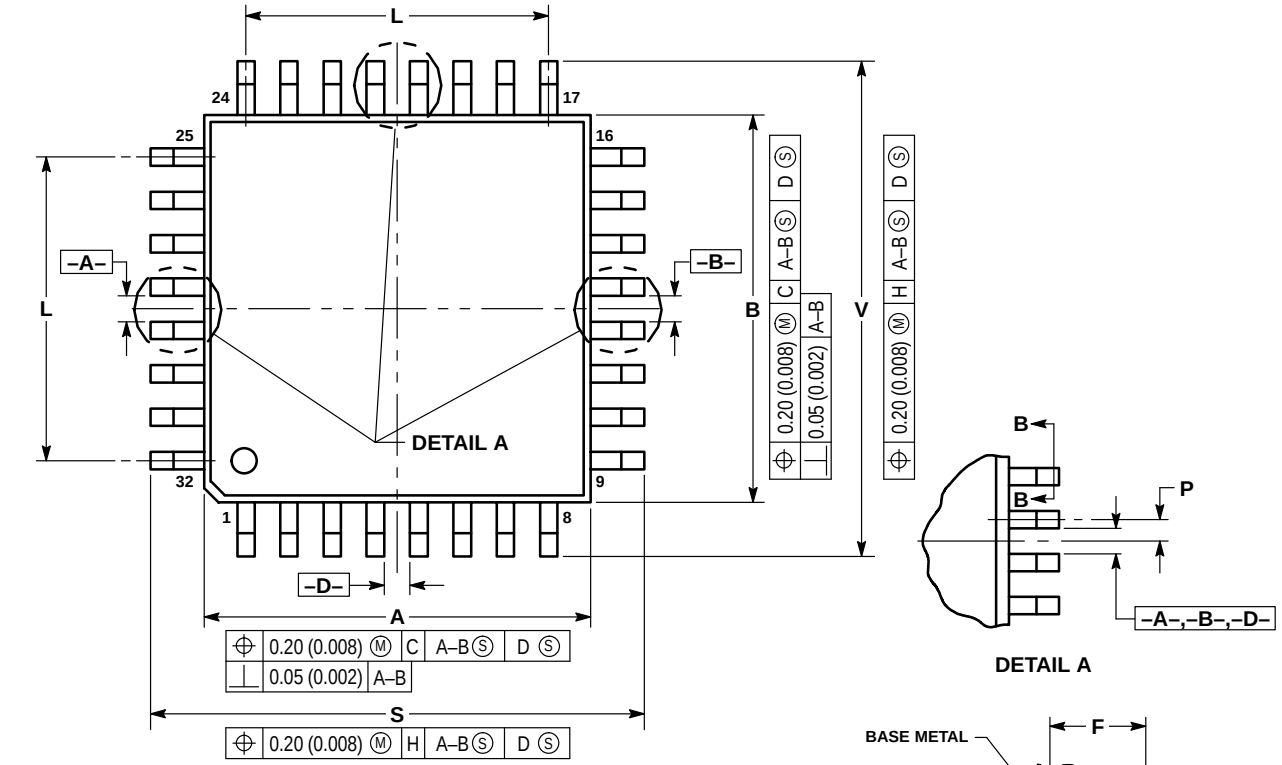
1) F1 & F2 – 10.7 MHz ceramic filter, Toko 107MA–AE–10 (360 kHz), Toko 107M0 AE–10 (330 kHz) or equivalent.
2) Tunable shielded inductors:
   56 μH Toko A119ANS–T1042Z 1.0 μH Toko 292KNS–T1372Z
   82 μH Toko A119ANS–T1044Z 1.5 μH Toko 292KNS–T1373Z
3) Crystal – 32.768 kHz C – Type tuning fork crystal. Digikey part number SE3201 or equivalent.
4) LEDs and Detectors SFH484–2, SFH485–2 and SFH206K are made by Siemens.
5) Optimum bias resistor depends on the LEDs used.
6) May be fixed or tunable.

Figure 16. Detailed Internal Block Diagram

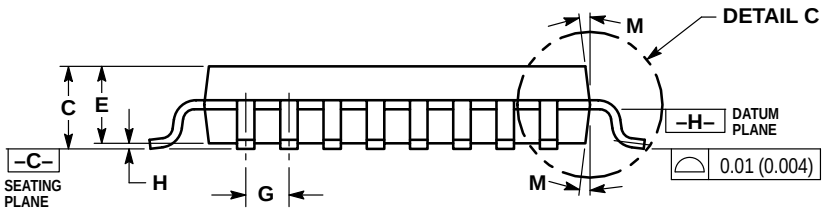


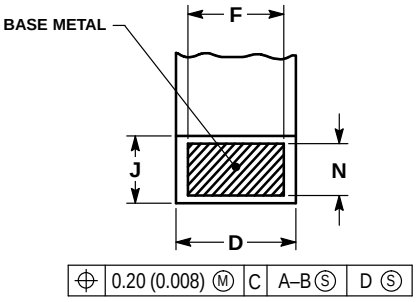
OUTLINE DIMENSIONS

FTB SUFFIX
PLASTIC TQFP PACKAGE
CASE 873–01

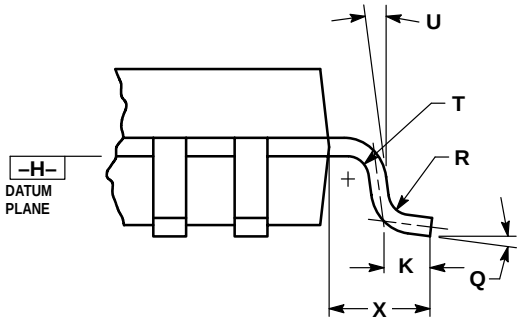


DETAIL A





SECTION B–B
VIEW ROTATED 90° CLOCKWISE



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

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