

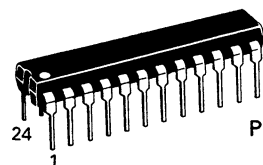
**MOTOROLA****SEMICONDUCTORS**

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

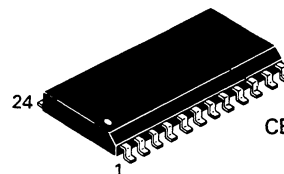
**MC13011****Product Preview****HIGH PERFORMANCE COLOR TV IF**

The MC13011 is a single channel TV IF and PLL detector system for all standard transmission systems. This device enables the designer to produce a high quality IF system with white spot inversion, AFT and AGC. The MC13011 was designed with an emphasis on linearity to minimize sound/picture intermodulation.

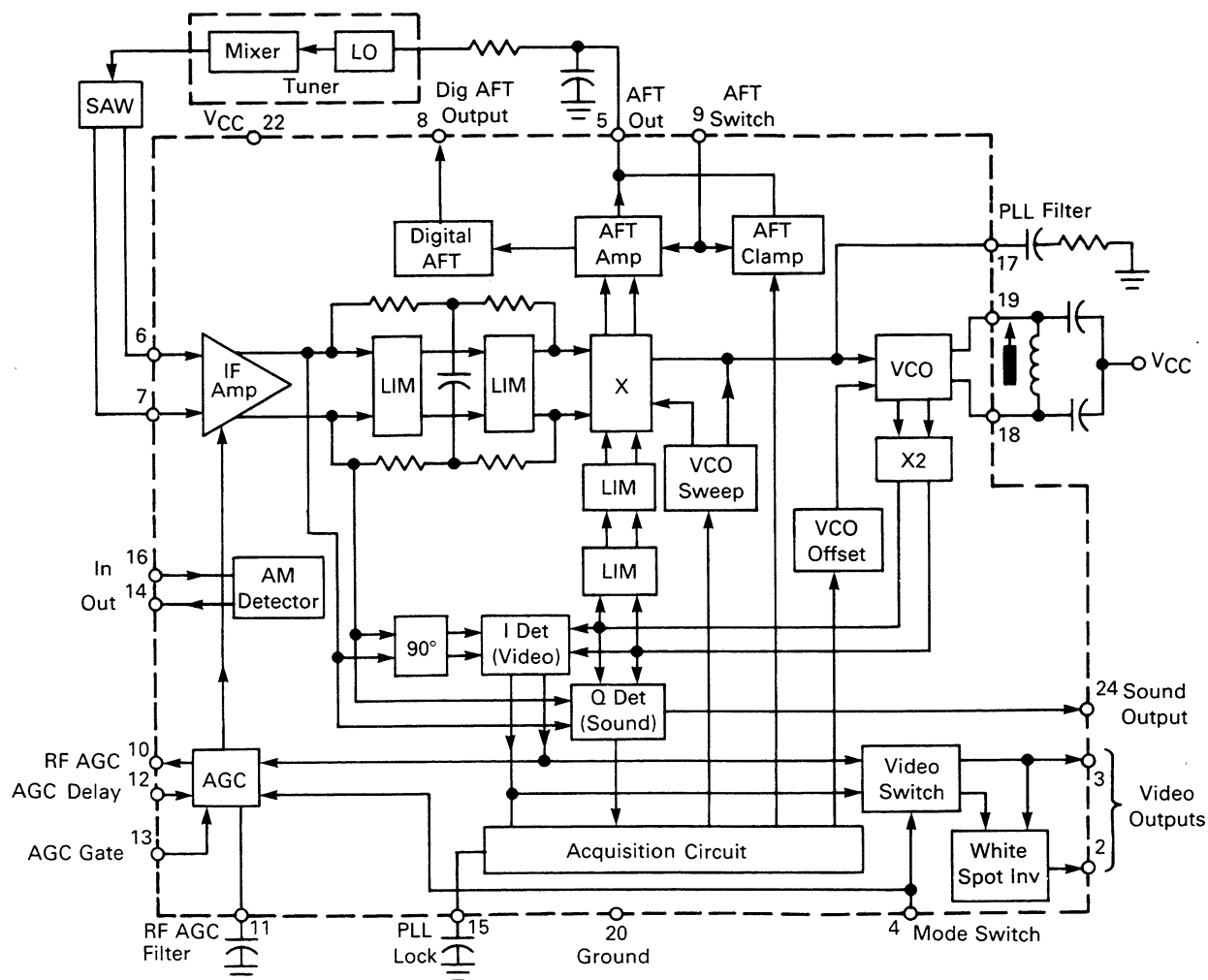
- Single Coil Adjustment for AFT and PLL
- VCO at 1/2 IF for Minimum Beats
- Simple Circuitry for Low System Cost
- White Spot Inversion
- Symmetrical  $\pm 2.0$  MHz Pull-In
- Detects Positive or Negative Modulation
- Auxiliary AM Detector for AM Sound
- Simple Alignment Procedure

**HIGH PERFORMANCE  
COLOR TV IF****SILICON MONOLITHIC  
INTEGRATED CIRCUIT**

**P SUFFIX**  
PLASTIC PACKAGE  
CASE 724-03



**DW SUFFIX**  
CERAMIC PACKAGE  
CASE 751E-01

**FIGURE 1 — BLOCK DIAGRAM**

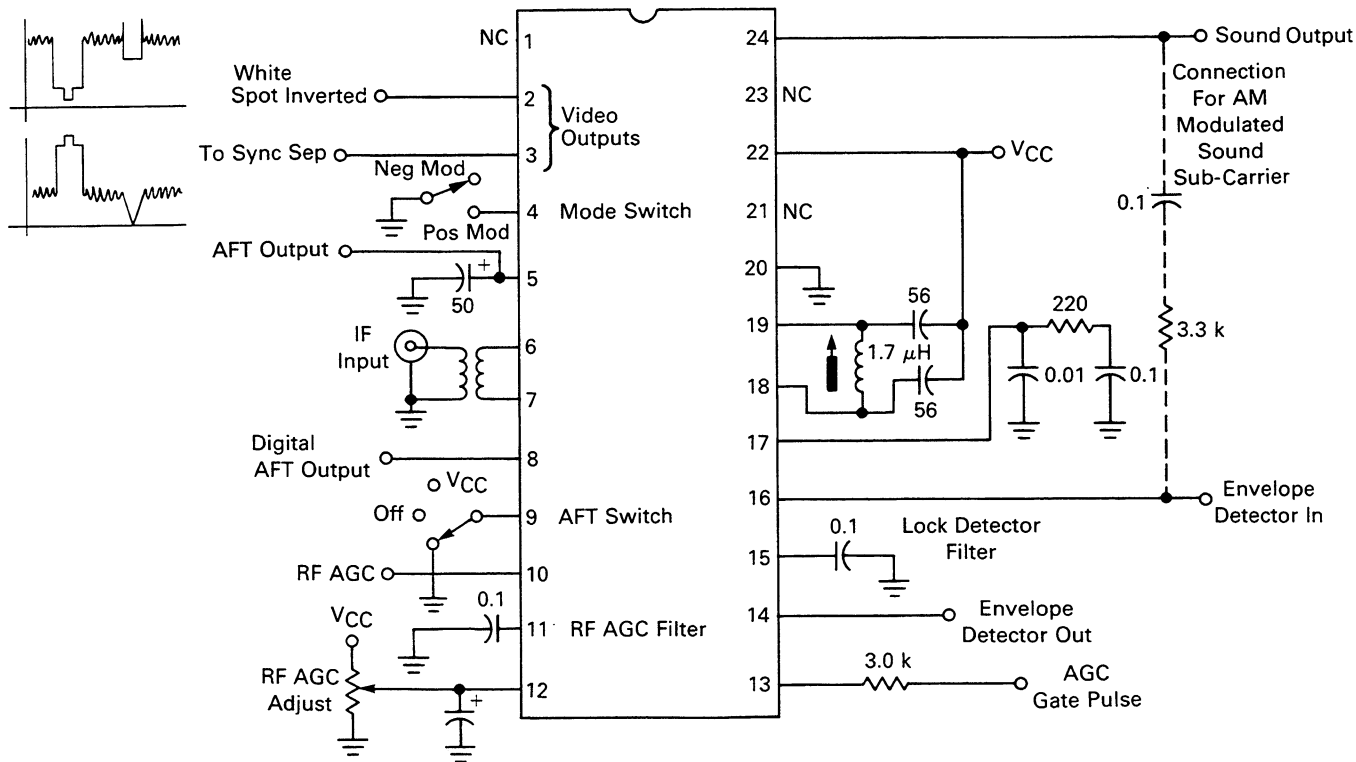
MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage — Pin 22	V <sub>CC</sub>	7.0	V <sub>dc</sub>
Gating Pulse Amplitude	V <sub>13</sub>	± 500	mApk
Operating Temperature	T <sub>A</sub>	− 40 to + 85	°C
Storage Temperature	T <sub>stg</sub>	− 65 to + 150	°C
Junction Temperature	T <sub>J</sub> Max	150	°C
Power Dissipation	P <sub>D</sub>	1.25	W
Derate above 25°C		10	mW/°C

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0 V<sub>dc</sub>, T<sub>A</sub> = 25°C unless noted)

Characteristic	Pins	Min	Typ	Max	Units
Operating Supply Voltage Range	22	4.5	—	5.5	V <sub>dc</sub>
Supply Current	22	—	50	—	mAdc
Differential Input Sensitivity for Full Output	6, 7	—	20	—	μV <sub>rms</sub>
Bandwidth	—	—	120	—	MHz
AGC Range	—	—	80	—	dB
Noise Figure	—	—	7.0	—	dB
Lock-Up Time	—	—	5.0	—	ms
Video Amplitude (100% mod depth)	2, 3	—	2.4	—	V <sub>pp</sub>
Tuner AGC Current	10	5.0	—	—	mAdc
Differential Gain Distortion	2	—	—	5.0	%
Differential Phase Distortion	2	—	—	2.0	degrees
Video Bandwidth	2, 3	—	8.0	—	MHz
Sound Subcarrier Output (− 20 dB to PIX)	24	—	0.1	—	V <sub>rms</sub>
AGC Gate Pulse (R pin 13 ≈ 5.0 k)	13	—	± 0.3	—	mApk
Differential Input Impedance	R <sub>in</sub> C <sub>in</sub>	—	3.4 3.0	—	kΩ pF

FIGURE 2 — TEST CIRCUIT



## MC13011 CIRCUIT DESCRIPTION

### Design Aims

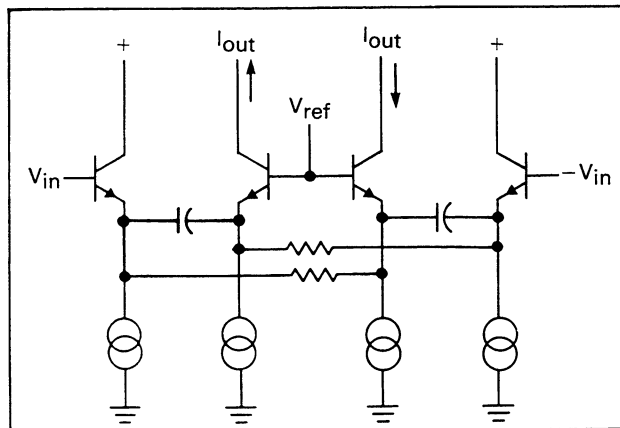
The MC13011 performs the functions of IF amplification, AGC, AFT and demodulation of a T.V. IF signal for both positive and negative modulation systems. In this respect it is similar to other circuits already on the market. However, in the means of obtaining these functions the MC13011 is very different compared to traditional designs. A unique approach was needed for several reasons. Tuned circuits associated with the IF amplifier output had to be eliminated to enable the part to be easy to use with the minimum of adjustments and external components. With this approach a high degree of IF stability could be obtained with a reduction in cost. Secondly, new techniques were required to improve performance in certain critical areas (differential phase and gain, etc.). This was especially so in view of the removal of the above mentioned tuned circuits. The basic idea therefore, was to produce an advanced, high performance multi standard IF system which would be economical and easy to use. Such a device can successfully compete with the already-established IF amplifiers now available.

### System Description

Despite the extra complications compared to pseudo synchronous demodulation, true synchronous demodulation seemed to be the only way in which enhanced performance could be achieved. The basic system is shown in Figure 1 in block diagram form. The IF amplifier is a four stage, AC coupled design having a sensitivity of about  $20 \mu\text{V}$ . With a low loss SAW filter and 3.0 to 6.0 dB extra gain in the tuner, there is no need for a SAW pre-amp. The T.V. set signal to noise performance is acceptable, while the net savings in cost is considerable. The AGC is a conventional gated system with the usual RF AGC output and RF AGC adjustment. Three stages of the amplifier are gain controlled to give an extended AGC range of 80 dB with improved intermodulation, signal handling, and differential phase and gain performance. The AGC reference is switched when positive modulation is selected, via the mode switch, to ensure the video level remains constant. Under these circumstances the AGC must be gated by a pulse which will sample the back porch, as opposed to negative modulation where flyback can be used. In both cases a positive or negative-going pulse may be used. To ensure that the improvements in performance mentioned above were not lost elsewhere, great care was taken in the design of the video demodulator and video amplifiers. An example of this care is the placing of the phase shift required by the video demodulator on the signal side instead of on the oscillator side of the demodulator as is common practice. The  $90^\circ$  phase shift is produced by replacing the usual emitter resistors by capacitors in the diff. amp (Figure 3) feeding the video demodulator. The output currents are  $90^\circ$  with respect to the input voltage over a wide band of frequencies and the small phase errors caused by the transistor

small signal emitter resistances ( $r_e$ ) are corrected by the cross-coupled resistors. This arrangement leads to a simpler design, the ability to adjust the demodulation angle, and lower distortion than is normal at the IF amplifier/demodulator interface. The dynamic emitter resistances, which can give rise to distortion, are now in quadrature with the capacitive reactance and, therefore, contribute very little to the resultant output.

FIGURE 3 —  $90^\circ$  PHASE SHIFT AMPLIFIER



Following the IF amp and preceding the PLL phase detector is a two stage limiter with a gain of 100 and overall dc feedback. This contrasts with the usual single stage of limiting with no dc feedback and a tuned circuit with diodes at its output. With two stages of limiting, the minimum gain required to remove signal amplitude modulation can be designed-in without the large voltage swings of a single stage with the same gain. Large voltage swings lead to poor differential phase and gain performance, hence the need for a tuned circuit and diodes as used in previous designs. The dc feedback removes the effects of input offsets which are another source of differential phase and gain problems. The combination of low swing per stage and dc feedback removes the need for having a tuned circuit at the output of the limiter and reduces the danger of IF instability and radiation. The only problem in using this technique is the potential for extra static phase shift and resultant errors in the demodulating angles at the video and sound demodulators. However, by putting a similar two stage limiter, with matching phase shift, on the oscillator side of the phase detector, the demodulating angles can be restored to the correct phases ( $0^\circ$ ,  $90^\circ$ ). Having processed the signal in this way, the VCO is then phase locked at  $90^\circ$  to the non-limited signal. The only unusual feature of the loop just described is that the VCO runs at half frequency, and is frequency doubled on-chip. This means radiation from the external frequency determining components will be at "half IF" and so will not desensitize the system even if picked up by the amplifier input leads (this could cause what is known as PLL push-off). Running the oscillator at twice IF frequency and dividing down, which is another way of



solving this problem has several disadvantages. First and foremost, radiation into the antenna at twice IF produces channel 6 and channel 8 problems in the U.S.A. Secondly, it is easier to produce a stable VCO at half IF.

After attaining phase lock, demodulation of the video is achieved by multiplying the signal (non limited) with the regenerated vision carrier (VCO) in a double balanced multiplier, the phase relationship between the two waveforms being zero degrees. Both positive and negative sync video outputs are produced.

FIGURE 4 — PIN 2 VIDEO OUTPUT WITH WHITE-SPOT INVERSION

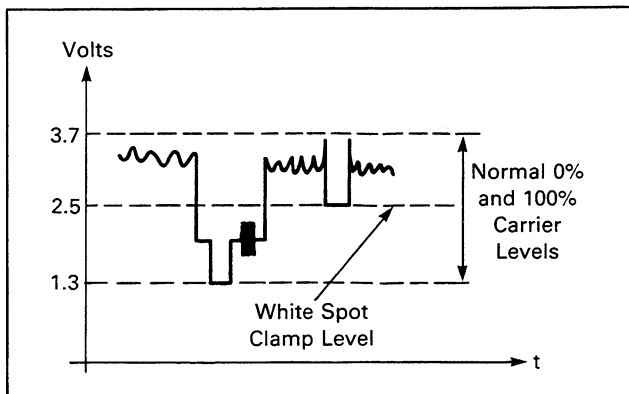
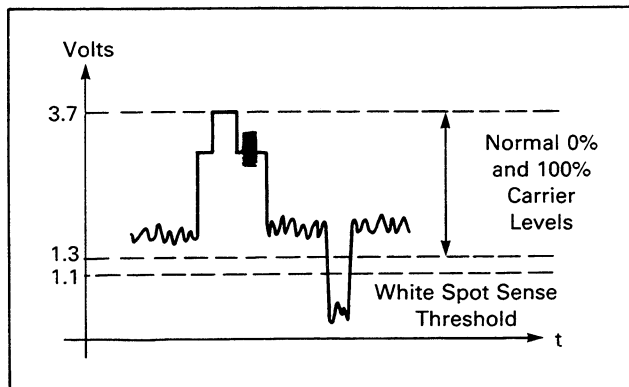


FIGURE 5 — PIN 3 VIDEO OUTPUT FOR DRIVE TO A SYNC SEPARATOR



The negative sync output is intended to be used as the actual video and is acted upon by the white spot noise inverter. This effectively removes the "whiter than white" noise produced by a true synchronous demodulator and prevents the C.R.T. from being over-driven and defocused. The positive sync video output is not acted on by a white spot noise inverter and of course the noise output from a synchronous detector does not contain a dc component. Hence, this drive should be used as the sync separator drive because a simple pre-separator low pass noise filter will produce optimum sync performance. Note the sense of the video signals at the outputs remain the same whether positive or negative modulation is being received. Positive or negative modulation is selected externally by the mode switch pin. The sound intercarrier is recovered by

another demodulator similar to the video, except that the phase relationship between the signal and the VCO is 90° instead of 0°. A consequence of this phase relationship is that video interference of the intercarrier signal at the detector output is minimized by suppression of the lower frequency video components. Should the sound carrier contain amplitude information, as in the French T.V. system or as in some scrambled cable signals, this information can be recovered by feeding the sound intercarrier output back into the circuit through a bandpass filter if so desired, to the amplitude detector provided on chip.

The AFT portion of the circuit is the most unconventional in form. Essentially, AFT is derived by amplifying the error signal driving the VCO after phase lock, and applying this to the local oscillator in the tuner, thus eliminating a coil and a potential IF instability problem. After acquisition, and when the circuit has settled down, due to the much higher gain in the LO loop, the VCO will have moved a small amount ( $\Delta f_v$ ) from its nominal frequency, and almost all the original error frequency ( $\Delta f_e$ ) between LO and VCO will have been corrected by the change in LO frequency ( $\Delta f_l$ ). In this way, provided the PLL can be initially locked to the incoming IF signal, the VCO can be used as the frequency reference for the AFT system. It follows from the above therefore, because the system is phase locked, that  $\Delta f_e = (\Delta f_l + \Delta f_v)$ . The combination of the local VCO loop and the loop produced by feedback to the LO forms a double loop PLL. Analysis shows that overall system stability can be assured by treating the VCO loop as a stand alone PLL, provided its bandwidth is much wider than the LO loop. The VCO loop therefore is a low gain wide band loop which guarantees initial capture, while the LO loop is basically a high gain dc loop used to keep frequency and phase offsets to a minimum. Large phase offsets can also be caused by dc offsets in the phase detector and AFT amplifier. These are removed by the use of commutation on both the phase and AFT outputs. This eliminates the need for external phase adjustment, while at the same time minimizing distortion by maintaining the correct phase angles at the demodulators.

The AFT system has been designed to acquire the vision carrier, without false locking to the sound or adjacent sound carriers, with an initial LO frequency error of  $\pm 2.0$  MHz, reducing this initial error to 3.0 to 10 kHz when locked. This contrasts to the discriminator type of AFT's which have highly asymmetric lock characteristics ( $-2.0$  MHz  $+ 1.0$  MHz), because of the effects of the IF filter, and large frequency errors caused by limited loop gain. To achieve this level of performance without encountering the normal AFT problems associated with high loop gain, a novel approach has been taken to locking up to the PLL. In the absence of an IF signal, the acquisition circuitry examines the state of the video (I) and sound (Q) demodulators and detects the lack of a signal. It then clamps the LO drive to a reference dc level and applies a  $-2.0$  MHz offset to the VCO. This is done so that the nominal IF (should a signal appear), and the VCO, are sitting in the center of the IF filter passband. Therefore, even if the LO drifts high by  $+2.0$



MHz, the signal will not be significantly attenuated by the filter. When the acquisition circuit detects the appearance of a signal, beat notes are produced at the output of the demodulators, a sweep generator is switched on, and immediately sweeps the VCO an additional  $-2.0$  MHz from its out of lock nominal frequency.

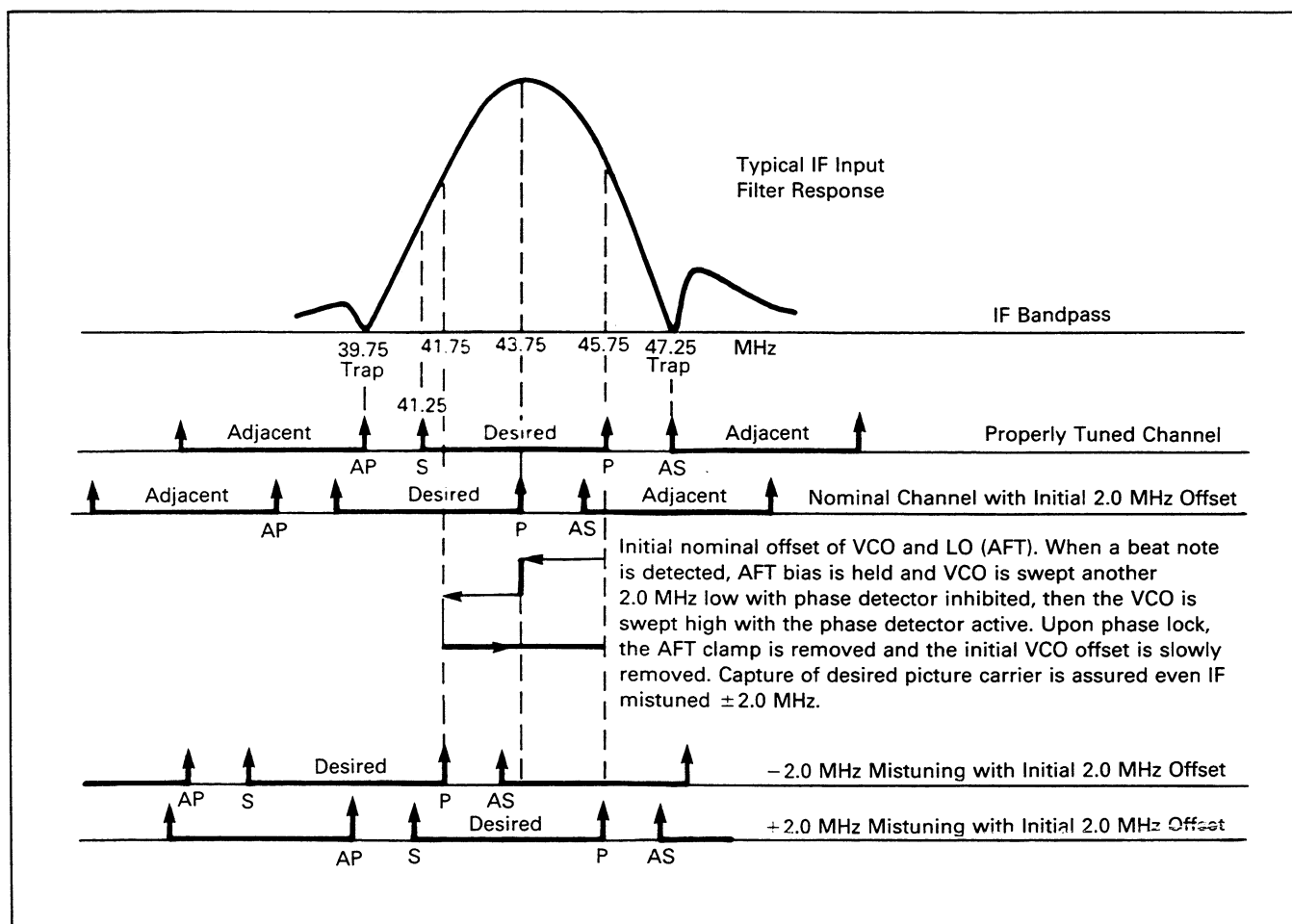
During this negative sweep, the PLL phase detector is switched off so phase lock cannot be obtained. The VCO is then swept positive from  $-2.0$  MHz to  $+2.0$  MHz of nominal with the phase detector switched on. The PLL will therefore lock to the first carrier it encounters. This in fact must be the vision carrier because the sound carrier is more negative than  $-2.0$  MHz from nominal and the adjacent sound carrier is higher than the vision carrier. On achieving phase lock, the AFT clamp is released, the VCO offset is slowly removed, the sweep is inhibited and the phase detector remains enabled. With the AFT clamp removed, a large error voltage appears at the AFT output, driving the system back towards the correct frequency. Since the LO loop is slow and the VCO is fast, the IF changes slowly and the VCO tracks it, maintaining phase lock until the final static conditions are reached. For large frequency errors during this period the slew rate of the LO loop is increased,

but not to the extent where it would cause any VCO tracking problems. This technique allows the acquisition time of the circuit to be considerably shortened while still using a larger than normal time constant in the LO loop. To accommodate all types of tuners and LO's, positive or negative LO drive can be selected externally by operation of the AFT switch. The AFT switch also has a third position which disconnects the drive to the tuner. Under this condition the T.V. set can be tuned in the normal manner and so appears to have a conventional type of AFT. Other PLL AFT systems cannot be manually tuned in this way having an abrupt capture characteristic when tuned, and because of this, have not gained general acceptance in industry.

### ALIGNMENT

The alignment is very simple and cheap compared to other IF amplifier circuits, especially those using a PLL. With a CW input signal of correct picture carrier frequency, the LO side of the  $22$  k resistor in series with the loop is connected to a dc supply. The dc supply (approximately  $2.5$  V) is adjusted until the output of the tuner is  $45.75$  MHz. The VCO coil is adjusted until lock is obtained and the voltage across the  $22$  k resistor is

FIGURE 6 — THE AFT SYSTEM IN ACTION



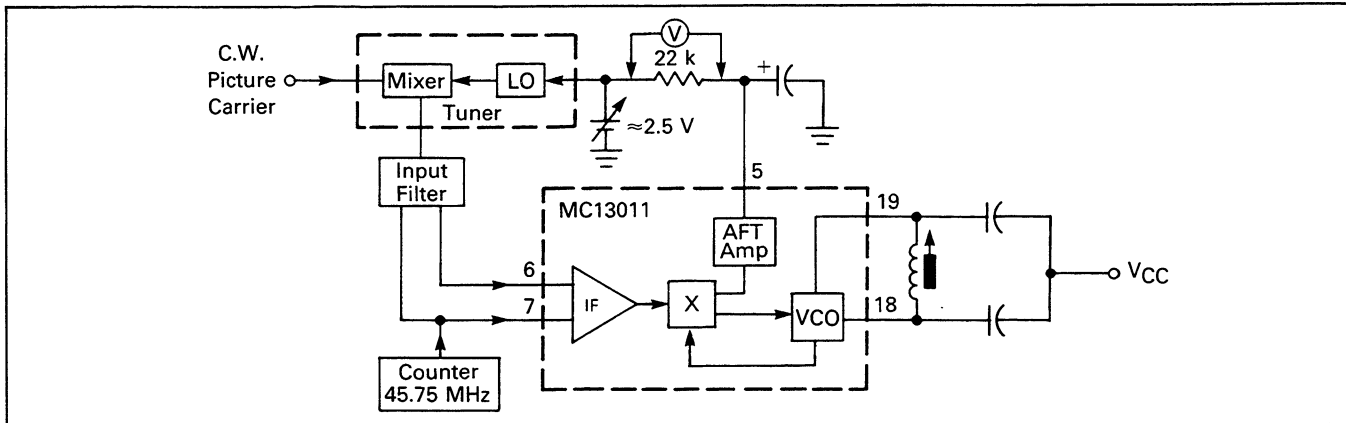
zero. The dc supply is then removed.

A digital AFT up/down output having a  $\pm 30$  kHz dead zone is also provided by the circuit. Again, as in the case of the analog output, the digital output polarity can be controlled externally by the AFT switch.

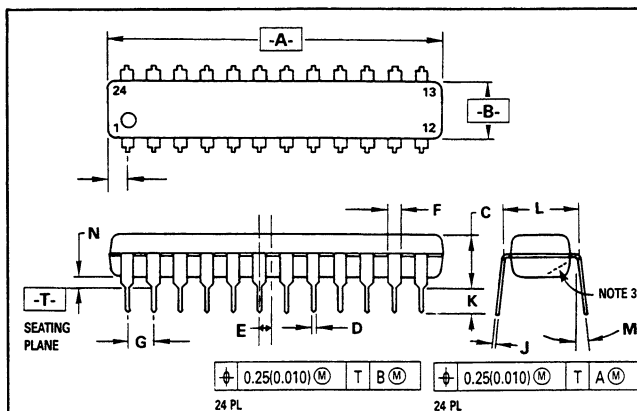
#### Note:

Most pins on the IC have electrostatic protection diodes to  $V_{CC}$  and ground. It is therefore imperative that no pin is taken below ground or above  $V_{CC}$  by more than one diode drop without current limiting.

FIGURE 7 — ALIGNMENT CONFIGURATION



#### OUTLINE DIMENSIONS

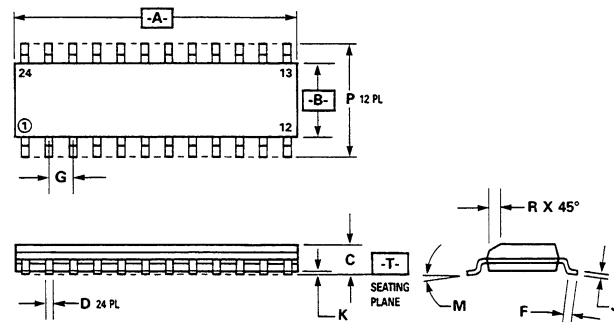


#### NOTES:

1. CHAMFERED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

P SUFFIX  
PLASTIC PACKAGE  
CASE 724-03



#### NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (24 PLACES):  
 $\pm 0.25 (0.010) \text{ (M) T B (S) A (S)}$
3. POSITIONAL TOLERANCE FOR P DIMENSION (12 PLACES):  
 $\pm 0.25 (0.010) \text{ (M) B (M)}$
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.50	0.601	0.610
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX  
CERAMIC PACKAGE  
CASE 751E-01



This page intentionally left blank.



Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**Literature Distribution Centers:**

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.



**MOTOROLA**

21640 PRINTED IN USA (1994) MPS/POD

MC13011/D

