MC10SX1190

Fibre Channel Coaxial Cable Driver and Loop Resiliency Circuit

The MC10SX1190 is a differential receiver, differential transmitter specifically designed to drive coaxial cables. It incorporates the output cable drive capability of the MC10EP89 Coaxial Cable Driver with additional circuitry to multiplex the output cable drive source between the cable receiver or the local transmitter inputs. The multiplexer control circuitry is TTL compatible for ease of operation.

The MC10SX1190 is useful as a bypass element for Fibre Channel-Arbitrated Loop (FC-AL) or Serial Storage Architecture (SSA) applications, to create loop style interconnects with fault tolerant, active switches at each device node. This device is particularly useful for back panel applications where small size is desirable.

The EP89 style drive circuitry produces swings approximately 70% larger than a standard PECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize reflections. The 1.4V output swings allow for proper termination at both ends of the cable, while maintaining the required swing at the receiving end of the cable. Because of the larger output swings, the QT, $\overline{QT}$ outputs are terminated into the thevenin equivalent of 50Ω to V_{CC} – 3.0V instead of 50Ω to V_{CC} – 2.0V.

- 2.5 Gbps Operation
- 425ps Propagation Delay
- 1.4V Output Swing on the Cable Driving Output
- PECL Mode: 3.0V to 5.5V V_{CC}, with V_{EE} = 0V
- ECL Mode: 0V V_{CC}, with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pull Down Resistors
- 2000 V H.B.M. ESD Protection, >100 V mm

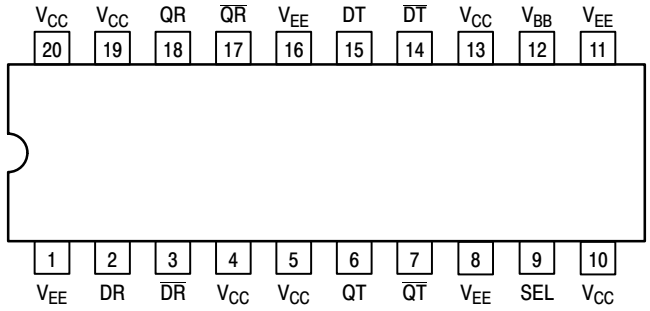

Figure 1. 20-Lead TSSOP Pinout: (Top View)

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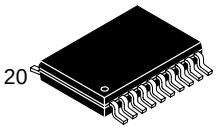
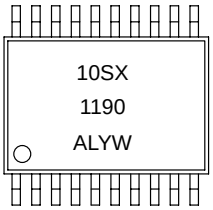


TSSOP–20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION

PIN	FUNCTION
DR/$\overline{DR}$	ECL Diff. Inputs from Receive Cable
QR/$\overline{QR}$	ECL Buffered Differential Outputs from Receive Cable
DT/$\overline{DT}$	ECL Differential Input to Transmit Cable
QT/$\overline{QT}$	ECL Buffered Differential Output to Transmit Cable
SEL	TTL Multiplexer Control Signal
V_{BB}	Reference Voltage Output
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative, 0 Supply

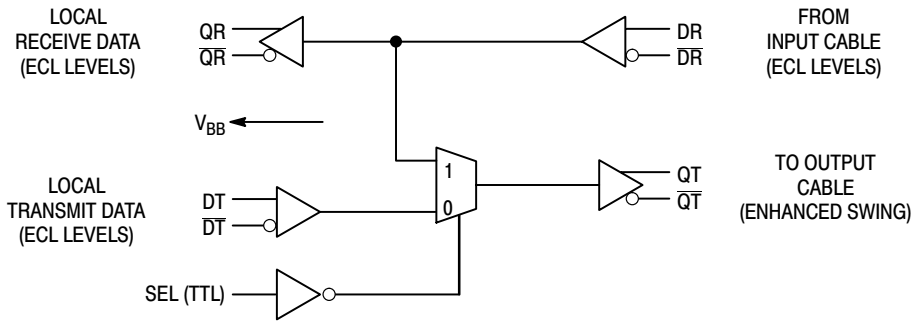
TRUTH TABLE

SEL	Function
L	DR → QT
H	DT → QT

ORDERING INFORMATION

Device	Package	Shipping
MC10SX1190DT	TSSOP–20	75 Units/Rail

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage (V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	Power Supply Voltage (V_{CC} = 0V)	–6.0 to 0	Vdc
V_{IN}	Input Voltage (V_{EE} = 0V, V_{IN} not more positive than V_{CC})	0 to +6.0	Vdc
V_{IN}	Input Voltage (V_{CC} = 0V, V_{IN} not more negative than V_{EE})	–6.0 to 0	Vdc
I_{OUT}	Output Current — Continuous Surge	50 100	mA
θJA	Thermal Resistance (Junction–to–Ambient) — Still Air 500 LFPM	90 60	°C/W
θJC	Thermal Resistance (Junction–to–Case)	30 to 35	°C/W
T_A	Operating Temperature Range	–40 to +85	°C
T_{STG}	Storage Temperature Range	–50 to +150	°C

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

DC CHARACTERISTICS (Note 1)

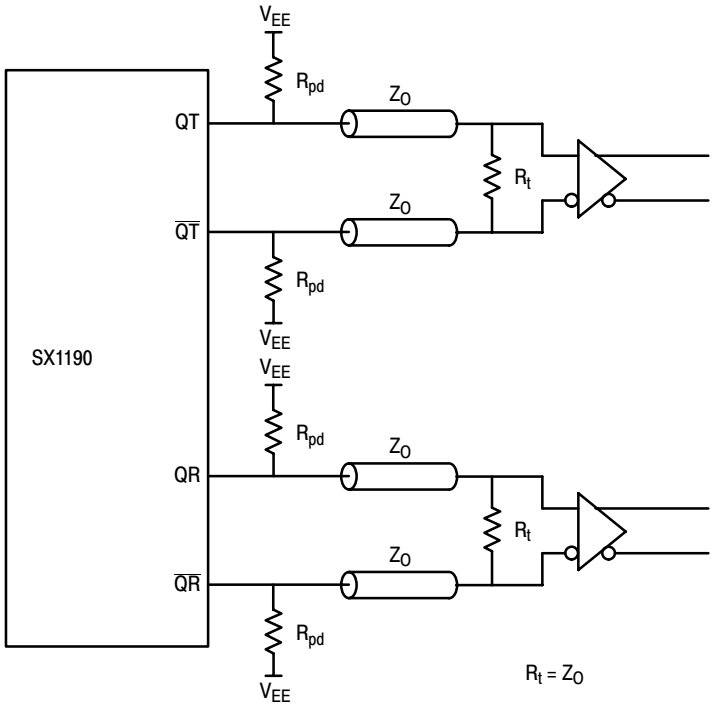
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output Voltage High (QR,$\overline{QR}$) V_{CC} = 5.0V, V_{EE} = 0V (Notes 2,3)	3.93	4.03	4.13		4.04		3.98	4.08	4.18	4.03	4.13	4.23	V
V_{OL}	Output Voltage Low (QR,$\overline{QR}$) V_{CC} = 5.0V, V_{EE} = 0V (Notes 2,3)	2.92	3.12	3.32		3.26		2.94	3.14	3.34	2.96	3.16	3.36	V
V_{OH}	Output Voltage High (QT,$\overline{QT}$) V_{CC} = 5.0V, V_{EE} = 0V (Notes 2,4)	3.84	3.94	4.04		3.98		3.94	4.04	4.14	4.05	4.15	4.25	V
V_{OL}	Output Voltage Low (QT,$\overline{QT}$) V_{CC} = 5.0V, V_{EE} = 0V (Notes 2,4)	2.00	2.20	2.40		2.49		1.90	2.10	2.30	1.85	2.05	2.25	V
I_{CC}	Quiescent Supply Current (Note 5)	75	95	115				75	95	115	75	95	115	mA
V_{IH}	Input Voltage High (DR,$\overline{DR}$ & DT,$\overline{DT}$) V_{CC} = 5.0V, V_{EE} = 0V (Note 2)	3.77		4.11	3.83		4.16	3.87		4.19	3.94		4.28	V
V_{IL}	Input Voltage Low (DR,$\overline{DR}$ & DT,$\overline{DT}$) V_{CC} = 5.0V, V_{EE} = 0V (Note 2)	3.05		3.50	3.05		3.52	3.05		3.52	3.05		3.56	V
V_{IH}	Input Voltage High SEL (Note 6)	2.0			2.0			2.0			2.0			V
V_{IL}	Input Voltage Low SEL (Note 6)			0.8			0.8			0.8			0.8	V
V_{BB}	Output Reference Voltage V_{CC} = 5.0V, V_{EE} = 0V (Note 2)	3.50	3.60	3.75	3.62	3.67	3.73	3.50	3.60	3.70	3.55	3.65	3.75	V

1. 10SX circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is mounted in a test socket or mounted on a printed circuit board and transverse air greater than 500lfm is maintained.
2. Values will track 1:1 with the V_{CC} supply.
3. Outputs loaded with 50Ω to V_{CC} –3 V
4. Outputs loaded with 50Ω to V_{CC} –2 V
5. Outputs open circuited.
6. TTL signal threshold is 1.5V above V_{EE}.

AC CHARACTERISTICS (Note 1 & 7)

Symbol	Characteristic	–40°C			25°C to 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
t_{pd}	Propagation Delay DR → QR (Diff) to Output	140	240	340	180	280	380	ps	Note 2 Note 3
	DR → QT (Diff)	300	400	500	350	470	650		
	DT → QT (Diff)	280	380	480	350	440	650		
t_{PLH}, t_{PHL}	Propagation Delay SEL → QT,$\overline{QT}$	400	700	1000	400	700	1000	ps	1.5V to 50% Pt
t_r, t_f	Rise Time QR,$\overline{QR}$ Fall Time	70	140	200	90	155	250	ps	20% to 80% 80% to 20%
t_r, t_f	Rise Time QT,$\overline{QT}$ Fall Time	150	200	280	150	230 230	500	ps	20% to 80% 80% to 20%
t_{skew}	Within Device Skew		15			15		ps	Note 4
V_{PP}	Minimum Input Swing	200			200			mV	Note 5
V_{CMR}	Common Mode Range	3.0		4.35	3.0		4.35	V	Note 6
f_{max}	Maximum Operation Frequency	2.5			2.5			Gb/s	

1. 10SX circuits are designed to meet the AC specifications shown in the table after thermal equilibrium has been established. The circuit is mounted in a test socket or mounted on a printed circuit board and transverse air greater than 500lfm is maintained.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. Duty cycle skew is the difference between t_{PLH} and t_{PHL} propagation delay through a device.
5. Minimum input swing for which AC parameters are guaranteed.
6. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\ Min}$ and 1.0V.
7. Data taken at $V_{CC,\ nom}$ = 3.3V.



Typical value for R_{pd} is 160Ω to 260Ω, depending on the application. The minimum value of R_{pd} should not be less than 50Ω.

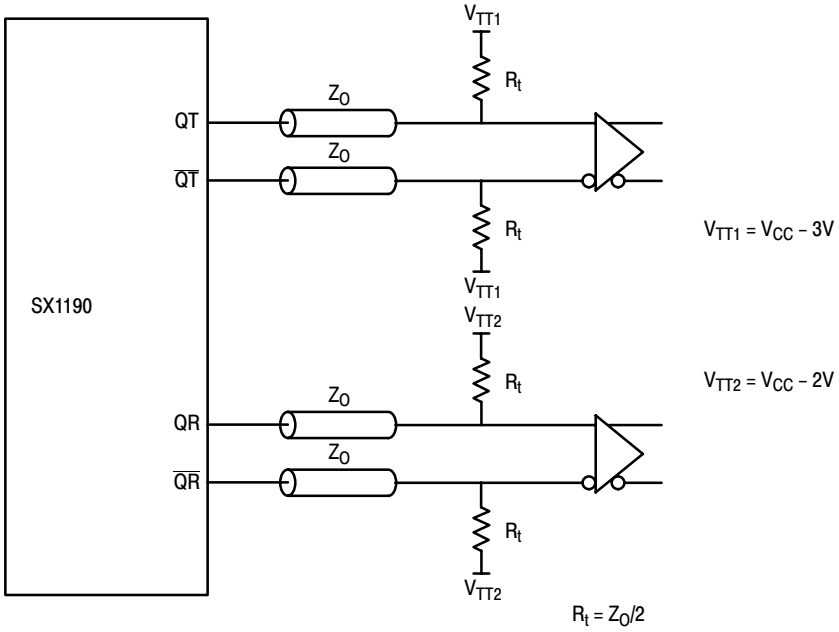
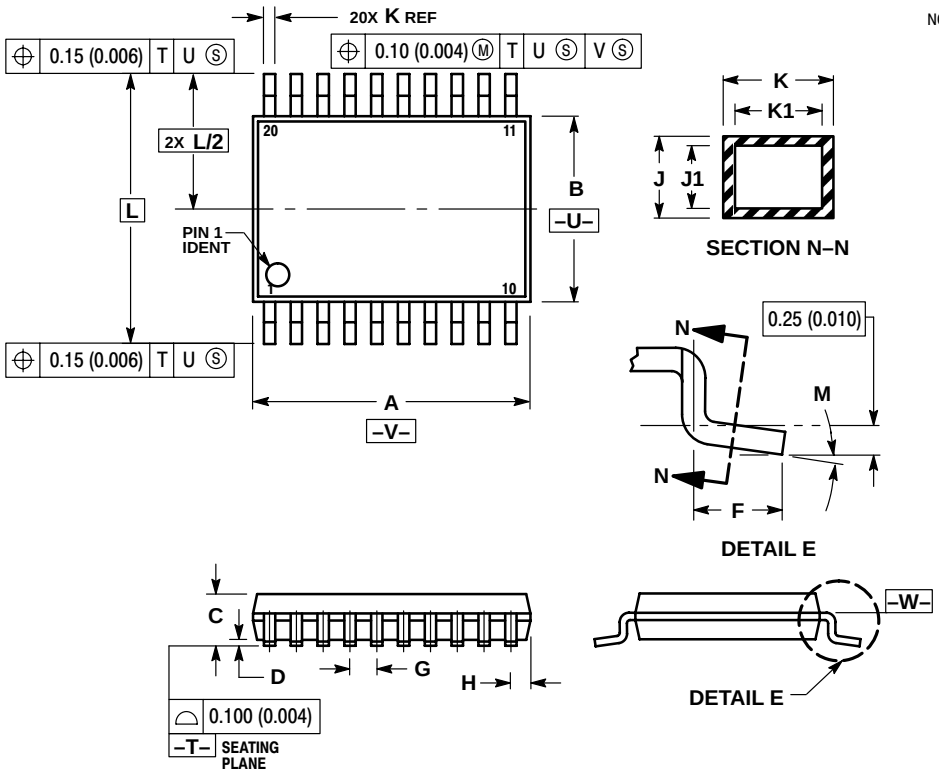


Figure 2. SX1190 Termination Configuration

PACKAGE DIMENSIONS

DT SUFFIX
PLASTIC PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. ICONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Notes

Notes

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