MC10SX1125A

Product Preview

622Mb/s Fiber Optic Post Amplifier

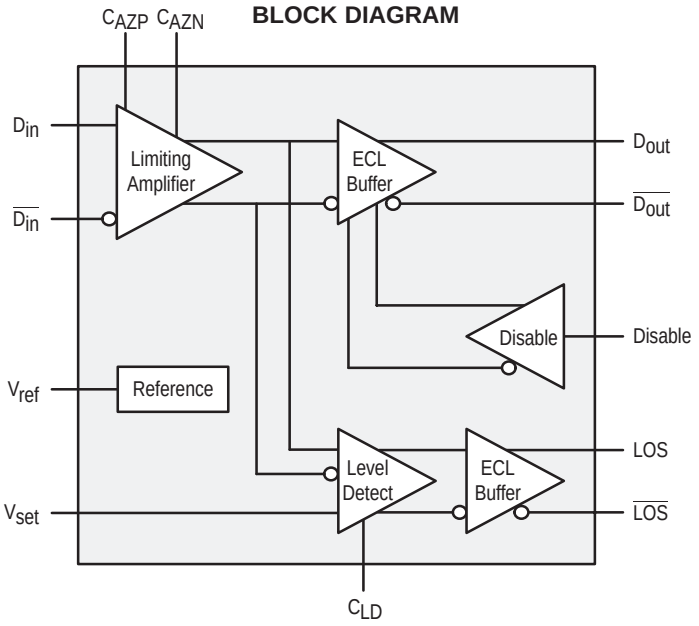
The SX1125A is an integrated limiting amplifier for high frequency fiber optic applications. The device interfaces directly to the trans–impedance amplifier of a typical optical to electrical conversion portion of a fiber optic link. With data rate capabilities in the 622Mb/s range, the high gain limiting amplification of the SX1125A is ideal for high speed fiber optic applications like SONET/SDM, ATM, FDDI, Fibre Channel or Serial Hippi. The device is functionally and pin compatible to the Signetics SA5225 with a significantly higher bandwidth. The C_{AZP} and C_{AZN} inputs to the limiting amplifier provide an auto-zero function to effectively cancel any input offset voltage present in the amplifier.

The SX1125A incorporates a programmable level detect function to identify when the input signal has been lost. This information can be fed back to the Disable input of the device to maintain stability under loss of signal conditions. Using the V_{set} pin the sensitivity of the level detect can be adjusted. The C_{LD} input is used to filter the level detect input so that random noise spikes are filtered out.

The MC10SX1125A is compatible with MECL10H logic levels.

- Wideband Operation: 20kHz to 550MHz
- Programmable Input Signal Level Detection
- Operation with single +5V or standard ECL supply
- Standard 16-lead SOIC Package
- Fully Differential Design to Minimize Noise Affects
- 10KH Compatible

BLOCK DIAGRAM



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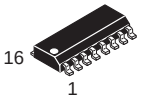
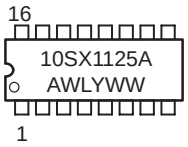
MARKING DIAGRAM

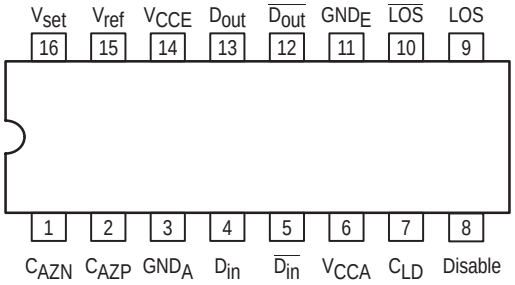


SO–16
D SUFFIX
CASE 751B



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

PIN ASSIGNMENT



Pinout: 16-Lead Plastic Package
(Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC10SX1125AD	SO–16	48 / Rail
MC10SX1125ADR2	SO–16	2500 / Reel

FUNCTION TABLE

Pin	Function
C_{AZN}	Auto-zero capacitor pin. A capacitor between this pin and C_{AZP} cancels any offset inherent to the limiting amplifier.
C_{AZP}	Auto-zero capacitor pin. A capacitor between this pin and C_{AZN} cancels any offset inherent to the limiting amplifier.
GND_A	Analog ground pin. Ground for PECL operation or –5.2V for standard ECL operation. GND_A and GND_E must be at the same potential.
D_{in}, $\overline{D_{in}}$	Differential data input.
V_{CCA}	Analog power supply pin. +5V for PECL operation or ground for standard ECL operation. V_{CCA} and V_{CCE} must be at the same potential.
C_{LD}	Filter capacitor for the level detect comparator. Capacitor should be connected to V_{CCA}.
Disable	When asserted LOW, or left open and pulled LOW via the input pulldown resistor, the output buffer will be enabled and will respond to the input stimulus on the D_{in} input. Forcing Disable HIGH will force the D_{out} output LOW and its complimentary output HIGH.
LOS	Loss of signal. This output will go HIGH when the input signal falls below (V_{set}/100) mV_{P-P}.
GND_E	Digital ground pin. Ground for PECL operation or –5.2V for standard ECL operation. GND_A and GND_E must be at the same potential.
D_{out}, $\overline{D_{out}}$	Differential data outputs.
V_{CCE}	Digital power supply pin. +5V for PECL operation or ground for standard ECL operation. V_{CCA} and V_{CCE} must be at the same potential.
V_{ref}	Reference voltage for threshold level set voltage division network (2.64V).
V_{set}	Input threshold level detect setting input. Input generated from voltage divider between V_{ref} and GND_A.

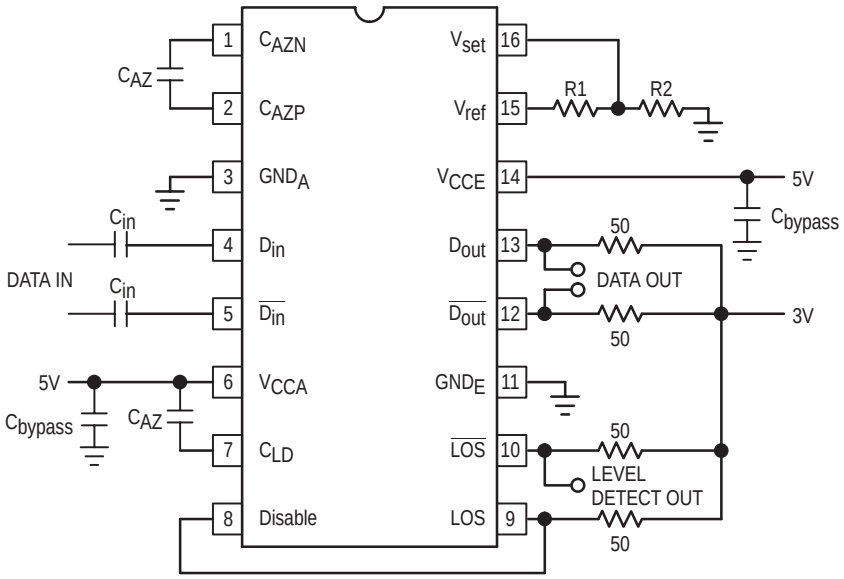


Figure 1. Typical Operating Circuit

Coupling Capacitors

The SX1125A inputs must be AC coupled to allow proper operation of the offset correction function. The coupling capacitors, C_{in}, must be large enough to pass the lowest input frequency of interest.

$$C_{in} = \frac{1}{2\pi\ (R_{in})\ (f_{low})}$$

where R_{in} = input resistance = 5000Ω
f_{low} = lowest frequency.

Auto–zero Capacitors

A feedback amplifier is used to cancel the offset voltage of the forward signal path, so the input to the internal ECL comparator is at its toggle point in the absence of any input signal. The time constant of the cancelling circuitry is set by an external capacitor (C_{AZ}) connected between Pins 1 and 2. The formula for the calculation of the auto–zero capacitor is:

$$C_{AZ} = \frac{150}{2\pi\ (R_{AZ})\ (f_{low})}$$

where R_{AZ} = internal driving impedance = 290kΩ
f_{low} = lowest frequency.

Input Signal Level Detector

The SX1125A allows for user programmable input signal level–detection and can automatically disable the switching of its ECL data output if the input level is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and ensures that data will only be transmitted when the signal–to–noise ratio is sufficient for low bit–error–rate system operation. Complimentary ECL flags (LOS and LOSB) indicate whether the input signal is above or below the desired threshold level. In the level detect system, the input signal is amplified and rectified before being compared to a programmable reference. A filter is included to prevent noise spikes from triggering the level–detector. The filter has a nominal 1μs time constant, and additional filtering can be achieved by using an external capacitor (C_{LD}) from Pin 7 to V_{CCA} (the internal driving impedance is nominally 28k). The formula for the calculation of the C_{LD} capacitor is:

$$C_{LD} = \frac{t}{R_Z}$$

where R_Z = internal driving impedance = 28kΩ
t = LOS filter time constant.

DC CHARACTERISTICS (GND_A = GND_E = Ground; V_{CCA} = V_{CCE} = 4.5V to 5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IN}	Input Signal Voltage (D_{in}) Single-Ended	0.008		1.5	V_{P-P}	Note 1.
V_{OS}	Input Offset Voltage			50	μV	
V_N	Input RMS Noise			225	μV	
V_{TH}	Input Level Detect Programmability	8.0		20	mV_{P-P}	
V_{HYS}	Level Detect Hysteresis	1.5	2.5	7.0	dB	Note 2.
I_{IH}	Input HIGH Current Disable			150	μA	
I_{CC}	Power Supply Current		33	45	mA	

1. This device functions with V_{in}min = 6mV_{P-P}, but with increased BER (See BER data).
2. This device has an anomoly in V_{HYS} when 0.65 < V_{SET} < 0.75V. Operation in this region is not recommended.

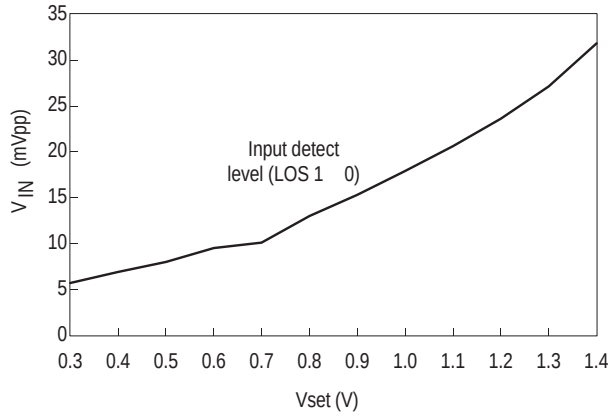


Figure 2. LOS versus Vset (T_A = 25°C)

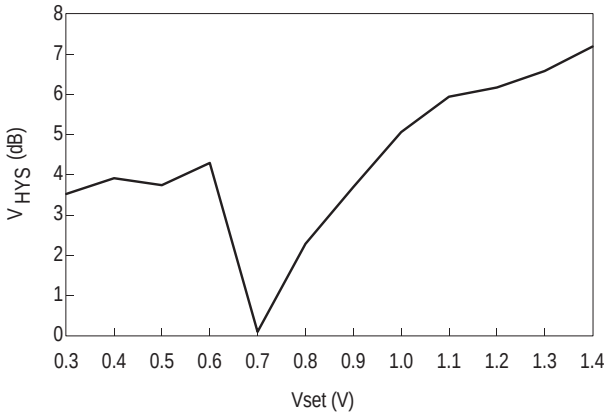


Figure 3. LOS Hysteresis (T_A = 25°C)

I/O DC CHARACTERISTICS[1]

Symbol	Characteristic	–40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage									mV
	V_{CC} = –4.5 to –5.5V	1080	–890	1020	–840	–980	–810	–910	–720	
	V_{CC} = 5.0V[2]	3920	4110	3980	4160	4020	4190	4090	4280	
V_{OL}	Output LOW Voltage									mV
	V_{CC} = –4.5 to –5.5V	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	
	V_{CC} = 5.0V[2]	3050	3350	3050	3370	3050	3370	3050	3405	
V_{IH}	Input HIGH Voltage[3]									mV
	V_{CC} = –4.5 to –5.5V	–1230	–890	–1170	–840	–1130	–810	–1060	–720	
	V_{CC} = 5.0V[2]	3770	4110	3830	4160	3870	4190	3940	4280	
V_{IL}	Input LOW Voltage[3]									mV
	V_{CC} = –4.5 to –5.5V	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	
	V_{CC} = 5.0V[2]	3050	3500	3050	3520	3050	3520	3050	3555	
I_{IL}	Input LOW Current[3]	0.5		0.5		0.5		0.3		μA

1. 10SX circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts except where otherwise specified on the individual data sheets.
2. Limits hold for V_{CC} = 5.0V only. Parametric values will vary 1:1 with any variation of V_{CC}.
3. Parametric values for the Disable input only.

AC CHARACTERISTICS (V_{CCA} = V_{CCE} = 4.5V to 5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
BW_{min}	Lower –3dB Bandwidth			20	kHz	
BW_{max}	Upper –3dB Bandwidth	550			MHz	
t_{PWD}	Pulse Width Distortion			70	ps	
t_r, t_f	Rise/Fall Times	150	250	650	ps	20% – 80%
R_{AZ}	Auto-Zero Output Resistance	200	325	450	kΩ	
R_F	Level Detect Filter Resistance	14	25	41	kΩ	
t_{LD}	Level Detect Time Constant	0.5		4.0	μs	

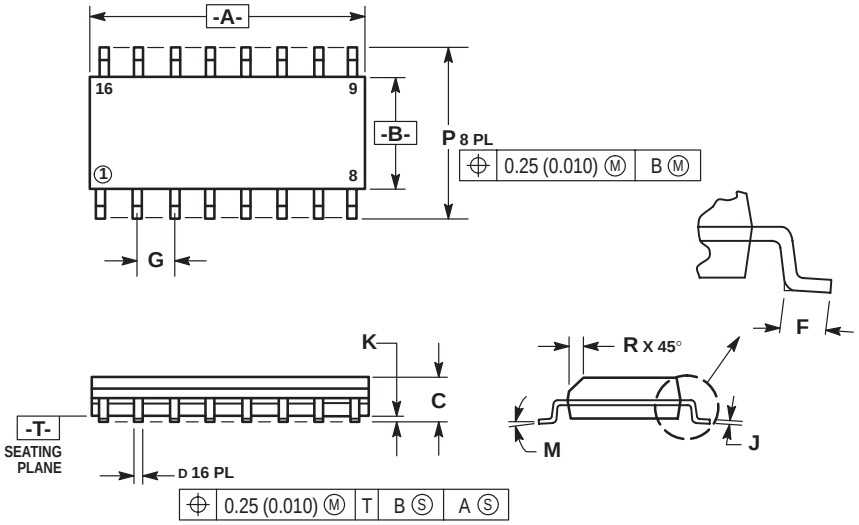
BER (Bit–Error–Rate)

Using a 622Mb/s SONET STS–12 pattern, the SX1125A shows the following typical BERs at T_A = 25°C:

Input V_{pp}	BER
6mV	4E–13
7mV	<1E–14
8mV	<5E–15

PACKAGE DIMENSIONS

SO–16
D SUFFIX
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Notes

Notes

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