MC10LVEP11

Product Preview

Low Voltage 1:2 Differential Fanout Buffer

The MC10LVEP11 is a differential 1:2 fanout buffer. The device is pin and functionally equivalent to the EP11 device. With AC performance the same as the EP11 device, the LVEP11 is ideal for applications requiring lower voltage.

- 220ps Typical Propagation Delay
- High Bandwidth to 3 GHz Typical
- PECL mode: 2.375V to 3.8V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –2.375V to –3.8V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Outputs will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 73 devices

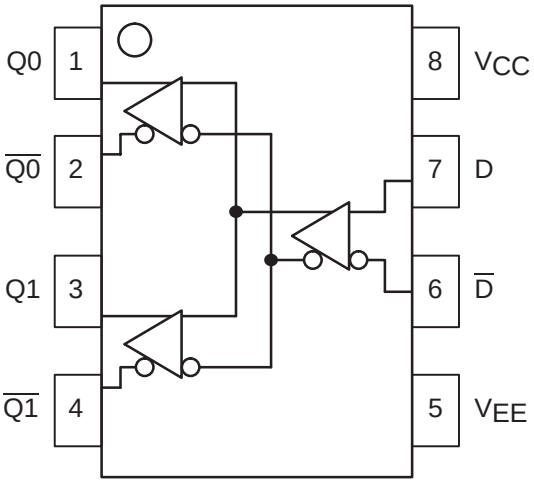

Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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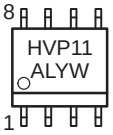
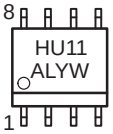
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D, $\overline{D}$	ECL Data Inputs
Q0, $\overline{Q0}$, Q1, $\overline{Q1}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

ORDERING INFORMATION

Device	Package	Shipping
MC10LVEP11D	SO–8	98 Units / Rail
MC10LVEP11DR2	SO–8	2500 / Reel
MC10LVEP11DT	TSSOP–8	98 Units / Rail
MC10LVEP11DTR2	TSSOP–8	2500 / Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (8–Pin SOIC) — Still Air 500lfpm	190 130	°C/W
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (8–Pin TSSOP) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –3.8V to –2.375V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	20	29	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current — D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 5.)	20	29	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 2.5V ± 0.125V, V_{EE} = 0V) (Note 12.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 9.)	20	29	37	20	30	39	22	31	40	mA
V_{OH}	Output HIGH Voltage (Note 10.)	1365	1440	1615	1430	1555	1680	1490	1615	1740	mV
V_{OL}	Output LOW Voltage (Note 10.)	565	690	815	630	755	880	690	815	940	mV
V_{IH}	Input HIGH Voltage Single Ended	1290		1615	1355		1680	1415		1740	mV
V_{IL}	Input LOW Voltage Single Ended	565		890	630		955	690		1015	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 2.5V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

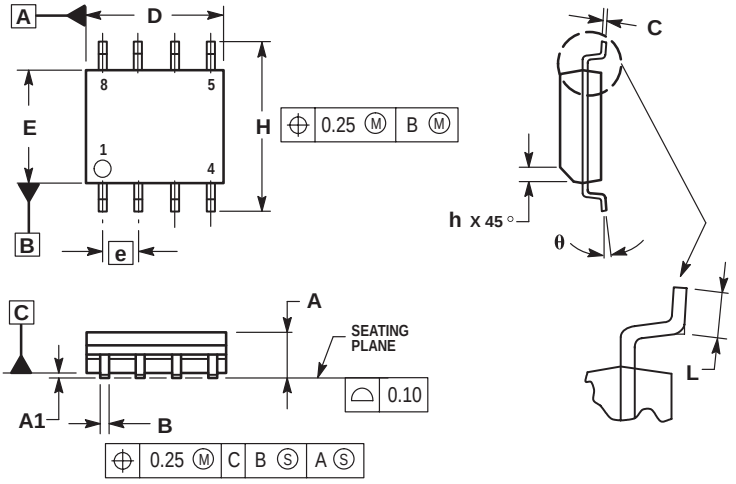
AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –2.375V to –3.8V) or (V_{CC} = 2.375V to 3.8V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)		3.0			3.0			3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay (Diff.) CLK–>Q, $\overline{Q}$	140	200	270	160	220	300	180	240	320	ps
t_{SKEW}	Device Skew Q, $\overline{Q}$ Part–to–Part (Note 14.)		TBD TBD			TBD TBD			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$	50	110	180	60	120	200	70	140	220	ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions.

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T

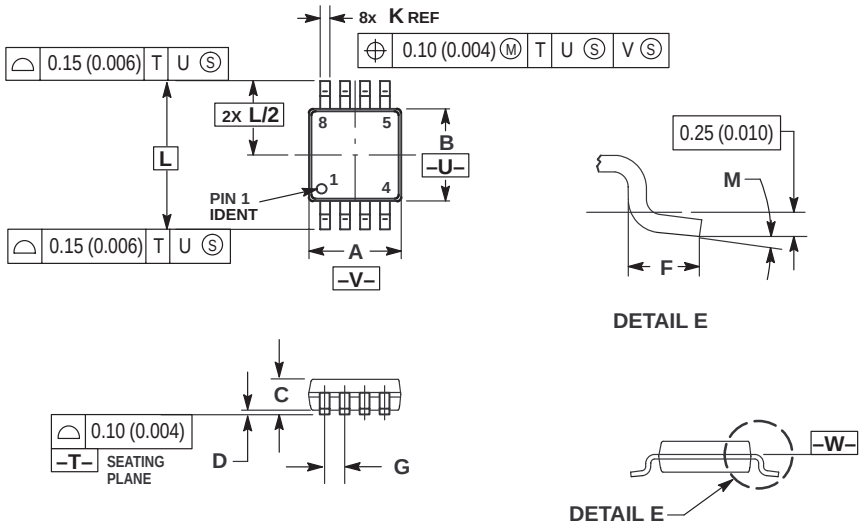


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

PACKAGE DIMENSIONS

TSSOP–8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

Notes

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