

Hex ECL/TTL Transceiver
with Latches

The MC10/100H681 is a dual supply Hex ECL/TTL transceiver with latches in both directions. ECL controlled Direction and Chip Enable Bar pins. There are two Latch Enable pins, one for each direction.

The ECL outputs are single ended and drive 50 Ω. The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads. The high driving ability of the TTL outputs make the device ideal for bussing applications.

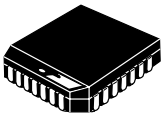
The ECL output levels are standard V_{OH} and V_{OL} cutoff equal to -2.0 V (V_{TT}). When the ECL ports are disabled the outputs go to the V_{OL} cutoff level. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

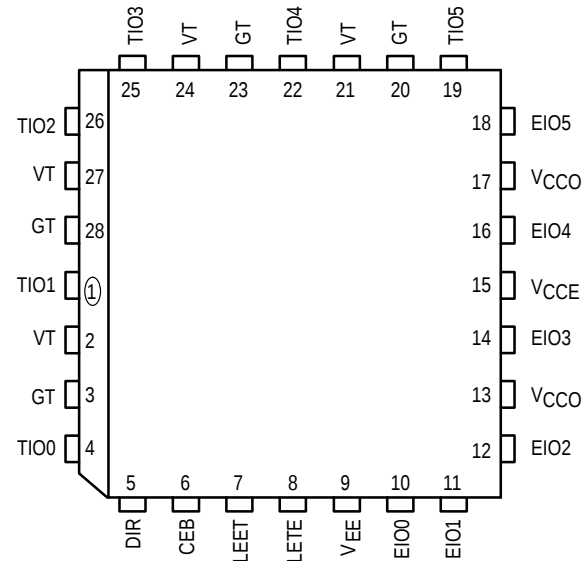
- Separate Latch Enable Controls for each Direction
- ECL Single Ended 50 Ω I/O Port
- High Drive TTL I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins

MC10H681
MC100H681



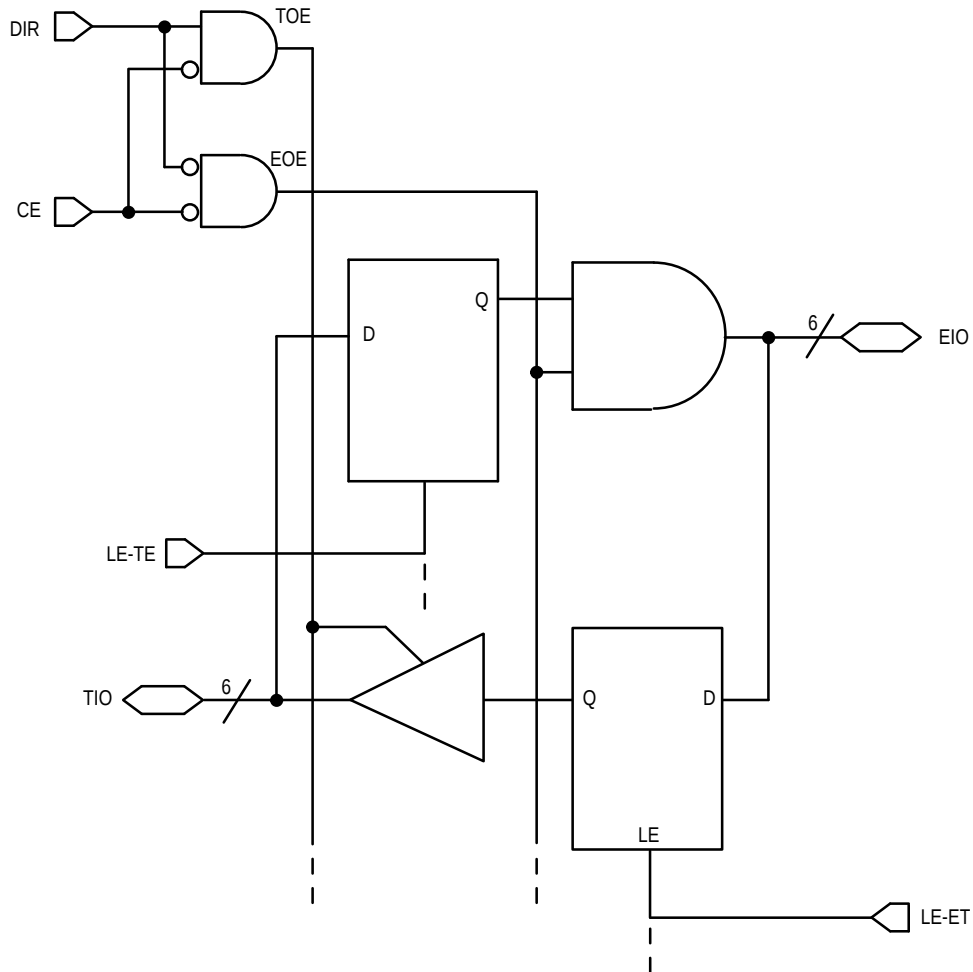
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



Pin	Symbol	Description
1	TIO1	TTL I/O BIT 1
2	VT	TTL V_{CC} (5.0 V)
3	GT	TTL GND (0 V)
4	TIO0	TTL I/O Bit 0
5	DIR	Direction Control (ECL)
6	CEB	Chip Enable Bar Control (ECL)
7	LEET	Latch Enable ECL-TTL Control (ECL)
8	LETE	Latch Enable TTL-ECL Control (ECL)
9	V_{EE}	ECL Supply ($-5.2/-4.5\text{ V}$)
10	EIO0	ECL I/O BIT 0
11	EIO1	ECL I/O BIT 1
12	EIO2	ECL I/O BIT 2
13	V_{CCO}	ECL V_{CC} (0 V) — Outputs
14	EIO3	TTL I/O BIT 3
15	V_{CCE}	ECL V_{CC} (0 V)
16	EIO4	ECL I/O BIT 4
17	V_{CCO}	ECL V_{CC} (0 V) — Outputs
18	EIO5	ECL I/O BIT 5
19	TIO5	TTL I/O BIT 5
20	GT	TTL GND (0 V)
21	VT	TTL V_{CC} (5.0 V)
22	TIO4	TTL I/O BIT 4
23	GT	TTL GND (0 V)
24	VT	TTL V_{CC} (5.0 V)
25	TIO3	TTL I/O BIT 3
26	TIO2	TTL I/O BIT 2
27	VT	TTL V_{CC} (5.0 V)
28	GT	TTL V_{CC} (0 V)





TRUTH TABLE

CEB	DIR	LEET	LETE	EOUT	TOUT
H	X	X	X	Z	Z
L	H	L	L	Z	EIN
L	H	H	L	Z	Q ₀
L	L	L	L	TIN	Z
L	L	L	H	Q ₀	Z

- Hex
- Bi-Directional
- ECL/TTL Translation
- Dual Supply
- ECL Outputs, 50 Ohm S.E., V_{OH}/Cutoff
- TTL Outputs, 48 mA Sink, 15 mA Source
- Multi Power and Ground Pins
- Separate LE Controls

ECL DC CHARACTERISTICS: $V_{CCT} = +5.0\text{ V} \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$ (10H Version); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H Version)

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Supply Current/ECL	—	-113	—	-113	—	-113	mA	
I_{INH}	Input HIGH Current	—	225	—	145	—	145	μA	
I_{INL}	Input LOW Current	0.5	—	0.5	—	0.3	—	μA	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	-1020 -2.1	-840 -2.03	-980 -2.1	-810 -2.03	-920 -2.1	-735 -2.03	mV V	50 Ω to -2.1 V

10H ECL DC CHARACTERISTICS: $V_{CCT} = +5.0 \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1070 -1950	-735 -1450	mV	

100H ECL DC CHARACTERISTICS: $V_{CCT} = +5.0 \pm 10\%$, $V_{EE} = -4.2\text{ V}$ to -5.5 V

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV	

ABSOLUTE RATINGS (Do not exceed):

Power Supply Voltage	V_{EE} (ECL)	-8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	-0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} -0.5 to +7.0	Vdc
Disabled 3-State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mA _{dc}
Output Source Current Surge	I_{out} (ECL)	200	mA _{dc}
Storage Temperature	T_{stg}	-65 to 150	$^\circ\text{C}$
Operating Temperature	T_{amb}	0.0 to +75	$^\circ\text{C}$

TTL DC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V} \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$ (10H Version); $V_{EE} = -4.2 \text{ V}$ to -5.5 V (100H Version)

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Standard Input Standard Input	2.0 —	— 0.8	2.0 —	— 0.8	2.0 —	— 0.8	Vdc	
V_{IK}	Input Clamp	—	-1.2	—	-1.2	—	-1.2	Vdc	$I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	$I_{OH} = -3.0 \text{ mA}$ $I_{OH} = -15 \text{ mA}$
V_{OL}	Output LOW Voltage	—	0.55	—	0.55	—	0.55	V	$I_{OL} = 48 \text{ mA}$
I_{IH}/I_{OZH} I_{IL}/I_{OZL}	Output Disable Current	— —	70 200	— —	70 200	— —	70 200	μA	$V_{OUT} = 2.7 \text{ V}$ $V_{OUT} = 0.5 \text{ V}$
I_{CCL}	Supply Current	—	63	—	63	—	63	mA	
I_{CCH}	Supply Current	—	63	—	63	—	63	mA	
I_{CCZ}	Supply Current	—	63	—	63	—	63	mA	
I_{OS}	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	$V_{OUT} = 0 \text{ V}$

ECL TO TTL DIRECTION AC CHARACTERISTICS

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	4.0	7.8	4.0	7.8	4.2	8.0	ns	$C_L = 50 \text{ pF}$
t_{PLH} t_{PHL}	LEET to Output	5.5 5.5	8.3 7.6	5.5 5.5	8.3 7.6	5.7 5.8	8.5 8.0	ns	$C_L = 50 \text{ pF}$
t_{PZH} t_{PZL}	CEB to Output Enable Time	5.5 5.3	8.3 8.3	5.5 5.3	8.3 8.3	4.7 5.4	8.5 8.4	ns	$C_L = 50 \text{ pF}$
t_{PHZ} t_{PLZ}	CEB to Output Disable Time	3.5 3.5	7.2 5.3	3.5 3.5	7.2 5.3	3.7 4.1	7.3 5.8	ns	$C_L = 50 \text{ pF}$
t_r/t_f	1.0 Vdc to 2.0 Vdc	0.4	2.2	0.4	2.2	0.4	2.2	ns	$C_L = 50 \text{ pF}$

TTL TO ECL DIRECTION AC CHARACTERISTICS

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	1.9	3.9	1.9	3.9	2.2	4.4	ns	50 Ω to -2.0 V
t_{PHL} t_{PLH}	CEB to Output	2.2 2.3	4.0 4.6	2.2 2.3	4.0 4.6	2.5 2.7	4.3 5.0	ns	50 Ω to -2.0 V
t_{PHL} t_{PLH}	LETE to Output	2.4	3.9	2.4	3.9	2.7	4.3	ns	50 Ω to -2.0 V
t_r/t_f	Output Rise/Fall Time 20%–80%	0.4	2.2	0.4	2.2	0.4	2.2	ns	50 Ω to -2.0 V

TEST CIRCUITS AND WAVEFORMS

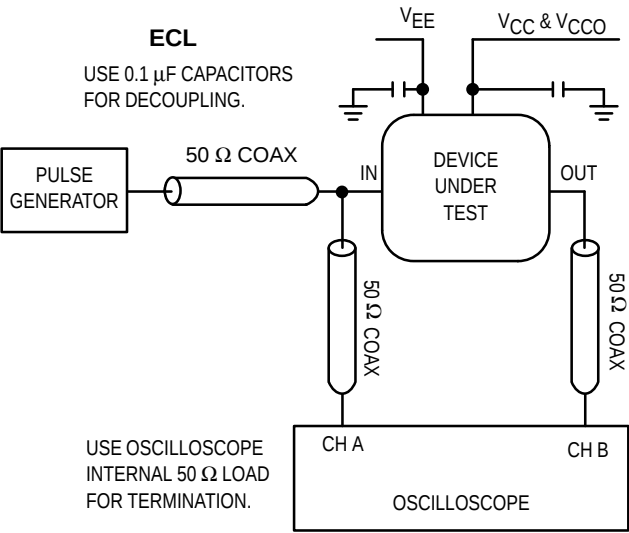


Figure 1. Test Circuit ECL

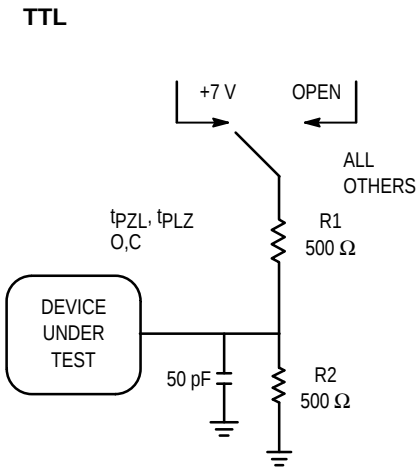


Figure 2. Test Circuit TTL

ECL/TTL

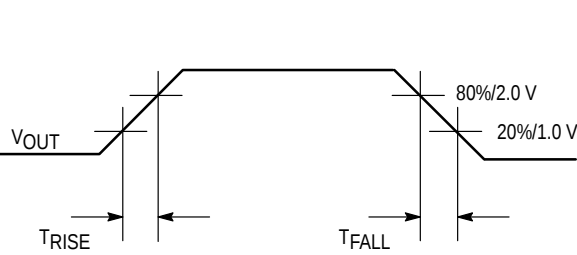


Figure 3. Rise and Fall Times

ECL/TTL

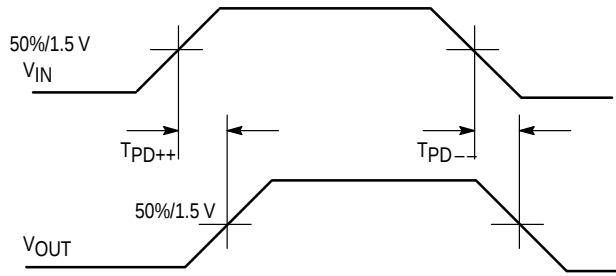


Figure 4. Propagation Delay — Single Ended

TTL

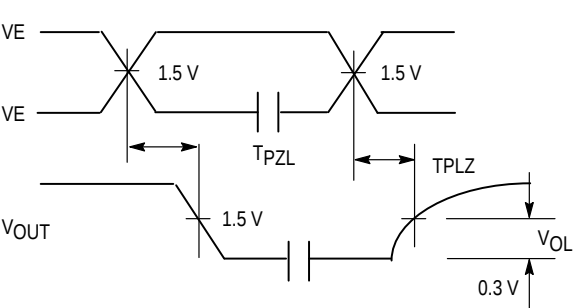


Figure 5. 3-State Output Low Enable and Disable Times

TTL

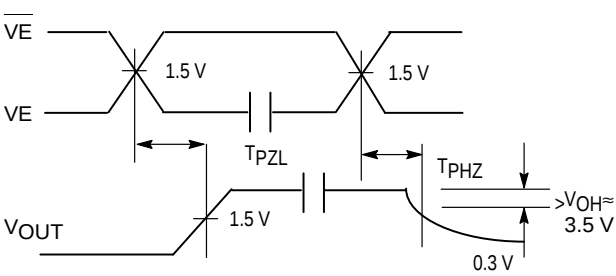


Figure 6. 3-State Output High Enable and Disable Times

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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

