PECL/TTL-TTL 1:8 Clock Distribution Chip

The MC10H/100H646 is a single supply, low skew translating 1:8 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance. The single supply H646 is similar to the H643, which is a dual supply 1:8 version of the same function.

- PECL/TTL–TTL Version of Popular ECLinPS™ E111
- Low Skew
- Guaranteed Skew Spec
- Tri–State Enable
- Differential Internal Design
- V_{BB} Output
- Single Supply
- Extra TTL and ECL Power/Ground Pins
- Matched High and Low Output Impedance
- Meets Specifications Required to Drive the Pentium™ Microprocessor

The H646 was designed specifically to drive series terminated transmission lines. Special techniques were used to match the HIGH and LOW output impedances to about 7ohms. This simplifies the choice of the termination resistor for series terminated applications. To match the HIGH and LOW output impedances, it was necessary to remove the standard IOS limiting resistor. As a result, the user should take care in preventing an output short to ground as the part will be permanently damaged.



MC10H646

MC100H646

The H646 device meets all of the requirements for driving the 60 and 66MHz Pentium Microprocessor. The device has no PLL components, which greatly simplifies its implementation into a digital design. The eight copies of the clock allows for point-to-point clock distribution to simplify board layout and optimize signal integrity.

The H646 provides differential PECL inputs for picking up LOW skew PECL clocks from the backplane and distributing it to TTL loads on a daughter board. When used in conjunction with the MC10/100E111, very low skew, very wide clock trees can be designed. In addition, a TTL level clock input is provided for flexibility. Note that only one of the inputs can be used on a single chip. For correct operation, the unused input pins should be left open.

The Output Enable pin forces the outputs into a high impedance state when a logic 0 is applied.

The output buffers of the H646 can drive two series terminated, 50Ω transmission lines each. This capability allows the H646 to drive up to 16 different point–to–point clock loads. Refer to the Applications section for a more detailed discussion in this area.

The 10H version is compatible with MECL 10H[™] ECL logic levels. The 100H version is compatible with 100K levels.

MECL 10H and ECLinPS are trademarks of Motorola, Inc. Pentium is a trademark of Intel Corporation.





TRUTH TABL	TRUTH TABLE											
TCLK	ECLK	ECLK	EN	Q								
GND	L	Н	Н	L								
GND	Н	L	Н	Н								
н	GND	GND	Н	Н								
L	GND	GND	Н	L								
Х	Х	Х	L	Z								

L = Low Voltage Level; H = High Voltage Level; Z = Tristate

DC CHARACTERISTICS (IVT = OVT = VCCE = $5.0V \pm 5\%$)

		0°C		25°C		85	°C		
Symbol	Characteristic	Min	Мах	Min	Max	Min	Max	Unit	Condition
VOH	Output HIGH Voltage	2.6	-	2.6	-	2.6		V	I _{OH} = 24mA
V _{OL}	Output LOW Voltage	-	0.5	-	0.5	-	0.5	V	I _{OL} = 48mA
IOS	Output Short Circuit Current	-	-	-	-	-	-	mA	See Note 1

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

TTL DC CHARACTERISTICS (VT = VE = $5.0 \text{ V} \pm 5\%$)

		0°C		25°C		85°C			
Symbol	Characteristic	Min	Мах	Min	Max	Min	Max	Unit	Condition
V _{IH} V _{IL}	Input HIGH Voltage Input LOW Voltage	2.0	0.8	2.0	0.8	2.0	0.8	V	
lн	Input HIGH Current		20 100		20 100		20 100	μA	V _{IN} = 2.7 V V _{IN} = 7.0 V
۱ _{IL}	Input LOW Current		-0.6		-0.6		-0.6	mA	V _{IN} = 0.5 V
VOH	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I _{OH} = -3.0 mA I _{OH} = -24 mA
VOL	Output LOW Voltage		0.5		0.5		0.5	V	I _{OL} = 24 mA
VIK	Input Clamp Voltage		-1.2		-1.2		-1.2	V	I _{IN} = -18 mA
IOS	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	V _{OUT} = 0 V

10H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = $5.0V \pm 5\%$)

		0°C			25°C				85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Notes
Чн	Input HIGH Current			225			175			175	μΑ	
۱ _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ	
VIH	Input HIGH Voltage	3.83		4.16	3.87		4.19	3.94		4.28	V	IVT = IVO = VCCE = 5.0V (1)
VIL	Input LOW Voltage	3.05		3.52	3.05		3.52	3.05		3.555	V	IVT = IVO = VCCE = 5.0V (1)
V _{BB}	Output Reference Voltage	3.62		3.73	3.65		3.75	3.69		3.81	V	IVT = IVO = VCCE = 5.0V (1)

100H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = $5.0V \pm 5\%$)

		0°C			25°C				85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Notes
Чн	Input HIGH Current			225			175			175	μΑ	
۱ _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ	
VIH	Input HIGH Voltage	3.835		4.12	3.835		4.12	3.835		3.835	V	IVT = IVO = VCCE = 5.0V (1)
VIL	Input LOW Voltage	3.19		3.525	3.19		3.525	3.19		3.525	V	IVT = IVO = VCCE = 5.0V (1)
V _{BB}	Output Reference Voltage	3.62		3.74	3.62		3.74	3.62		3.74	V	IVT = IVO = VCCE = 5.0V (1)

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to VCCE and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = VCCE = 5.0V

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

		0°C		25°C			85	°C		
Symbol	Characteristic	Min	Мах	Min	Тур	Max	Min	Мах	Unit	Condition
ICCL	Power Supply Current		185		166	185		185	mA	Total all OVT, IVT,
ІССН			175		154	175		175	mA	and VCCE pins
ICCZ			210			210		210		

AC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

			0 °	C	25	°C	85	°C		
Symbol	Characte	Characteristic			Min	Max	Min	Max	Unit	Condition
^t PLH	Propagation Delay	ECLK to Q TCLK to Q	4.8 5.1	5.8 6.4	5.0 5.3	6.0 6.4	5.6 5.7	6.6 7.0	ns	
^t PHL	Propagation Delay	ECLK to Q TCLK to Q	4.4 4.7	5.4 6.0	4.4 4.8	5.4 5.9	4.8 5.2	5.8 6.5	ns	
^t SK(O)	Output Skew	Q0, Q3, Q4, Q7 Q1, Q2, Q5 Q0–Q7		350 350 500		350 350 500		350 350 500	ps	Note 1, 6
^t SK(PR)	Process Skew	ECLK to Q TCLK to Q		1.0 1.3		1.0 1.1		1.0 1.3	ns	Note 2, 6
^t SK(P)	Pulse Skew	$\Delta t_{PLH} - t_{PHL}$		1.0		1.0		1.0	ns	
t _r , t _f	Rise/Fall Time		0.3	1.5	0.3	1.5	0.3	1.5	ns	
tpw	Output Pulse Width	66MHz @ 2.0V 66MHz @ 0.8V 60MHz @ 2.0V 60MHz @ 0.8V	5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		ns	Note 3, 6
^t Stability	Clock Stability			±75		±75		±75	ps	Note 4, 6
FMAX	Maximum Input Frequ	ency		80		80		80	MHz	Note 5, 6

Output skew defined for identical output transitions.
Process skew is valid for V_{CC} = 5.0V ±5%.
Parameters guaranteed by t_{SK}(P) and t_r, t_f specification limits.
Clock stability is the period variation between two successive rising edges.
For series terminated lines. See Applications section for F_{MAX} enhancement techniques.
All AC specifications tested driving 50Ω series terminated transmission lines at 80MHz.



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