

# 68030/040 PECL-TTL Clock Driver

The MC10H/100H640 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part-to-part skew, within-part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H640 also uses differential PECL internally to achieve its superior skew characteristic.

The H640 includes divide-by-two and divide-by-four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0V Supply

### Function

*Reset (R):* LOW on RESET forces all Q outputs LOW and all  $\bar{Q}$  outputs HIGH.

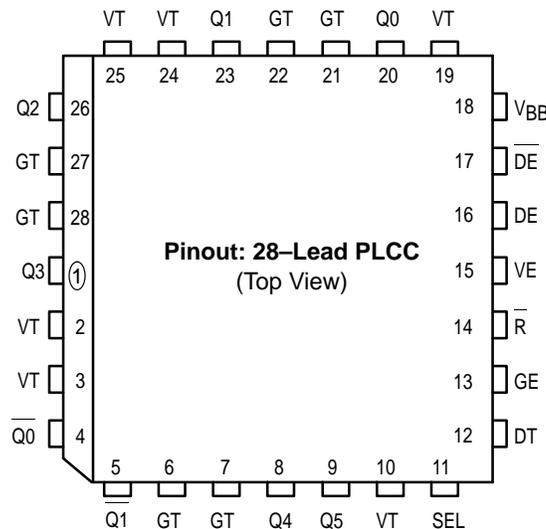
*Power-Up:* The device is designed to have the POS edges of the +2 and +4 outputs synchronized at power up.

*Select (SEL):* LOW selects the ECL input source (DE/DE). HIGH selects the TTL input source (DT).

The H640 also contains circuitry to force a stable state of the ECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and DE goes HIGH.

**MC10H640**  
**MC100H640**

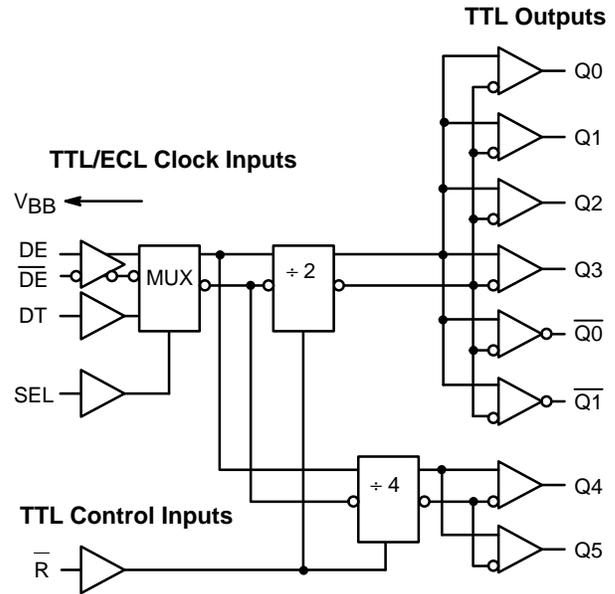
**68030/040**  
**PECL-TTL CLOCK**  
**DRIVER**



LOGIC DIAGRAM

PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V <sub>CC</sub> (+5.0 V)
VE	ECL V <sub>CC</sub> (+5.0 V)
GE	ECL Ground (0 V)
DE, $\overline{DE}$	ECL Signal Input (positive ECL)
V <sub>BB</sub>	V <sub>BB</sub> Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
R	Reset (TTL)



AC CHARACTERISTICS (V<sub>T</sub> = V<sub>E</sub> = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay ECL D to Output	Q0-Q3	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t <sub>PLH</sub>	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
tskwd*	Within-Device Skew			0.5		0.5		0.5	ns	CL = 25pF
t <sub>PLH</sub>	Propagation Delay ECL D to Output	Q0, Q1	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t <sub>PLH</sub>	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t <sub>PLH</sub>	Propagation Delay ECL D to Output	Q4, Q5	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t <sub>PLH</sub>	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t <sub>PD</sub>	Propagation Delay R to Output	All Outputs	4.3	6.3	4.3	6.3	5.0	7.0	ns	CL = 25pF
t <sub>R</sub> t <sub>F</sub>	Output Rise/Fall Time 0.8 V – 2.0 V	All Outputs		2.5 2.5		2.5 2.5		2.5 2.5	ns	CL = 25pF
f <sub>max</sub>	Maximum Input Frequency		135		135		135		MHz	CL = 25pF
t <sub>pw</sub>	Minimum Pulse Width		1.50		1.50		1.50		ns	
t <sub>rr</sub>	Reset Recovery Time		1.25		1.25		1.25		ns	

\* Within-Device Skew defined as identical transitions on similar paths through a device.

**V<sub>CC</sub> and CLOAD RANGES TO MEET DUTY CYCLE REQUIREMENTS** ( $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  Output Duty Cycle Measured Relative to 1.5V)

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
	Range of V <sub>CC</sub> and CL to meet minimum pulse width (HIGH or LOW) = 11.5 ns at f <sub>out</sub> ≤ 40 MHz	V <sub>CC</sub> CL	4.75 10	5.0	5.25 50	V pF	Q0–Q3 Q0–Q1
	Range of V <sub>CC</sub> and CL to meet minimum pulse width (HIGH or LOW) = 9.5 ns at 40 < f <sub>out</sub> ≤ 50 MHz	V <sub>CC</sub> CL	4.875 15	5.0	5.125 27	V pF	Q0–Q3

**DC CHARACTERISTICS** (V<sub>T</sub> = V<sub>E</sub> = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition	
		Min	Max	Min	Max	Min	Max			
I <sub>EE</sub>	Power Supply Current	ECL		57		57		57	mA	VE Pin
I <sub>CCH</sub>		TTL		30		30		30	mA	Total all VT pins
I <sub>CCL</sub>				30		30		30	mA	

**TTL DC CHARACTERISTICS** (V<sub>T</sub> = V<sub>E</sub> = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V <sub>IH</sub> V <sub>IL</sub>	Input HIGH Voltage Input LOW Voltage	2.0	0.8	2.0	0.8	2.0	0.8	V	
I <sub>IH</sub>	Input HIGH Current		20 100		20 100		20 100	μA	V <sub>IN</sub> = 2.7V V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current		–0.6		–0.6		–0.6	mA	V <sub>IN</sub> = 0.5V
V <sub>OH</sub>	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I <sub>OH</sub> = –3.0mA I <sub>OH</sub> = –15mA
V <sub>OL</sub>	Output LOW Voltage		0.5		0.5		0.5	V	I <sub>OL</sub> = 24mA
V <sub>IK</sub>	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I <sub>IN</sub> = –18mA
I <sub>OS</sub>	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V <sub>OUT</sub> = 0V

# MC10H640 MC100H640

## 10H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I <sub>IH</sub> I <sub>IL</sub>	Input HIGH Current Input LOW Current	0.5	225	0.5	175	0.5	175	μA	
V <sub>IH</sub> * V <sub>IL</sub> *	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	VE = 5.0V
V <sub>BB</sub> *	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

\*NOTE: PECL levels are referenced to V<sub>CC</sub> and will vary 1:1 with the power supply. The values shown are for V<sub>CC</sub> = 5.0V.

## 100H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

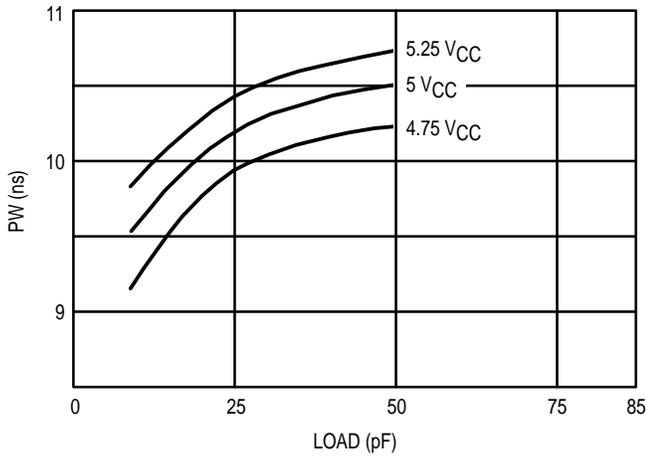
Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I <sub>IH</sub> I <sub>IL</sub>	Input HIGH Current Input LOW Current	0.5	225	0.5	175	0.5	175	μA	
V <sub>IH</sub> * V <sub>IL</sub> *	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	VE = 5.0V
V <sub>BB</sub> *	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	

\*NOTE: PECL levels are referenced to V<sub>CC</sub> and will vary 1:1 with the power supply. The values shown are for V<sub>CC</sub> = 5.0V.

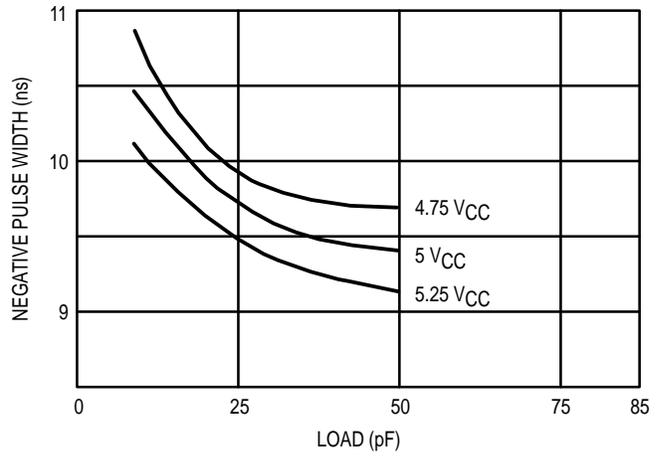
## 10/100H640 DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

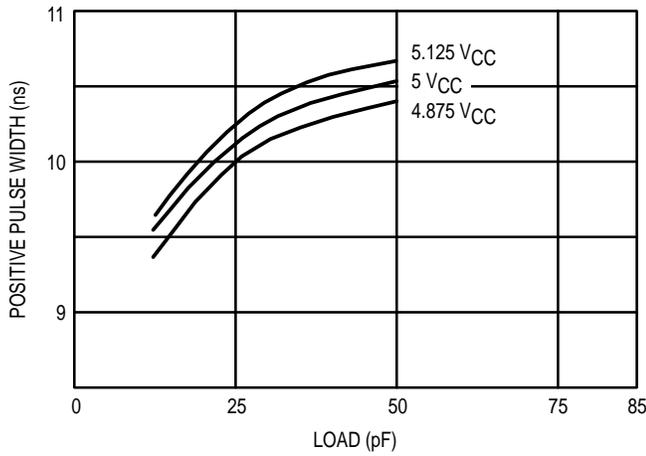
Best duty cycle control is obtained with a single μP load and minimum line length.



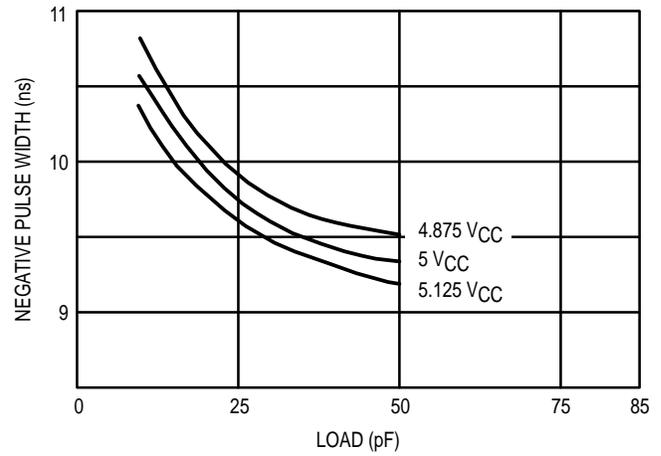
**Figure 1. Positive Pulse Width at 25°C Ambient and 50 MHz Out**



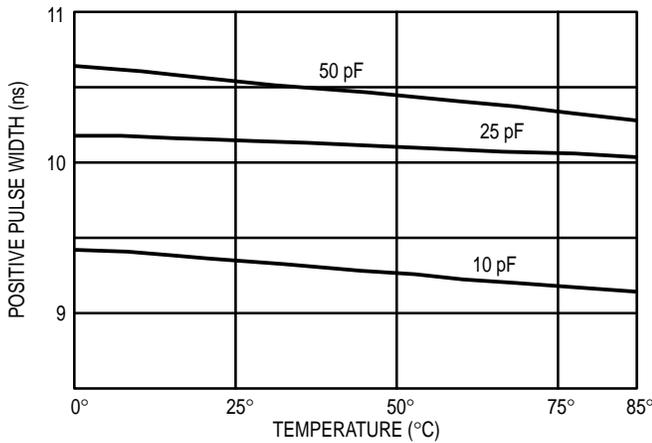
**Figure 2. Negative Pulse Width @ 50 MHz Out and 25°C Ambient**



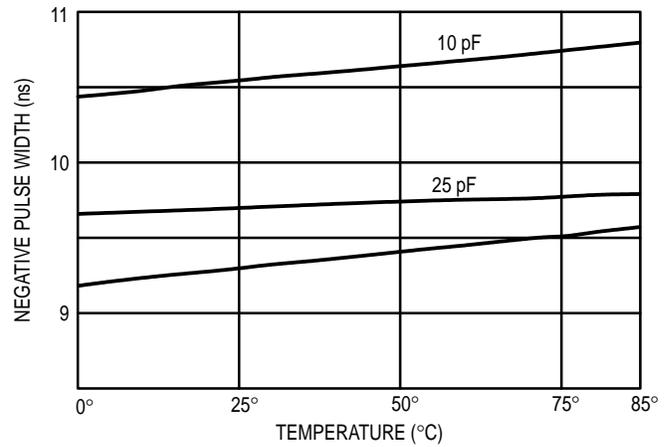
**Figure 3. Positive Pulse Width at 25°C Ambient at 50 MHz Out**



**Figure 4. Negative Pulse Width @ 50 MHz Out and 25°C Ambient**



**Figure 5. Temperature versus Positive Pulse Width for 100H640 at 50 MHz and +5.0 V V<sub>CC</sub>**



**Figure 6. Temperature versus Negative Pulse Width for MC100H640 @ 50 MHz and +5.0 V V<sub>CC</sub>**

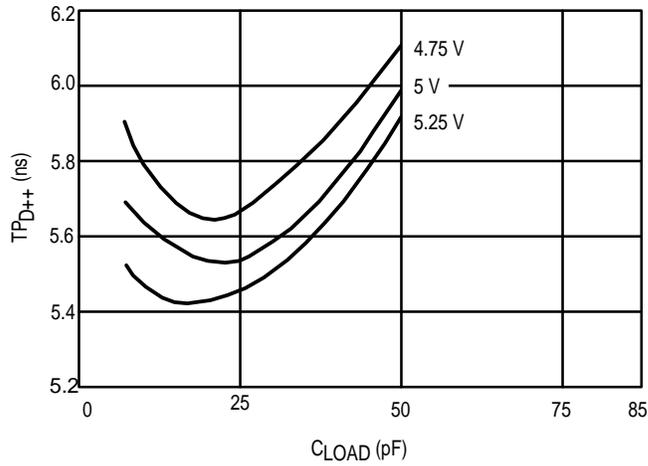


Figure 7. TP versus Load Typical at T<sub>A</sub> = 25°C

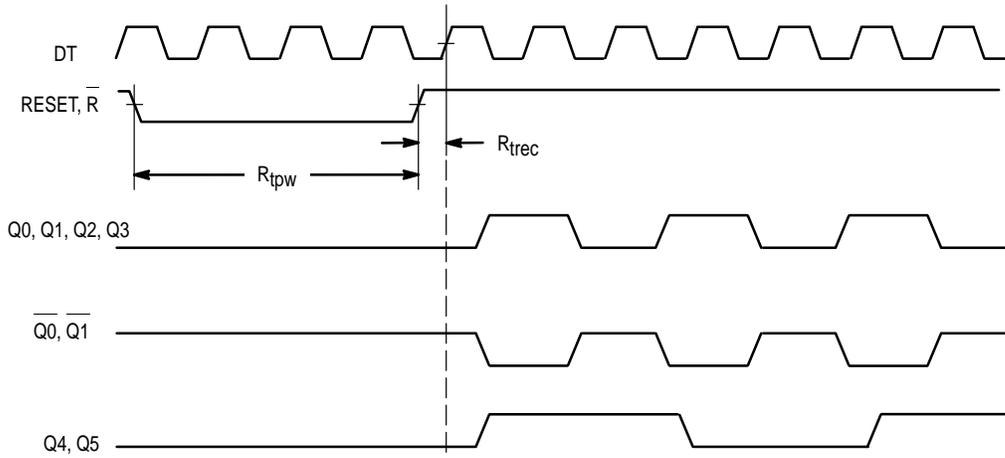
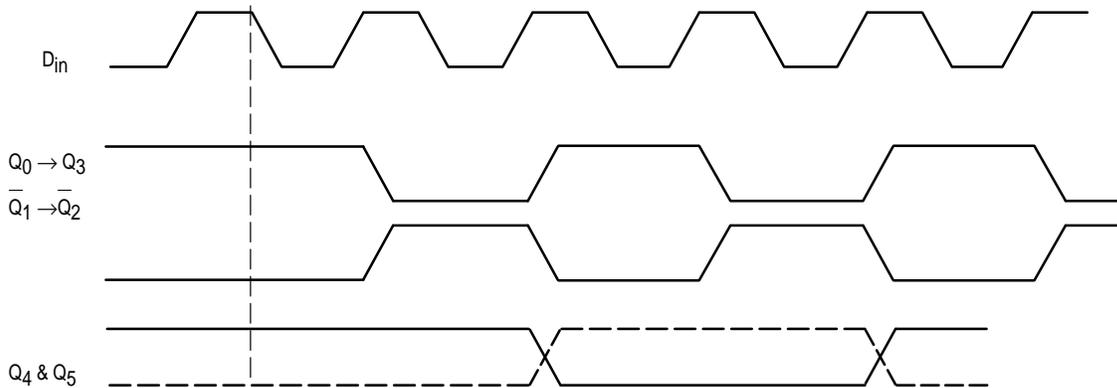


Figure 8. MC10H/100H640 Clock Phase and Reset Recovery Time After Reset Pulse

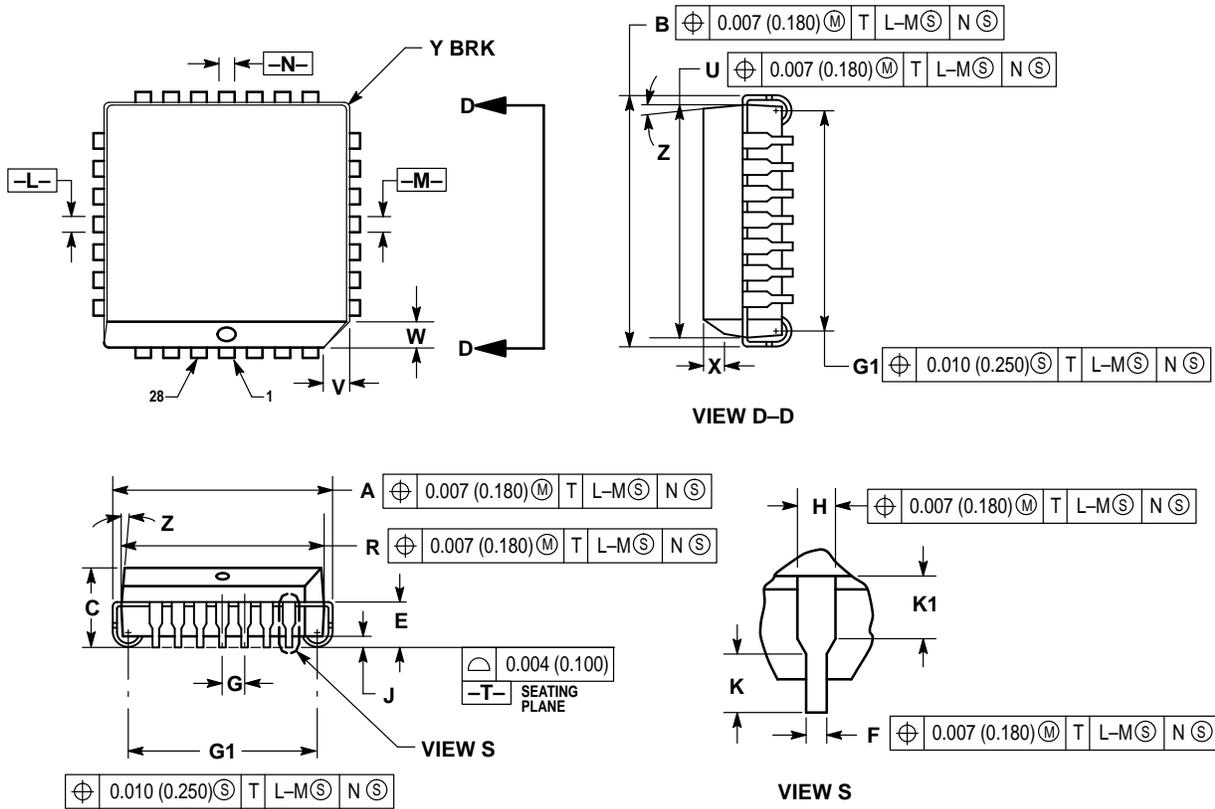


AFTER POWER UP  
 OUTPUTS Q<sub>4</sub> & Q<sub>5</sub> WILL SYN WITH POSITIVE EDGES OF D<sub>in</sub> & Q<sub>0</sub> → Q<sub>3</sub> & NEGATIVE EDGES OF Q<sub>0</sub><sup>-</sup> & Q<sub>1</sub><sup>-</sup>

Figure 9. Output Timing Diagram

OUTLINE DIMENSIONS

FN SUFFIX  
 PLASTIC PLCC PACKAGE  
 CASE 776-02  
 ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°		10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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