MC10H607, MC10H607

Registered Hex PECL to TTL Translator

The MC10H/100H607 is a 6–bit, registered PECL to TTL translator. The device features differential PECL inputs for both data and clock. The TTL outputs feature 48mA sink, 24mA source drive capability for driving high fanout loads or transmission lines. The asynchronous master reset control is an ECL level input.

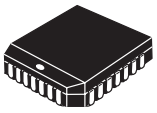
With its differential PECL inputs and TTL outputs the H607 device is ideally suited for the receive function of a HPPI bus type board–to–board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with MECL 10H™ logic levels, with a V_{CC} of +5.0 volts, while the 100H device is compatible with 100K logic levels, with a V_{CC} of +5.0 volts.

- Differential ECL Data and Clock Inputs
- 48mA Sink, 24mA Source TTL Outputs
- Single Power Supply
- Multiple Power and Ground Pins to Minimize Noise

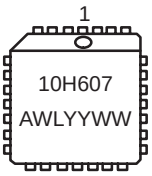
ON Semiconductor

http://onsemi.com



PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

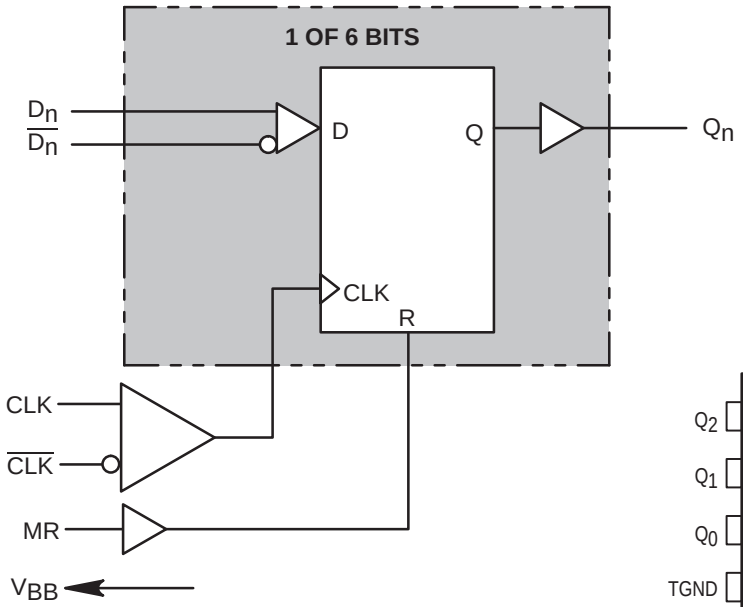


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

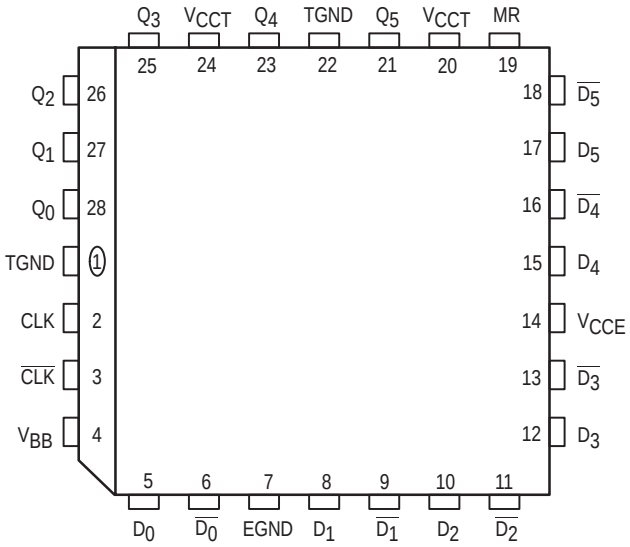
ORDERING INFORMATION

Device	Package	Shipping
MC10H607FN	PLCC–28	37 Units/Rail
MC100H607FN	PLCC–28	37 Units/Rail

LOGIC DIAGRAM



Pinout: 28–Lead PLCC (Top View)



PIN NAMES

Pin	Function
$D_0 - D_5$ $\overline{D_0} - \overline{D_5}$ CLK, $\overline{CLK}$ MR $Q_0 - Q_5$	True PECL Data Inputs Inverted PECL Data Inputs Differential PECL Clock Input PECL Master Reset Input TTL Outputs
V_{CCE} V_{CCT} TGND EGND	PECL V_{CC} TTL V_{CC} TTL Ground PECL Ground

TRUTH TABLE

D_n	MR	TCLK/CLK	$Q_n + 1$
L	L	Z	L
H	L	Z	H
X	H	X	L
Open Input	X	X	L

Z = LOW to HIGH Transition

DC CHARACTERISTICS ($V_{CCT} = V_{CCE} = 5.0V \pm 5\%$)

Symbol	Characteristic	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	ECL Power Supply Current 10H 100H		70 65	85 80		70 70	85 85		70 75	85 95	mA	
I_{CCL}	TTL Supply Current		100	120		100	120		100	120	mA	
I_{CCH}	TTL Supply Current		100	120		100	120		100	120	mA	

10H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH}	Input HIGH Current		255		145		145	μA	
I_{INL}	Input LOW Current		0.5		0.5		0.5	μA	
V_{IH}	Input HIGH Voltage	3830	4160	3870	4190	3930	4280	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage	3050	3520	3050	3520	3050	3555	mV	V_{CCT} = 5.0V
V_{BB}	Output Bias Voltage	3600	3710	3630	3730	3670	3790	mV	V_{CCT} = 5.0V

NOTE: PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CCT} = V_{CCE} = 5.0V and will vary 1:1 with power supply.

100H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Current		255		145		145	μA	
I_{IL}	Input LOW Current		0.5		0.5		0.5	μA	
V_{IH}	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	mV	V_{CCT} = 5.0V
V_{IL}	Input LOW Voltage	3190	3525	3190	3525	3190	3525	mV	V_{CCT} = 5.0V
V_{BB}	Output Bias Voltage	3600	3720	3600	3720	3600	3720	mV	V_{CCT} = 5.0V

NOTE: PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CCT} = V_{CCE} = 5.0V and will vary 1:1 with power supply.

10H/100H TTL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –15mA I_{OH} = –24mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48mA

NOTE: DC levels such as V_{OH}, V_{OL}, etc., are standard for PECL and FAST devices, with the exceptions of: I_{OL} = 48mA at 0.5V_{OL}; and I_{OH} = –24mA at 2.0V_{OH}.

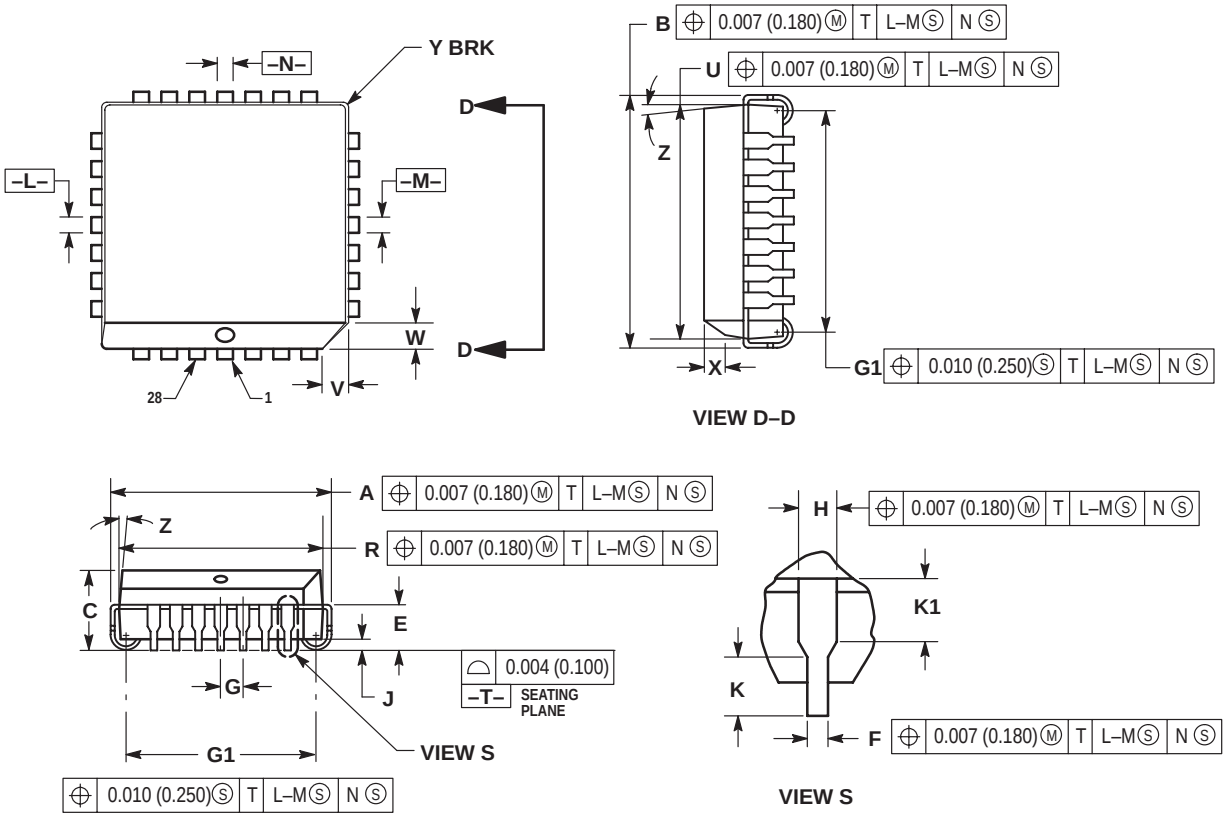
AC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = + 25°C		T_A = + 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHH}	Propagation Delay to Output CLK to Q	5.5 4.6	7.7 7.7	6.0 4.9	8.2 8.3	6.7 5.9	10.0 10.0	ns	CL = 50pF
t_{PHL}	Propagation Delay to Output MR to Q	4.4	7.5	4.7	8.1	5.8	10.5	ns	CL = 50pF
t_{PW}	Minimum Pulse Width CLK, MR	1.0		1.0		1.0		ns	
t_r	Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1.0V to 2.0V
t_f	Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1.0V to 2.0V
t_S	Setup Time	1.5		1.5		1.5		ns	
t_H	Hold Time	1.5		1.5		1.5		ns	
V_{PP}	Minimum Input Swing	200		200		200		mV	

1. Numbers are for both ++ and – – delay MR to Q.

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10°	2 °	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

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PUBLICATION ORDERING INFORMATION

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