MC10H604, MC100H604

Registered Hex TTL to ECL Translator

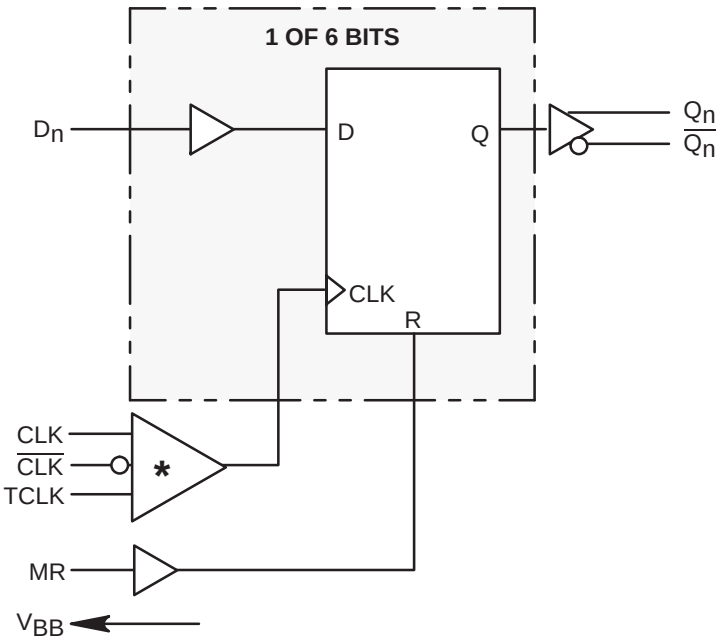
The MC10H/100H604 is a 6–bit, registered, dual supply TTL to ECL translator. The device features differential ECL outputs as well as a choice between either a differential ECL clock input or a TTL clock input. The asynchronous master reset control is an ECL level input..

With its differential ECL outputs and TTL inputs the H604 device is ideally suited for the transmit function of a HPPI bus type board–to–board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with MECL 10KH logic levels while the 100H device is compatible with 100K logic levels.

- Differential 50Ω ECL Outputs
- Choice Between Differential ECL or TTL Clock Input
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- Specified Within–Device Skew

LOGIC SYMBOL



* 1. When using MECL inputs, TCLK must be tied to ground (0V).
2. When using only one MECL input, the unused MECL input must be tied to V_{BB}, and TCLK must be tied to ground (0V).
3. When using TCLK, both MECL inputs must be tied to V_{EE} (–5.2V).

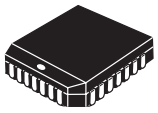
TRUTH TABLE

Dn	MR	TCLK/CLK	Qn+1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

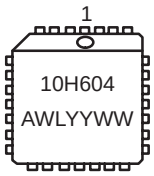
ON Semiconductor

http://onsemi.com



PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

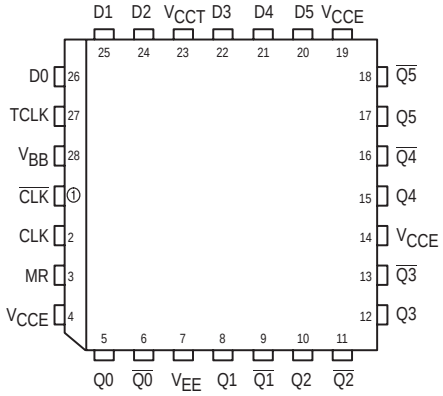


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
D0–D5	TTL Data Inputs
CLK, $\overline{CLK}$	Differential ECL Clock Input
TCLK	TTL Clock Input
MR	ECL Master Reset Input
Q0–Q5	True ECL Outputs
$\overline{Q0}$–$\overline{Q5}$	Inverted ECL Outputs
V_{CCE}	ECL V_{CC} (0V)
V_{CCT}	TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (–5.2V)

Pinout: 28–Lead PLCC (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC10H604FN	PLCC–28	37 Units/Rail
MC100H604FN	PLCC–28	37 Units/Rail

DC CHARACTERISTICS: VEE = VEE(Min) to VEE(Max); VCCE = GND; VCCT = 5.0V +10%

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	ECL Power Supply Current 10H 100H		130 130		130 140		130 150	mA	
I_{CCH} I_{CCL}	TTL Power Supply Current		35 45		35 45		35 45	mA	

10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ± 10%; V_{EE} = –5.20 V ±5%

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1060 –1950	–720 –1480	mV	
V_{BB}	Output Bias Voltage	–1400	–1290	–1370	–1270	–1330	–1210	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1020 –1950	–840 –1630	–980 –1950	–810 –1630	–910 –1950	–720 –1595	mV	50 Ω to –2.0 V

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –4.2 V to –5.5 V

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	145	 0.5	145	µA µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	
V_{BB}	Output Bias Voltage	–1400	–1280	–1400	–1280	–1400	–1280	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	–1025 –1810	–880 –1620	mV	50 Ω to –2.0 V

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

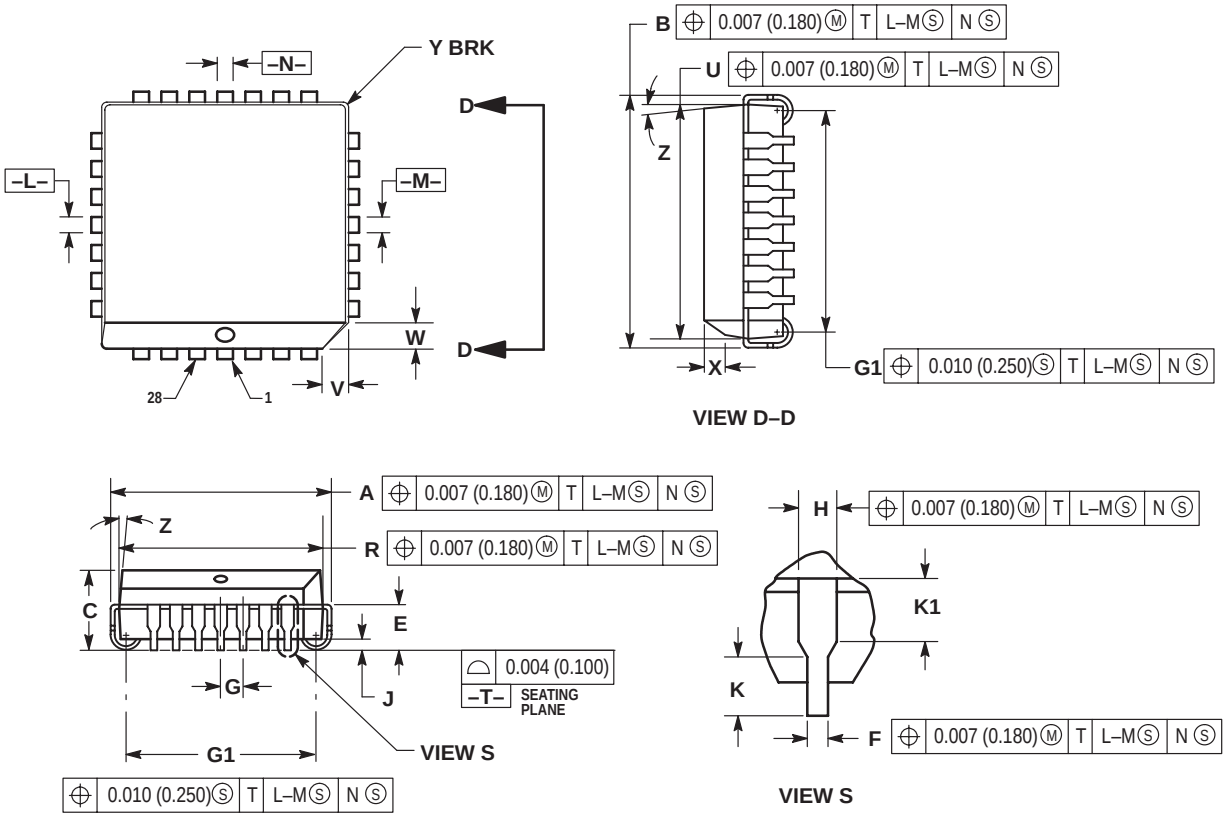
Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version); V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Parameter	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay CLK to Q to Output TCLK to Q MR to Q	1.5 2.0 1.5		3.5 4.0 4.0	1.5 2.0 1.5		3.5 4.0 4.0	1.5 2.0 1.5		3.5 4.0 4.0	ns	50Ω to –2.0V
t_S	Setup Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	50Ω to –2.0V
t_H	Hold Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	50Ω to –2.0V
t_{PW}	Minimum Pulse Width CLK, MR		1.0			1.0			1.0		ns	50Ω to –2.0V
V_{PP}	Minimum Input Swing					150					mV	
t_r t_f	Rise/Fall Times	0.3	1.0	2.0	0.3	1.0	2.0	0.3	1.0	2.0	ns	20% – 80%

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10°	2 °	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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