MC10H603, MC100H603

9-Bit Latch ECL to TTL Translator

The MC10H/100H603 is a 9–bit, dual supply ECL to TTL translator. Devices in the Motorola 9–bit translator series utilize the 28–lead PLCC for optimal power pinning, signal flow–through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. Latching is controlled by Latch Enable (LEN), and Master Reset (MR) resets the latches. A HIGH on $\overline{OEECL}$ sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9–Bit Ideal for Byte–Parity Applications
- 3–State TTL Outputs
- Flow–Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- Dual Supply
- 6.0 ns Max Delay into 50 pF, 12 ns into 200 pF (all outputs switching)
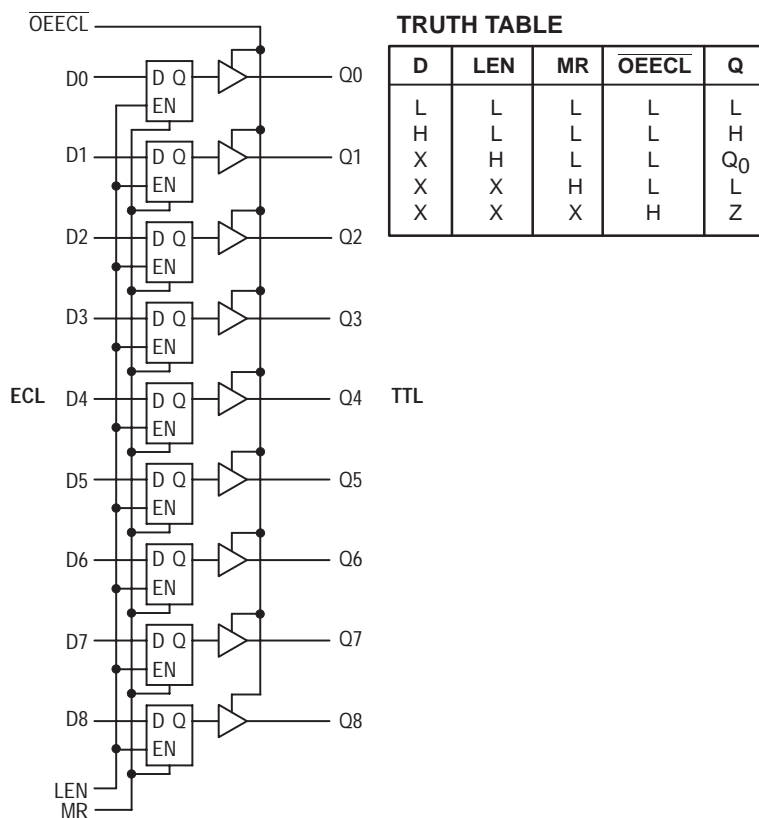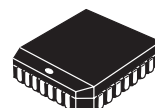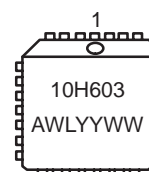- PNP TTL Inputs for Low Loading

ON Semiconductor

http://onsemi.com

PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM

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10H603
AWLYYWW
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A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2/−4.5 V)
D0–D8	Data Inputs (ECL)
Q0–Q8	Data Outputs (TTL)
$\overline{OEECL}$	3-State Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)
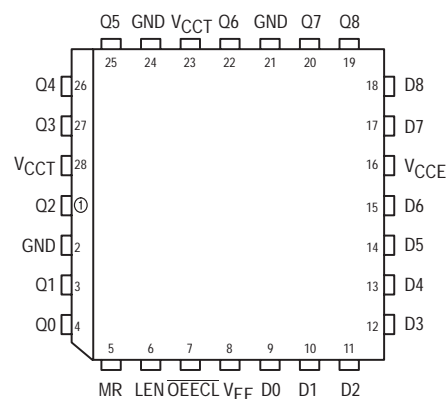
Figure 1. 28–Lead Pinout (Top View)

TRUTH TABLE

D	LEN	MR	$\overline{OEECL}$	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q_0
X	X	H	L	L
X	X	X	H	Z

Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping
MC10H603FN	PLCC–28	37 Units/Rail
MC100H603FN	PLCC–28	37 Units/Rail

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current		−64		−64		−64	mA	
I_{INH}	Input HIGH Current		225		145		145	µA	
I_{INL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1170	−840	−1130	−810	−1060	−720	mV	
V_{IL}	Input LOW Voltage	−1950	−1480	−1950	−1480	−1950	−1445		

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current		−63		−64		−68	mA	
I_{INH}	Input HIGH Current		225		145		145	µA	
I_{INL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1165	−880	−1165	−880	−1165	−880	mV	
V_{IL}	Input LOW Voltage	−1810	−1475	−1810	−1475	−1810	−1475		

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version);
V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{CCH}	Power Supply Current		110		110		110	mA	
I_{CCL}			110		110		110		
I_{CCZ}	Power Supply Current		110		110		110		
I_{OS}	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V
I_{OZH}	Output Disable Current HIGH		50		50		50	µA	V_{OUT} = 2.7 V
I_{OZL}	Output Disable Current LOW		−50		−50		−50		V_{OUT} = 0.5 V
V_{OHT}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OLT}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version);
V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	D	3.0 6.4	6.0 12	3.0 6.4	6.0 12	3.0 6.4	6.0 12	ns ns	C_L = 50 pF C_L = 200 pF
		LEN	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns ns	C_L = 50 pF C_L = 200 pF
		MR	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns ns	C_L = 50 pF C_L = 200 pF
t_{PLZ} t_{PHZ}	Output Disable Time		2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns ns	C_L = 50 pF C_L = 200 pF
t_{PZL} t_{PZH}	Output Enable Time		2.0 4.0	5.0 10	2.0 4.0	5.0 10	2.0 4.0	5.0 10	ns ns	C_L = 50 pF C_L = 200 pF
t_s	Setup Time	D to LEN	1.5		1.5		1.5		ns	
t_h	Hold Time	D to LEN	0.8		0.8		0.8		ns	
$t_{w(L)}$	LEN Pulse Width, LOW		2.0		2.0		2.0		ns	
t_R t_F	Output Rise/Fall Time 1.0 V − 2.0 V		0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns ns	C_L = 50 pF C_L = 200 pF

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D
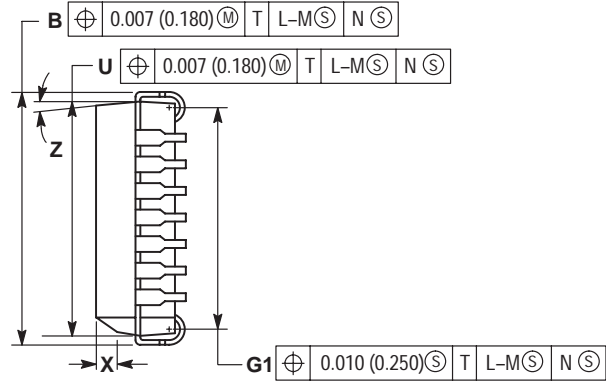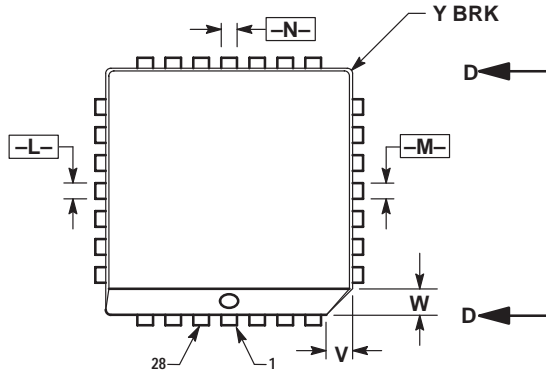
VIEW D–D
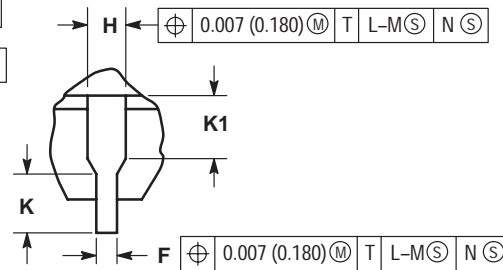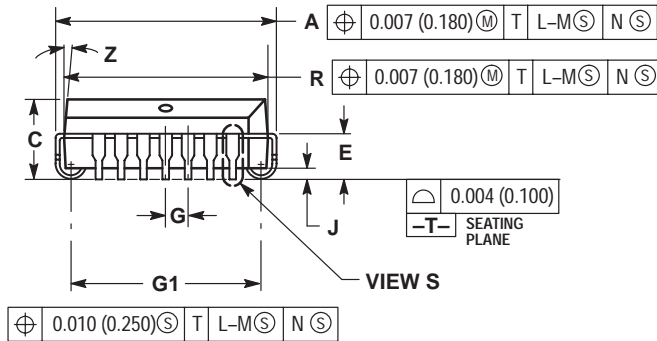
VIEW S

NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	–––	0.51	–––
K	0.025	–––	0.64	–––
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	–––	0.020	–––	0.50
Z	2 °	10°	2 °	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	–––	1.02	–––

MC10H603, MC100H603

PUBLICATION ORDERING INFORMATION