MC10H352

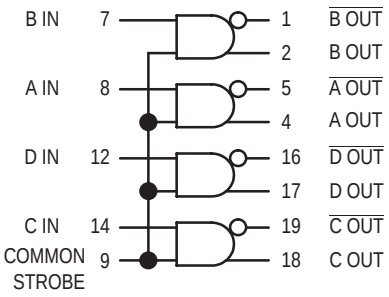
Quad CMOS to PECL* Translator

The MC10H352 is a quad translator for interfacing data between a CMOS logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H352 has CMOS compatible inputs and PECL complementary open–emitter outputs that allow use as an inverting/non–inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H352 can also be used with the MC10H350 to transmit and receive CMOS information differentially via balanced twisted pair lines.

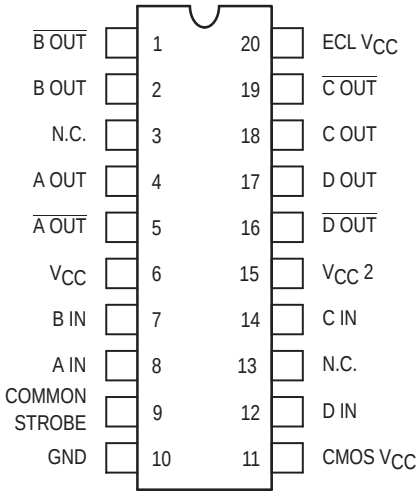
- Single +5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical

LOGIC DIAGRAM



V_{CC} (+5.0 VDC) = PINS 6, 11, 15, 20
GND = PIN 10

DIP PIN ASSIGNMENT

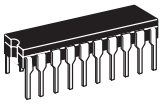


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

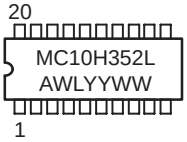
ON Semiconductor

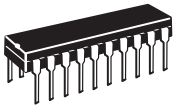
http://onsemi.com

MARKING DIAGRAMS

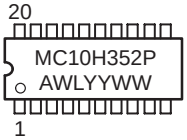


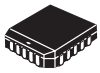
CDIP–20
L SUFFIX
CASE 732



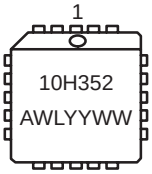


PDIP–20
P SUFFIX
CASE 738





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H352L	CDIP–20	18 Units/Rail
MC10H352P	PDIP–20	18 Units/Rail
MC10H352FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply	0 to +7.0	Vdc
V_I	Input Voltage (V_{CC} = 5.0 V)	0 to V_{CC}	Vdc
I_{out}	Output Current — Continuous — Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)†

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
ECL	Power Supply Current	—	50	—	45	—	50	mA
TTL		—	20	—	15	—	20	mA
I_R	Reverse Current Pins 7, 8, 12, 14 Pin 9	 — —	 25 100	 — —	 20 80	 — —	 25 100	µA
I_F	Forward Current Pins 7, 8, 12, 14 Pin 9	 — —	 –0.8 –3.2	 — —	 –0.6 –2.4	 — —	 –0.8 –3.2	mA
$V_{(BR)in}$	Input Voltage Breakdown	5.5	—	5.5	—	5.5	—	Vdc
V_I	Input Clamp Voltage (I_{in} = –18 mA)	—	–1.5	—	–1.5	—	–1.5	Vdc
V_{OH}	High Output Voltage (Note 1.)	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
V_{OL}	Low Output Voltage (Note 1.)	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
V_{IH}	High Input Voltage	3.15	—	3.15	—	3.15	—	Vdc
V_{IL}	Low Input Voltage	—	1.5	—	1.5	—	1.5	Vdc

1. With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.

**Positive Emitter Coupled Logic

AC PARAMETERS

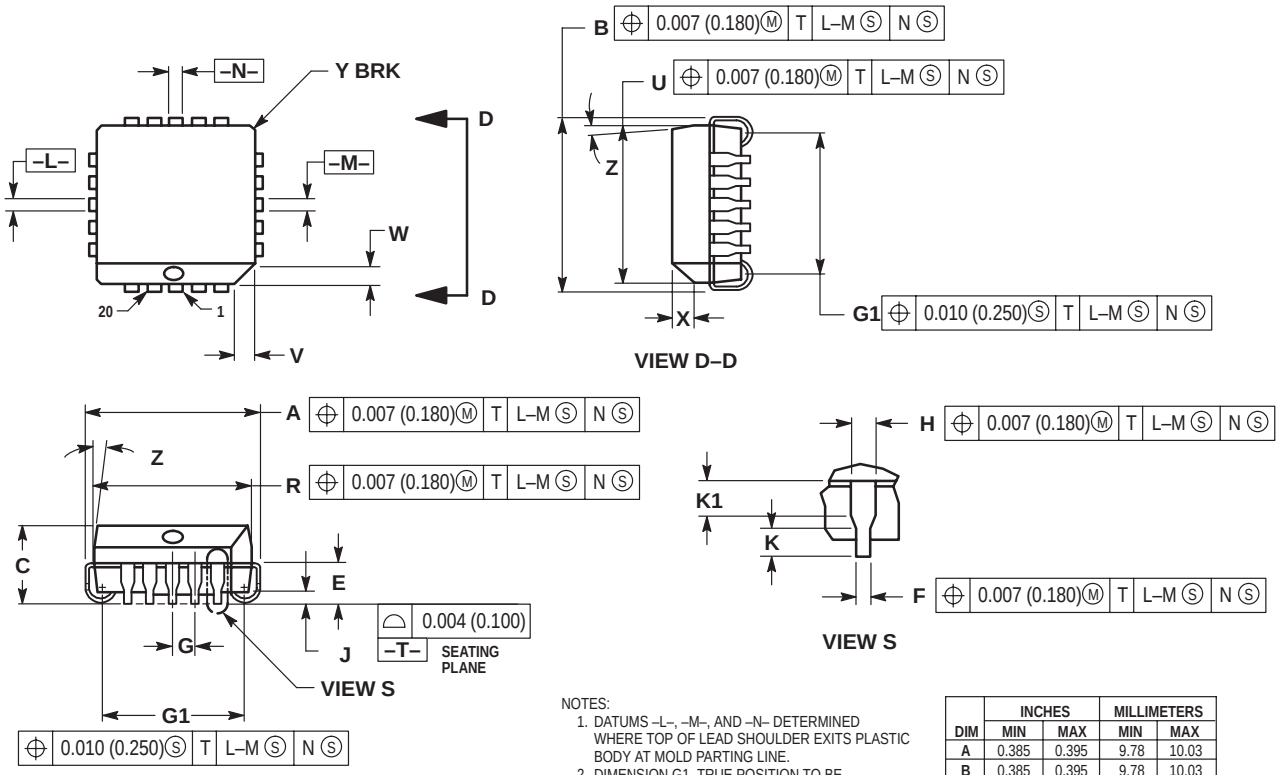
		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
t_{pd}	Propagation Delay (Note 2.)	0.4	1.9	0.4	2.0	0.4	2.1	ns
t_r	Rise Time (20% to 80%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
t_f	Fall Time (80% to 20%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
f_{max}	Maximum Operating Frequency	150	—	150	—	150	—	MHz

2. Propagation delay is measured on this circuit from V_{CC}/2 on the input waveform to the 50% point on the output waveform.

†Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to V_{CC} – 2.0 Vdc.

PACKAGE DIMENSIONS

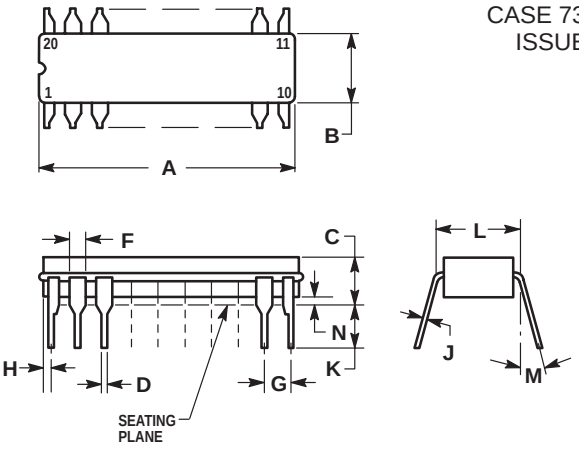
PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

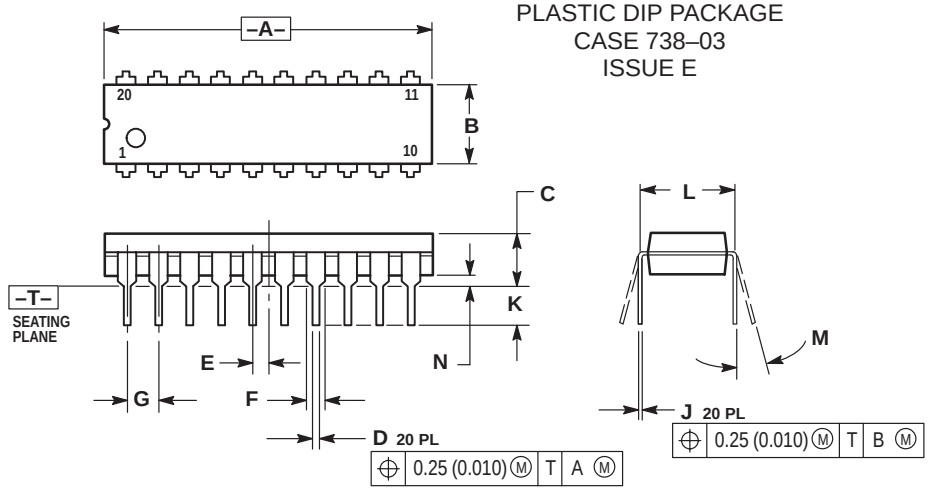
CDIP–20
L SUFFIX
CERAMIC DIP PACKAGE
CASE 732–03
ISSUE E



NOTES:
1. LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	INCHES	
DIM	MIN	MAX
A	0.940	0.990
B	0.260	0.295
C	0.150	0.200
D	0.015	0.022
F	0.055	0.065
G	0.100 BSC	
H	0.020	0.050
J	0.008	0.012
K	0.125	0.160
L	0.300 BSC	
M	0°	15°
N	0.010	0.040

PDIP–20
P SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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