4-Wide OR-AND/OR-AND Gate

The MC10H121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-Invert function, useful in data control and digital multiplexing applications. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power- supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	l _{out}	50 100	mA
Operating Temperature Range	T _A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

		0 °		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	_	29	_	26		29	mA
Input Current High Pins 3, 4, 5, 6, 7, 9 11, 12, 13, 14, 15 Pin 10	^l inH		500 610		295 360	1 1	295 360	μА
Input Current Low	l _{inL}	0.5		0.5		0.3	_	μΑ
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

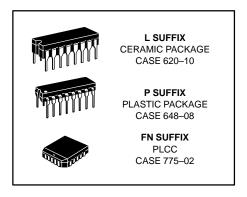
AC PARAMETERS

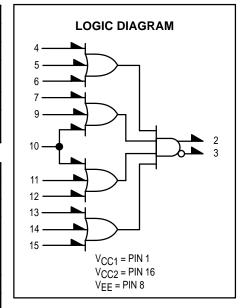
Propagation Delay Pin 10 Only Exclude Pin 10	^t pd	0.45 0.55	1.8 1.95	0.45 0.6	1.8 2.0	0.55 0.7	2.2 2.4	ns
Rise Time	t _r	0.5	1.7	0.5	1.8	0.5	1.9	ns
Fall Time	t _f	0.5	1.7	0.5	1.8	0.5	1.9	ns

NOTE:

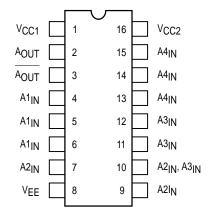
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to -2.0 volts.

MC10H121



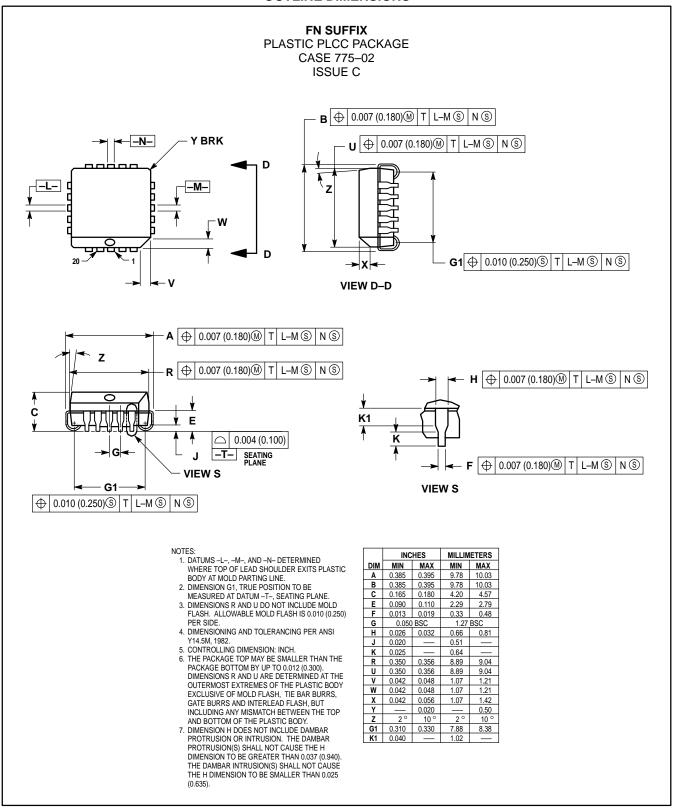


DIP PIN ASSIGNMENT

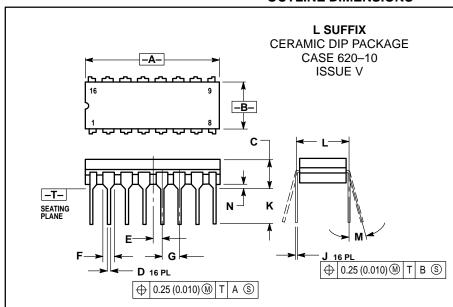


Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

OUTLINE DIMENSIONS



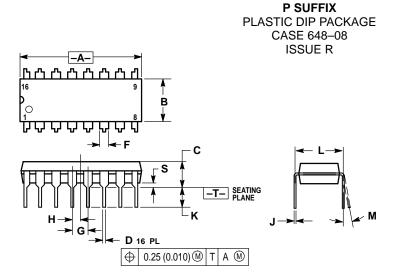
OUTLINE DIMENSIONS



NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62 BSC		
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050 BSC		1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

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