Quad Exclusive OR Gate

The MC10H113 is a Quad Exclusive OR Gate with an enable common to all four gates. The outputs may be wire–ORed together to perform a 4–bit comparison function (A = B). The enable is active LOW.

- Propagation Delay, 1.3 ns Typical
- Power Dissipation 175 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V _{CC} = 0)	V _{EE}	-8.0 to 0	Vdc
Input Voltage (V _{CC} = 0)	VI	0 to VEE	Vdc
Output Current — Continuous — Surge	lout	50 100	mA
Operating Temperature Range	T _A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T _{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2 \text{ V } \pm 5\%$) (See Note)

		0 °		25 °		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙE	_	46	_	42	-	46	mA
Input Current High Pins 5, 7, 11, 13 Pins 4, 6, 10, 12 Pin 9	linH	111	430 510 1100	111	270 320 740	111	270 320 740	μΑ
Input Current Low	l _{inL}	0.5	1	0.5	_	0.3	_	μΑ
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V _{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

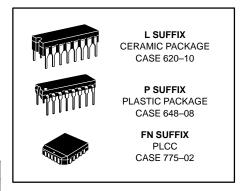
AC PARAMETERS

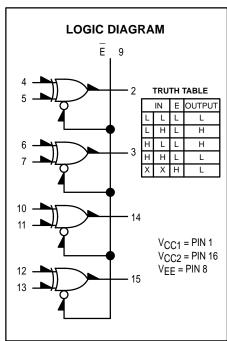
Propagation Delay Data Enable	^t pd	0.4 0.5	1.7 2.3	0.4 0.5	1.8 2.4	0.5 0.6	1.9 2.5	ns
Rise Time	t _r	0.5	1.8	0.6	1.9	0.6	2.0	ns
Fall Time	t _f	0.5	1.8	0.6	1.9	0.6	2.0	ns

NOTE:

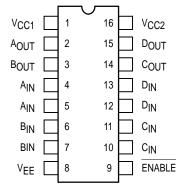
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to -2.0 volts.

MC10H113



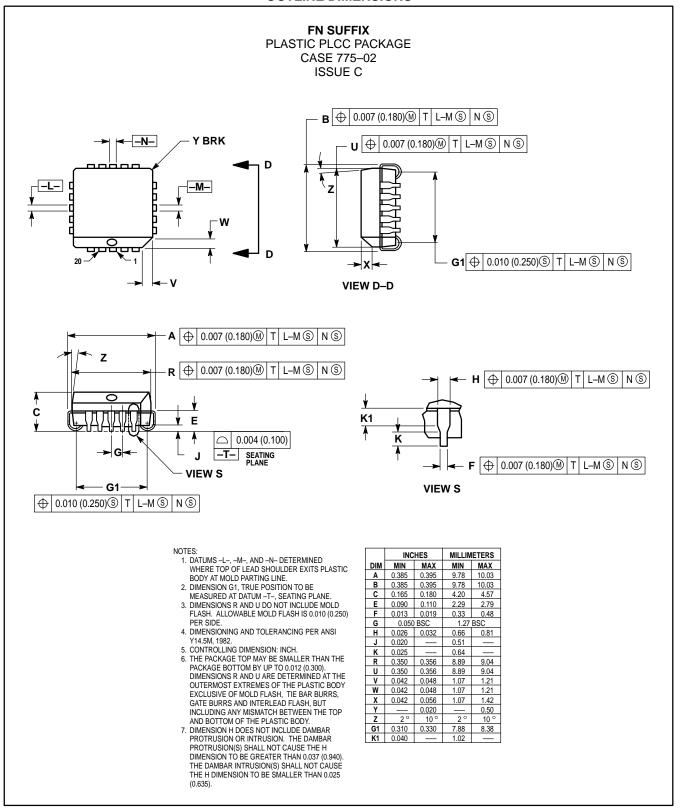


DIP PIN ASSIGNMENT



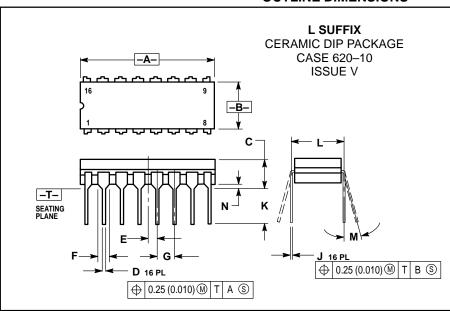
Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion
Tables on page 6–11 of the Motorola MECL Data
Book (DL122/D).

OUTLINE DIMENSIONS



MOTOROLA 2–214

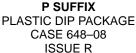
OUTLINE DIMENSIONS

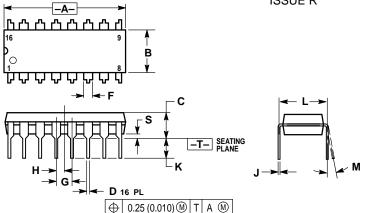


NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100 BSC		2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300 BSC		7.62 BSC		
М	0°	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.740	0.770	18.80	19.55		
В	0.250	0.270	6.35	6.85		
С	0.145	0.175	3.69	4.44		
D	0.015	0.021	0.39	0.53		
F	0.040	0.70	1.02	1.77		
G	0.100	0.100 BSC		2.54 BSC		
Н	0.050	0.050 BSC		1.27 BSC		
J	0.008	0.015	0.21	0.38		
K	0.110	0.130	2.80	3.30		
L	0.295	0.305	7.50	7.74		
М	0°	10 °	0°	10 °		
S	0.020	0.040	0.51	1.01		

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