Product Preview
1:2 Fanout Differential PECL to TTL Translator

The MC10EPT26 is a 1:2 Fanout Differential PECL to TTL translator. Because PEL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8–lead SOIC package and the 1:2 fanout design of the EPT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The VBB output allows the EPT26 to also be used in a single–ended input mode. In this mode the VBB output is tied to the D0b input for a non–inverting buffer or the D0 input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01μF capacitor.

The EPT26 is available in both ECL standards; the 10EPT is compatible with positive MECL 10H logic levels while the 100EPT is compatible with positive ECL 100k logic levels.

- 1.4ns Typical Propagation Delay
- Differential LVPECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flowthrough Pinouts
- ESD performance: Human Body model 2000V, Machine Model 200V
- 275MHz Fmax (Steady bit stream, not pseudo–random)

Note:
1) Pulling the output higher than VCC is not recommended. Doing so causes excessive leakage and possible latchup leading to reliability risk.

MC10EPT26
MC100EPT26

D SUFFIX
8–LEAD PLASTIC SOIC PACKAGE
CASE 751-06

PIN DESCRIPTION

PIN	FUNCTION
Qn	TTL Outputs
D0/D0b	Diff PECL Input Pair
V_{CC}	+5.0V Supply
V_{BB}	Reference Output
GND	Ground
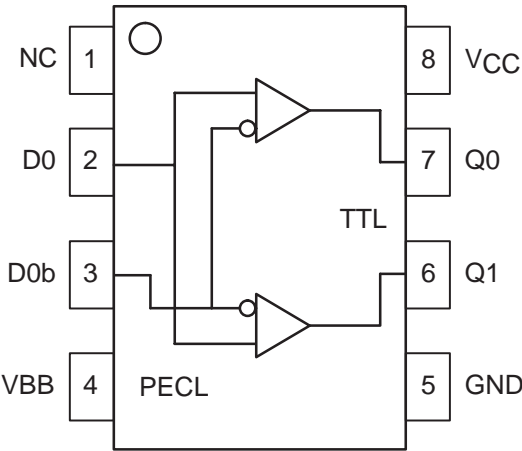
Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply	7.0	VDC
θT_A	Operating Temperature Range	−40 to +85	°C
T_{stg}	Storage Temperature Range	−55 to +155	°C
θ	Thermal Resistance Through Package	130	°C/W

* Maximum Ratings are those values beyond which damage to the device may occur.
  Functional operation should be restricted to the Recommended Operating Conditions.

10E DC CHARACTERISTICS (V_{EE} = 3.0 to 3.6; T_A = −40°C to 85°C)

Symbol	Characteristic	−40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Power Supply Current (Outputs set to High)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
I_{CCL}	Power Supply Current (Outputs set to Low)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V_{IH}	Input HIGH Voltage (VCC = 3.3) [1]	2070	2410	2130	2460	2170	2490	2240	2580	mV
V_{IL}	Input LOW Voltage (VCC = 3.3) [1]	1350	1800	1350	1820	1350	1820	1350	1855	mV
V_{OH}	Output HIGH Voltage (I_{OH} = −3mA) [2]		2.2		2.2		2.2		2.2	mV
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) [2]	0.5		0.5		0.5		0.5		mV
I_{IH}	Input HIGH Current	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{IL}	Input LOW Current	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA

Conditions: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.
1. All values vary 1:1 with VCC when VCC other than 3.3V.
2. All loading with 500 ohms to Gnd, CL = 20pF.

100E DC CHARACTERISTICS (V_{EE} = 3.0 to 3.6; T_A = −40°C to 85°C)

Symbol	Characteristic	Min	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to High)	TBD	TBD	mA
I_{CCL}	Power Supply Current (Outputs set to Low)	TBD	TBD	mA
V_{IH}	Input HIGH Voltage (VCC = 3.3) [1]	2135	2420	mV
V_{IL}	Input LOW Voltage (VCC = 3.3) [1]	1490	1825	mV
V_{OH}	Output HIGH Voltage (I_{OH} = −3mA) [2]		2.2	mV
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) [2]	0.5		mV
I_{IH}	Input HIGH Current	TBD	TBD	µA
I_{IL}	Input LOW Current	TBD	TBD	µA

Conditions: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.
1. All values vary 1:1 with VCC when VCC other than 3.3V.
2. All loading with 500 ohms to Gnd, CL = 20pF.

AC CHARACTERISTICS (V_{EE} = −3.6 to −3.0; V_{CC} = GND)

| Symbol	Characteristic	−40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency[3]		275			275			275			275		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output		1.45 1.4			1.45 1.4			1.45 1.4			1.45 1.4		ns
t_{SK++}	Output to Output skew ++		60			60			60			60		ps
$t_{SK—}$	Output to Output skew —		25			25			25			25		ps
t_{SKwpp}	Part to Part skew		0.5			0.5			0.5			0.5		ns
V_{PP}	Minimum Input Swing[4]		150			150			150			150		mV
V_{CMR}	Common Mode Range[5]	TBD		TBD	TBD		TBD	TBD		TBD	TBD		TBD	V
t_r t_f	Output Rise Q/Qb Fall Times (20% – 80%)		525 450			525 450			525 450			525 450		ps

3. F_{max} specified with required to meet 500mV to 2.2V output specification in a continuous bit stream, pseudo–random not specified.
4. Minimum input swing for which AC parameters guaranteed
5. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR is dependent on V_{EE} and is equal to V_{EE} + tbdV.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T
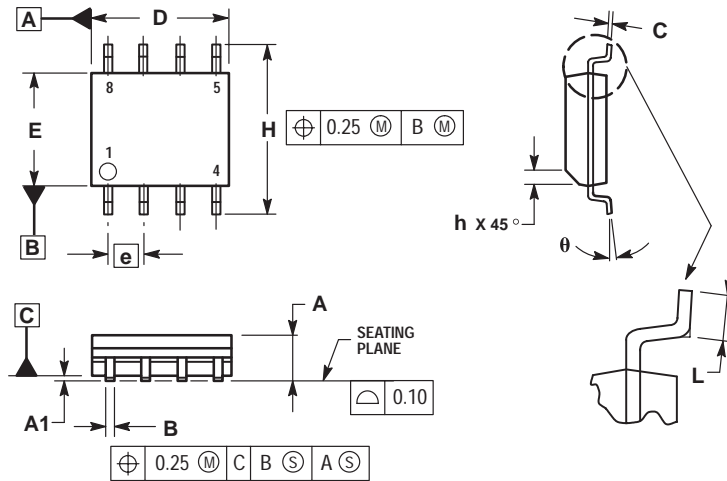
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0 °	7 °

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