Product Preview

D Flip Flop with Set and Reset

The MC10/100EP51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 and LVEL51 devices.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EP51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the \overline{CLK} input will be biased at $V_{CC}/2$.

- 420ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with $V_{EE} = 0V$
- ECL mode: 0V V_{CC} with $V_{EE} = -3.0V$ to -5.5V
- 75kΩ Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at VEE
- ESD Protection: >2KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.
 For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 165 devices

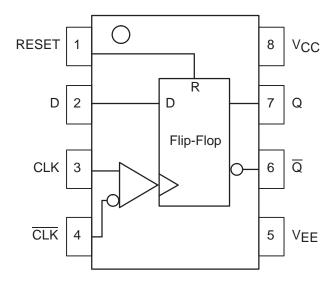


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

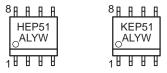


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MARKING DIAGRAM



H = MC10 L = Wafer Lot K = MC100 Y = Year A = Assembly Location W = Work Week

^{*}For additional information, see Application Note AND8002/D

PIN DESCRIPTION								
PIN	FUNCTION							
CLK, CLK	ECL Clock Inputs							
Reset	ECL Asynchronous Reset							
D	ECL Data Input							
Q, \overline{Q}	ECL Data Outputs							
VCC	Positive Supply							
VEE	Negative, 0 Supply							

TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
Н	L	Z	Н
X	Н	Х	L

Z = LOW to HIGH Transition

ORDERING INFORMATION

Device	Package	Shipping				
MC10EP51D	SOIC	98 Units/Rail				
MC10EP51DR2	SOIC	2500 Tape & Reel				
MC100EP51D	SOIC	98 Units/Rail				
MC100EP51DR2	SOIC	2500 Tape & Reel				

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
VEE	Power Supply (V _{CC} = 0V)	-6.0 to 0	VDC
Vcc	Power Supply (VEE = 0V)	6.0 to 0	VDC
VI	Input Voltage ($V_{CC} = 0V$, V_I not more negative than V_{EE})	-6.0 to 0	VDC
VI	Input Voltage ($V_{EE} = 0V$, V_{I} not more positive than V_{CC})	6.0 to 0	VDC
l _{out}	Output Current Continu	ous 50 rge 100	mA
TA	Operating Temperature Range	-40 to +85	°C
T _{stg}	Storage Temperature	-65 to +150	°C
θЈА	Thermal Resistance (Junction–to–Ambient) Still 500li	Air 190 fpm 130	°C/W
θJC	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T _{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

^{*} Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL ($V_{CC} = 0V$; $V_{EE} = -5.5V$ to -3.0V) (Note 3.)

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current (Note 1.)	26	34	44	26	35	45	28	37	47	mA
VOH	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
VOL	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
VIH	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
V _{IL}	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
lн	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.

2. All loading with 50 ohms to V_{CC}-2.0 volts.

3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL ($V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$) (Note 6.)

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current (Note 4.)	26	34	44	26	35	45	28	37	47	mA
VOH	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
VOL	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
VIH	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
VIL	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
lН	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

- 4. $V_{CC} = 3.3V$, $V_{EE} = 0V$, all other pins floating.
- 5. All loading with 50 ohms to V_{CC}-2.0 volts.
- 6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL ($V_{CC} = 5.0V \pm 0.5V$, $V_{EE} = 0V$) (Note 9.)

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current (Note 7.)	26	34	44	26	35	45	28	37	47	mA
Vон	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
VOL	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
VIH	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
VIL	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
lН	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

- 7. $V_{CC} = 5.0V$, $V_{EE} = 0V$, all other pins floating.
- 8. All loading with 50 ohms to V_{CC} -2.0 volts.
- 9. Input and output parameters vary 1:1 with V_{CC}.

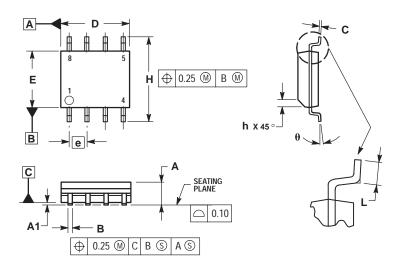
AC CHARACTERISTICS ($V_{CC} = 0V$; $V_{EE} = -3.0V$ to -5.5V) or ($V_{CC} = 3.0V$ to 5.5V; $V_{EE} = 0V$)

	, 00 , LL	/ (00			7 LL = 0V)						
			–40°C		25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
fmax	Maximum Toggle Frequency (Note 10.)					3.0					GHz
^t PLH [,] ^t PHL	Propagation Delay to Output Differential CLK, CLK->Q, Q RESET->Q, Q					420 420					ps
^t RR	Reset Recovery					140					ps
t _S	Setup Time Hold Time					50 50					ps
^t SKEW	Duty Cycle Skew (Note 11.) Skew Part–to–Part					TBD TBD					ps
tpW	Minimum Pulse Width CLK, RESET					450					ps
^t JITTER	Cycle-to-Cycle Jitter					TBD					ps
t _r t _f	Output Rise/Fall Times (20% – 80%) Q, $\overline{\mathbb{Q}}$					130					ps

^{10.} F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

PACKAGE DIMENSIONS

SO-8 **D SUFFIX** PLASTIC SOIC PACKAGE CASE 751-06 ISSUE T



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS ARE IN MILLIMETER.
 3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS								
DIM	MIN	MAX							
Α	1.35	1.75							
A1	0.10	0.25							
В	0.35	0.49							
С	0.19	0.25							
D	4.80	5.00							
Ε	3.80	4.00							
е	1.27	BSC							
Н	5.80	6.20							
h	0.25	0.50							
L	0.40	1.25							
θ	0°	7°							

Notes



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