MC10EP131

Product Preview

Quad D Flip Flop with Set, Reset and Differential Clock

The MC10EP131 is a Quad Master–slaved D flip flop with common set and separate resets. The device is an expansion of the E131 with differential common clock and individual clock enables. With AC performance faster than the E131 device, the EP131 is ideal for applications requiring the fastest AC performance available. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable (C0–3) inputs for clocking. Common clocking is achieved by holding the C0–3 inputs LOW and using C_C to clock all four flip-flops. In this case, the C0–3 inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets (R0–3) and an asynchronous set (SET) are provided.

Data enters the master when both C_C and C0–3 are LOW, and transfers to the slave when either C_C or C0–3 (or both) go HIGH.

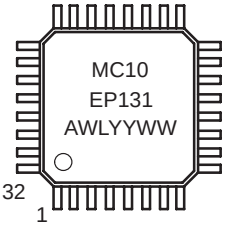
- 450ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- Differential Individual and Common Clocks
- Individual Asynchronous Resets
- Asynchronous Set
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 2,
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 935 devices

ON Semiconductor

http://onsemi.com

32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP131FA	TQFP	250 Units/Tray
MC10EP131FAR2	TQFP	2000 Tape & Reel

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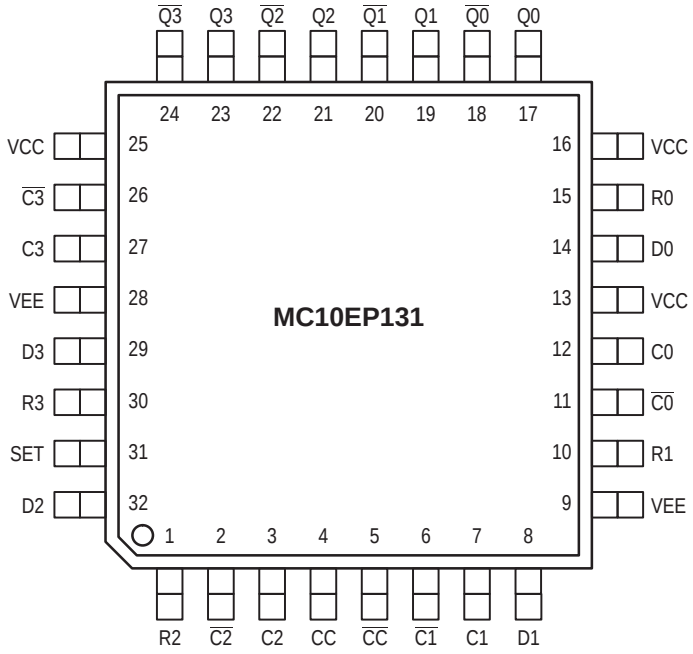
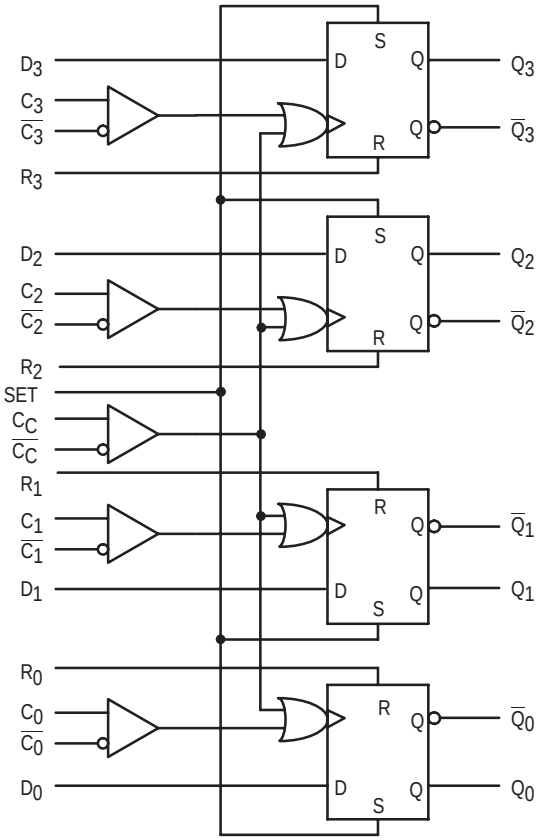


Figure 1. 32–Lead TQFP Pinout
(Top View)

PIN DESCRIPTION	
PIN	**FUNCTION**
D0–3	ECL Data Inputs
C0–3, $\overline{C0–3}$	ECL Separate Clock Inputs
CC, $\overline{CC}$	ECL Common Clock Inputs
R0–3	ECL Asynchronous Reset
SET	ECL Asynchronous Set
Q0–3, $\overline{Q0–3}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

All V_{CCO} pins are internally tied together on the die, but it is highly recommended that all pins be externally connected to evenly distribute power.

LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 3.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)					90					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)					90					mA
V_{OH}	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC}–2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)					90					mA
V_{OH}	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

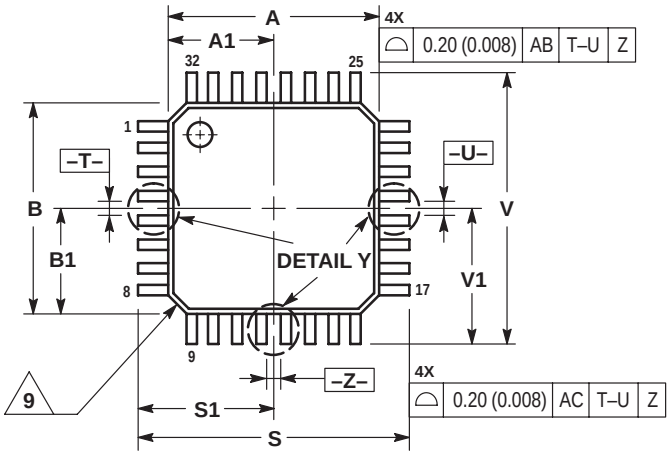
AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

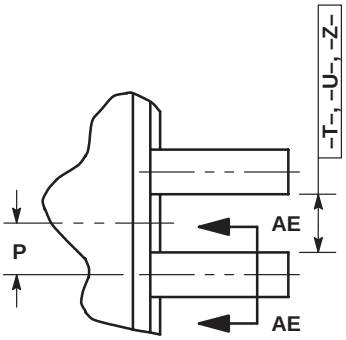
Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 10.)						3.0					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	C0–3 CC R0–3 SET					450 450 400 400					ps
t_{RR}	Set/Reset Recovery						150					ps
t_S t_H	Setup Time Hold Time						50 50					ps
t_{SKEW}	Duty Cycle Skew (Note 11.) Skew Part–to–Part						15 TBD					ps
t_{PW}	Minimum Pulse Width	CLK, SET, RESET		TBD			400			TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times (20% – 80%)	Q, $\overline{Q}$					150					ps

10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

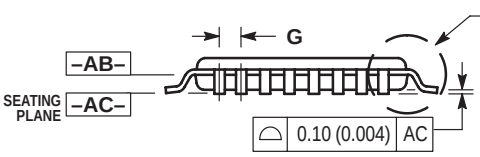
PACKAGE DIMENSIONS

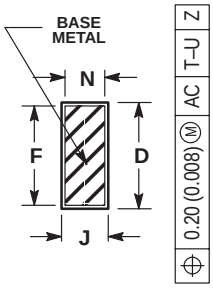
TQFP
FA SUFFIX
32–LEAD PLASTIC PACKAGE
CASE 873A–02
ISSUE A



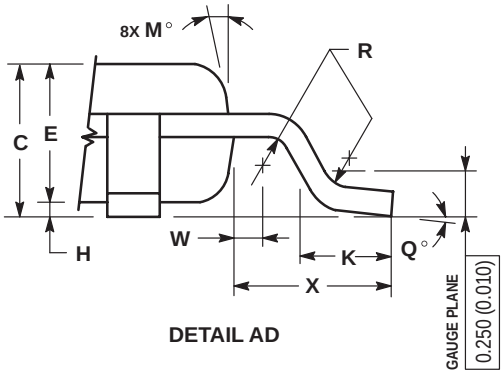


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

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