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MC10320
MC10320-1

Specifications and Applications Information

TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

The MC10320 integrates a triple 4-bit digital-to-analog converter and a 16 x 12 color look-up table into a single 28 pin IC for use in a high resolution color graphics display system. The outputs are EIA-343-A compatible red, blue, and green video signals capable of driving single or doubly terminated 50 ohm or 75 ohm cables directly. Complementary outputs are provided for custom displays.

Control inputs include $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ to produce the levels required for vertical and horizontal retrace.

The color look-up table allows up to 16 color combinations (out of a palette of 4096 possible colors) on the screen at any one time. The table can be updated as often as required.

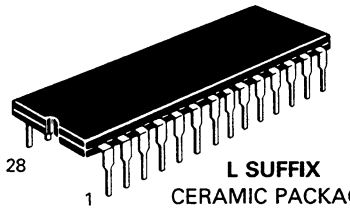
The lower speed digital inputs ($\overline{\text{WRITE}}$, DATA, and $\overline{\text{SYNC}}$) are TTL compatible, whereas the high speed inputs ($\overline{\text{ADDRESS}}$, PIXEL CLOCK, and $\overline{\text{BLANK}}$) can be user programmed to either ECL or TTL compatability. The address and blank signals are latched into input registers, facilitating the timing requirements for those signals. Additional registers frame the data as it is presented to the three DACs, ensuring low glitch area and matched response.

Innovative level translators permit the MC10320 series to be used in single or dual supply systems, permitting compatability with most any system configuration. The MC10320 series is fabricated with Motorola's MOSAIC process, which provides both low power consumption and high speed.

- Triple 4-Bit Video DAC with 16 x 12 Color Look-Up Table
- 125 MHz Max Pixel Rate (MC10320), 90 MHz Max (MC10320-1)
- User Selectable TTL or ECL Compatability on High Speed Inputs
- Single/Dual Supply Operation (Inputs and/or Outputs May Be Above/Below Ground)
- Supply Sensitivity Typically −34 dB
- EIA-343-A Compatible Output Levels
- Directly Drives 50 or 75 Ohm Cables
- Low Power Dissipation — 684 mW Typical
- Internal Bandgap Reference
- $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ Control Inputs

TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

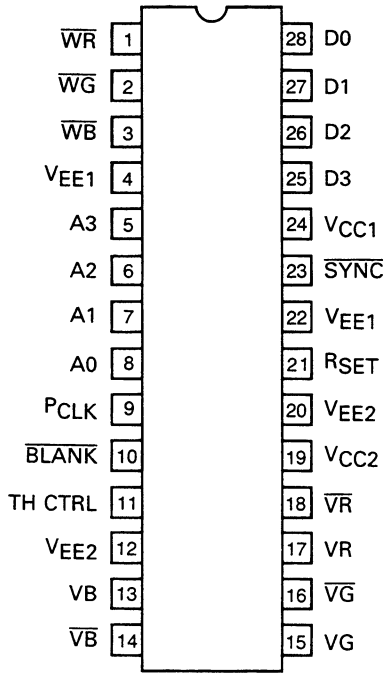
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 733-04

PIN CONNECTIONS

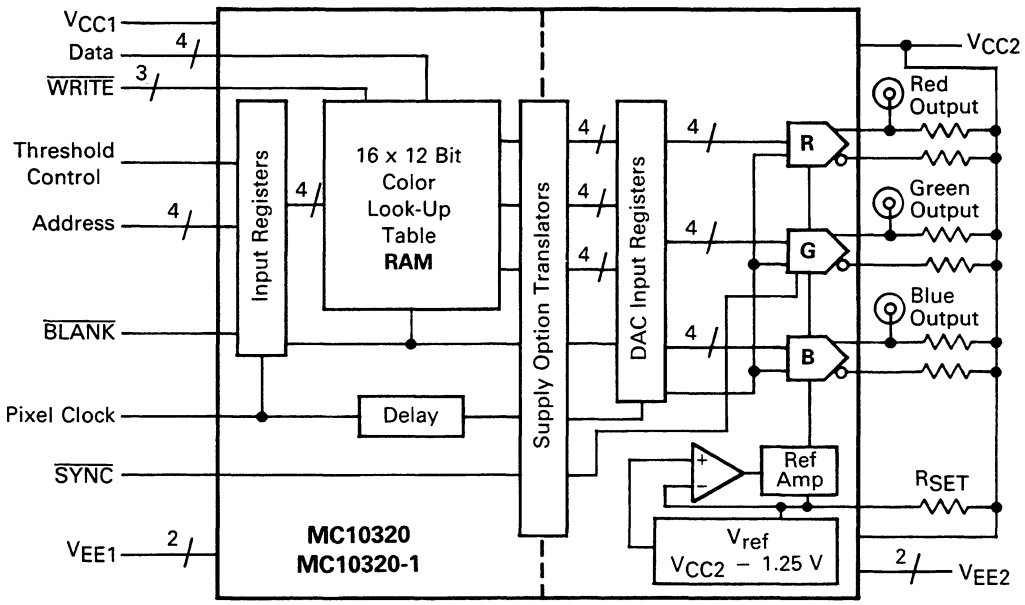
(Top View)



ORDERING INFORMATION

Maximum Pixel Rate	Device
125 MHz	MC10320L
90 MHz	MC10320L-1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltages		Vdc
V_{CC1} (Measured to V_{EE1})	−0.5, +7.0	
V_{CC2} (Measured to V_{EE2})	−0.5, +7.0	
V_{EE1} (Measured to V_{EE2})	−0.5, +7.0	
V_{CC2} (Measured to V_{EE1})	−0.5, +7.0	
Input Voltages		
(Address, Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$, $\overline{BLANK}$, P_{CLK}, and Threshold Control)	$V_{EE1}-0.5$, $V_{CC1}+0.5$	Vdc
R_{SET} (Pin 21)	$V_{EE2}-0.5$, V_{CC2}	Vdc
R_{SET} External Resistor	0, 3.0 k	Ω
Outputs (VR, $\overline{VR}$, VG, $\overline{VG}$, VB, $\overline{VB}$ Measured to V_{EE2})	+2.5, +8.0	Vdc
Junction Temperature	−55, +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Single Supply — V_{CC1}, V_{CC2}	4.5	5.0	5.5	Vdc
V_{EE1}, V_{EE2}	—	0	—	
or V_{CC1}, V_{CC2}	—	0	—	
V_{EE1}, V_{EE2}	−4.5	−5.0	−5.72	
Dual Supply — V_{CC1}	4.5	5.0	5.5	
V_{CC2}	—	0	—	
V_{EE1}	—	0	—	
V_{EE2}	−4.5	−5.0	−5.72	
R_{SET} (Between V_{CC2} and Pin 21)	500	1.0 k	2.0 k	Ω
I_{SET} (Determined by R_{SET})	0.55	1.25	2.8	mA
R_L (Load Resistance at Each Output)	0	—	75	Ω
Input Voltages — Threshold Control (Pin 11, See Text)	V_{EE1}	—	V_{CC1}	Vdc
TTL High (Pins 1–3, 5–10, 23, 25–28,	$V_{EE1}+2.0$	—	V_{CC1}	
TTL Low Pin 11 connected to V_{EE1})	V_{EE1}	—	$V_{EE1}+0.8$	
ECL High (Pins 5–10 only, Pin 11	$V_{CC1}-1.13$	—	V_{CC1}	
ECL Low connected to V_{CC1})	V_{EE1}	—	$V_{CC1}-1.48$	
Output Compliance (Measured to V_{CC2})	−2.0	0	+2.0	Vdc
Ambient Temperature	0	—	+70	°C

ELECTRICAL CHARACTERISTICS (See Figure 1, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (Each DAC)	Res	4.0	4.0	4.0	Bits
Palette Colors (Active)	—	—	—	16	Colors
(Total Available)	—	—	—	4096	Colors
Integral Nonlinearity	INL	−1/4	0	+1/4	LSB
Differential Nonlinearity	DNL	−1/4	0	+1/4	LSB
Monotinicity	—	Guaranteed*			
Output Levels @ VR, VG, VB, relative to V_{CC2} unless otherwise noted.					
Ref. White Offset (DAC Input = 1111)	I_{OW}	—	50	400	μA
$\overline{BLANK}$, $\overline{SYNC}$ = 1	V_{OW}	−15	−1.9	—	mV
Ref. Black (DAC Input = 0000) Relative to	I_{OB}	16.1	17.2	18.2	mA
Ref. White, $\overline{BLANK}$, $\overline{SYNC}$ = 1	V_{OB}	−682	−645	−604	mV
Blank Level Relative to Ref. Black	I_{OBK}	1.17	1.33	1.5	mA
$\overline{BLANK}$ = 0, $\overline{SYNC}$ = 1	V_{OBK}	−56.2	−50	−43.9	mV
Sync Level — VG Only, Relative to Blank	I_{OSY}	6.71	7.63	8.54	mA
$\overline{SYNC}$, $\overline{BLANK}$ = 0	V_{OSY}	−320	−286	−251	mV
Total Error (Each DAC, Ref. White to Ref. Black)	G_{ER}	−6.0	0	+6.0	%
Gain Tracking Error (Any two DACs @ Ref. Black)	G_{TR}	−3.0	0	+3.0	%
Output Impedance @ VR, VG, VB	Z_o	10	100	—	kΩ
Reference Voltage (V_{CC2} − V_{RSET}, R_{SET} = 1.0 kΩ)	V_{REF}	−1.4	−1.25	−1.1	Vdc
Pin 21 Output DC Resistance (0 mA < I_{REF} < 3.0 mA)	—	—	3.0	—	Ω
Input Voltage High (Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$)	V_{IHA}	V_{EE1} + 2.0	—	V_{CC1}	Vdc
Low (Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$)	V_{ILA}	V_{EE1}	—	V_{EE1} + 0.8	
Input Voltage High (Address, P_{CLK}, $\overline{BLANK}$)					
(Threshold Control @ V_{EE1} [TTL Mode])	V_{IHB}	V_{EE1} + 2.0	—	V_{CC1}	
(Threshold Control @ V_{CC1} [ECL Mode])	V_{IHC}	V_{CC1} − 1.13	—	V_{CC1}	
Input Voltage Low (Address, P_{CLK}, $\overline{BLANK}$)					
(Threshold Control @ V_{EE1} [TTL Mode])	V_{ILB}	V_{EE1}	—	V_{EE1} + 0.8	
(Threshold Control @ V_{CC1} [ECL Mode])	V_{ILC}	V_{EE1}	—	V_{CC1} − 1.48	
Input Current @ 2.4 V (TTL Mode) (All Input Pins	I_{IHA}	—	50	150	μA
@ 0.4 V (TTL Mode) Except Pin 11)	I_{ILA}	—	10	100	
Input Current @ V_{CC1} − 0.8 V (ECL Mode)	I_{IHB}	—	100	250	
@ V_{CC1} − 1.8 V (ECL Mode)	I_{ILB}	—	70	200	
Input Current @ Pin 11 (Pin 11 = V_{CC1})	I_{ITH}	−5.0	0	—	mA
@ Pin 11 (Pin 11 = V_{EE1})	I_{ITL}	−1.0	−0.4	—	
Signal Feedthrough to Outputs Due to	SRR				dB
Pixel Clock (@ 125 MHz for MC10320,		—	−50	—	
$\overline{BLANK}$ 90 MHz MC10320-1)		—	−50	—	
Data		—	−60	—	
Power Supply Rejection Ratio (All DACs)	PSRR				dB
V_{CC1} @ 1.0 kHz		—	60	—	
V_{CC1} @ 1.0 MHz		—	45	—	
V_{CC1} @ 50 MHz		—	30	—	
V_{EE2} @ 1.0 kHz		—	50	—	
V_{EE2} @ 1.0 MHz		—	33	—	
V_{EE2} @ 50 MHz		—	12	—	
Power Supply Sensitivity**		—	0.02	0.12	%/%
Power Supply Requirements (See Figure 1)					mA
V_{CC1} Current (V_{CC1} − V_{EE1} = 5.0 V)	I_{CC1}	—	50	70	
V_{EE1} Current (V_{CC1} − V_{EE1} = 5.0 V)	I_{EE1}	—	−50	−70	
V_{CC2} Current (V_{CC2} − V_{EE2} = 5.0 V)	I_{CC2}	—	28	45	
V_{EE2} Current (V_{CC2} − V_{EE2} = 5.0 V, Includes output currents)	I_{EE}	—	−92	−120	
Power Dissipation (@ 5.0 volt supplies)	P_D	—	684	894	mW

*Guaranteed by linearity tests.

**(V_{CC1} − V_{EE1}) and (V_{CC2} − V_{EE2}) are each varied from 4.5 to 5.72 volts, but not simultaneously.

TIMING CHARACTERISTICS (See Timing Diagram — Figure 2)

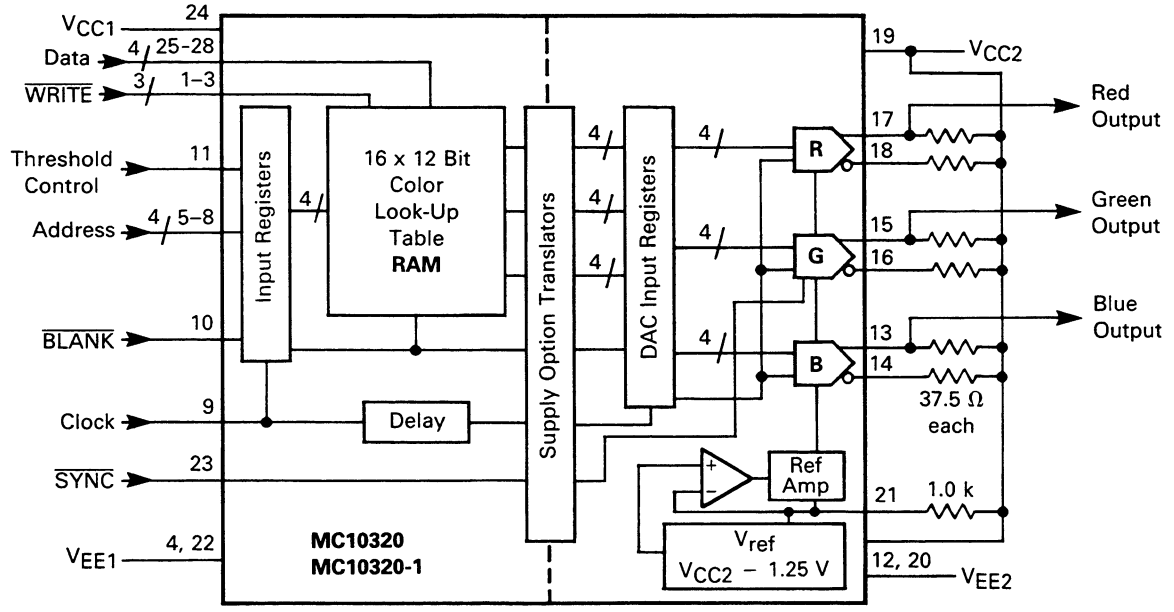
Parameter	Symbol	Min	Typ	Max	Units
READ Cycle (Display Mode)					
Address, $\overline{\text{BLANK}}$ Setup Time	t_{RSA}	—	1.5	—	ns
Address, $\overline{\text{BLANK}}$ Hold Time	t_{RHA}	—	1.5	—	ns
Clock Pulse Width — High	t_{PWH}	—	3.0	—	ns
Clock Pulse Width — Low	t_{PWL}	—	3.0	—	ns
Pipeline Delay	t_{PIPE}	1.0	1.0	1.0	clk cycle
DAC Prop Delay (P_{CLK} to 50% Point)	t_{DPD}	—	9.0	—	ns
DAC Prop Delay Difference (DAC to DAC)	$t_{DPD\Delta}$	—	0.5	—	ns
$\overline{\text{SYNC}}$ Prop Delay	t_{SPD}	—	6.0	—	ns
Output Settling Time (±1/2 LSB to ±1/2 LSB)	t_{DS}	—	3.0	—	ns
Output Slew Rate	SR	—	300	—	V/μs
Glitch Area	A_G	—	20	—	pV-S
WRITE Cycle (RAM Update Mode)					ns
Address Setup Time	t_{WSA}	—	1.5	—	
Address Hold Time	t_{WHA}	—	1.5	—	
Clock Setup Time	t_{WSC}	—	5.0	—	
Clock Hold Time	t_{WHC}	—	10	—	
Data Setup Time	t_{WSD}	—	90	—	
Data Hold Time	t_{WHD}	—	10	—	
Write Pulse Width	t_{WPW}	—	90	—	

TEMPERATURE CHARACTERISTICS (0°C to +70°C)

Parameter	Typ	Units
Offset (at Ref. White)	±20	ppm GS/°C
DAC Gain	±100	ppm GS/°C
Gain Tracking (any 2 DACs @ Ref. Black)	±50	ppm GS/°C
Linearity	±100	ppm GS/°C

Note: ppm GS/°C = Parts Per Million of Grey Scale/°C.

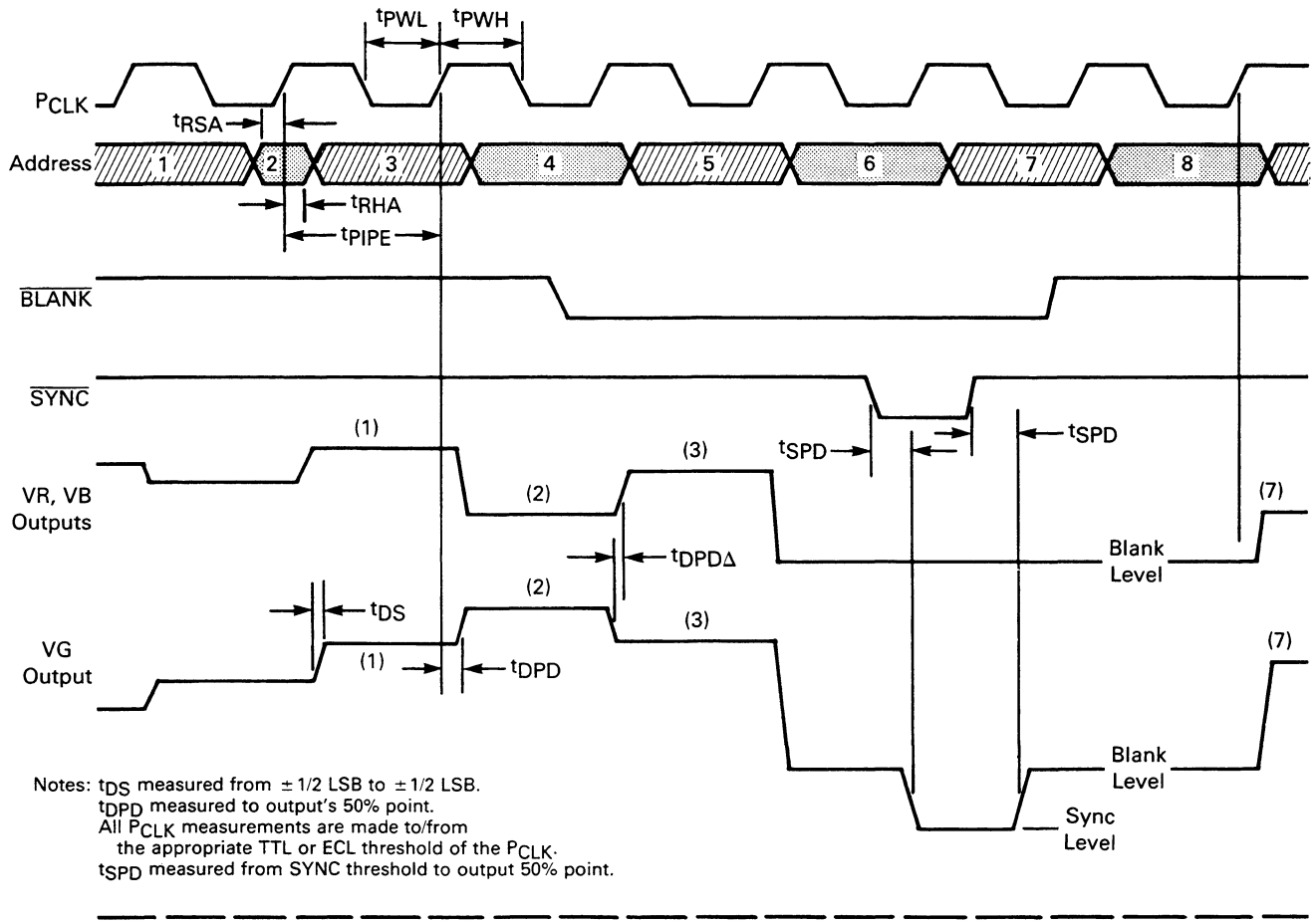
FIGURE 1 — BLOCK DIAGRAM



Note:
Electrical Characteristics are tested with both single and dual supply configurations at the typical supply voltages listed in the "Recommended Operating Limits." Input levels are TTL or ECL, as appropriate. Threshold control input is set at V_{CC1}, or V_{EE1}, as appropriate. Exceptions to these conditions are noted in the Characteristics.

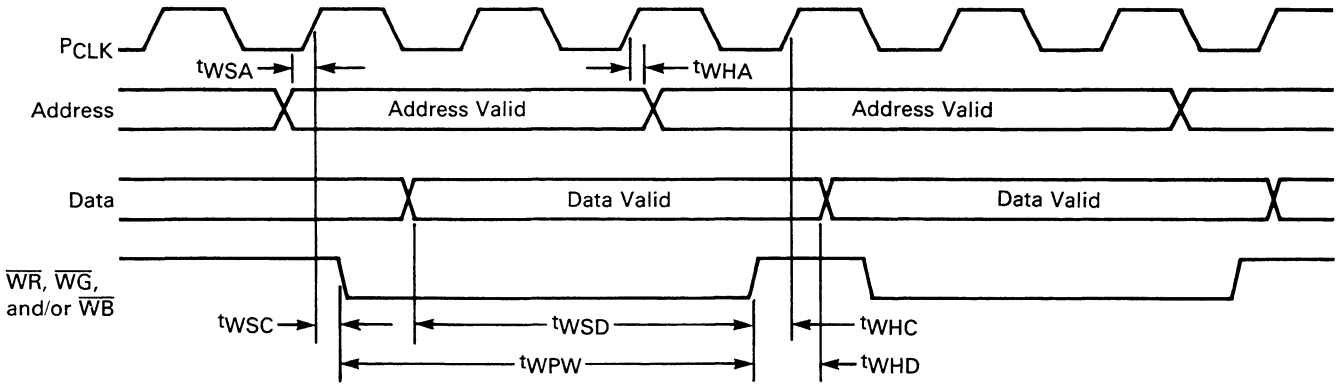
FIGURE 2 — TIMING DIAGRAM

READ CYCLE (PIXEL DISPLAY MODE)



Notes: t_{DS} measured from ±1/2 LSB to ±1/2 LSB.
t_{DPD} measured to output's 50% point.
All P_{CLK} measurements are made to/from the appropriate TTL or ECL threshold of the P_{CLK}.
t_{SPD} measured from SYNC threshold to output 50% point.

WRITE CYCLE (RAM UPDATE MODE)



PIN DESCRIPTIONS

Symbol	Pin	Description
$\overline{WR}$	1	Write Enable (Red) — Taking this pin low enables the data (Pins 25–28) to be written into the selected address location for the RED look-up table. The data is latched in the RAM when the pin is high.
$\overline{WG}$	2	Write Enable (Green) — Same as Pin 1, except for the GREEN table.
$\overline{WB}$	3	Write Enable (Blue) — Same as Pin 1, except for the BLUE table.
V_{EE1}	4	Power supply pin for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for V_{CC1}, and is typically 5.0 volts below it. Internally it is connected to Pin 22. This pin and Pin 22 **must** be connected externally for proper operation.
A0–A3	5–8	Address lines — They are used to select one of sixteen 12-bit words in the color look-up table for both reading and writing. The address is latched on the P_{CLK} rising edge, and presented to the DACs on the following rising edge. Pin 5 is A3 (MSB), and Pin 8 is A0 (LSB).
P_{CLK}	9	Pixel clock — Address and $\overline{BLANK}$ signals are latched on the rising edge of this clock. The following rising edge presents the data in the look-up table (of the selected address) to the DACs. $\overline{SYNC}$ is independent from P_{CLK}.
$\overline{BLANK}$	10	Blanking — A logic low overrides the color look-up table, and forces the three DACs to the blanking level. The $\overline{BLANK}$ input is latched, the same as the address lines.
ThCntl	11	Threshold Control — When tied to V_{CC1}, the P_{CLK}, A0–A3, and $\overline{BLANK}$ inputs are at ECL levels with respect to V_{CC1}. When tied to V_{EE1} (Pin 4 or 22), the same inputs are at TTL levels with respect to V_{EE1}.
V_{EE2}	12	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for V_{CC2}, and is typically 5.0 volts below it. It is internally connected to Pin 20. This pin and Pin 20 **must** be connected externally.
VB	13	The output of the BLUE 4-bit DAC. Output compliance is ±2.0 volts with respect to V_{CC2}, and output impedance is typically 100 kΩ. Designed for a typical load of 37.5 Ω, the load may be between 0 and 75 Ω. The output is a current sink.
$\overline{VB}$	14	The complementary output of the BLUE DAC. This output may be used in conjunction with Pin 13 for twisted pair signal transmission or for custom interface schemes. If unused, it must be tied to V_{CC2}.

PIN DESCRIPTIONS

Symbol	Pin	Description
VG	15	Same as Pin 13, except for the GREEN DAC. The SYNC signal appears at this output. Waveform polarity is "sync down."
$\overline{VG}$	16	Same as Pin 14, except for the GREEN DAC. The SYNC signal appears at this output. Waveform polarity is "sync up."
VR	17	Same as Pin 13, except for the RED DAC.
$\overline{VR}$	18	Same as Pin 14, except for the RED DAC.
V_{CC2}	19	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). Its reference is V_{EE2}, and is nominally 5.0 volts more positive than V_{EE2}.
V_{EE2}	20	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for V_{CC2}, and is typically 5.0 volts below it. It is internally connected to Pin 12. This pin and Pin 12 **must** be connected externally.
R_{SET}	21	Current setting resistor — A user supplied low inductance resistor is to be connected between V_{CC2} and this pin to set the DAC's full scale current. An R_{SET} of 1.0 kΩ, combined with load resistors of 37.5 Ω (at Pins 13, 15, 17) provides output signals consistent with EIA-343-A. The R_{SET} resistor is to be between 500 Ω to 2.0 kΩ. The voltage at this pin is 1.25 volts below V_{CC2}.
V_{EE1}	22	Power supply pin for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for V_{CC1}, and is typically 5.0 volts below it. Internally it is connected to Pin 4. This pin and Pin 4 **must** be connected externally for proper operation.
$\overline{SYNC}$	23	A logic low on this input forces the GREEN DAC to increase its output current by 7.6 mA (R_{SET} = 1.0 kΩ), providing the sync level of 286 mV (R_L = 37.5 Ω) below blanking. The $\overline{BLANK}$ input must have been asserted previously. $\overline{SYNC}$ is independent of P_{CLK}.
V_{CC1}	24	Power supply pin for the circuitry to the left of the supply option translators (See Block Diagram). Its reference is V_{EE1}, and is nominally 5.0 volts more positive than V_{EE1}.
D0–D3	25–28	Data inputs — Information on these pins is written into the color look-up table, at the locations specified by the address lines, by taking the appropriate Write pin low. Pin 28 is D0 (LSB), and Pin 25 is D3 (MSB).

FUNCTIONAL DESCRIPTION

GENERAL

The MC10320 is a triple video DAC, with a 16 location color palette RAM, designed for high resolution graphics systems. The maximum pixel speed capability is 125 MHz for the MC10320, and 90 MHz for the MC10320-1. The input configurations are compatible with TTL or ECL systems, and the outputs are directly compatible with monitors having 50 Ω or 75 Ω RGB inputs. Using the external components recommended in this data sheet, the outputs will conform to EIA-343-A levels. The output levels are adjustable by means of the R_{SET} resistor.

The MC10320 contains three 4-bit DACs whose inputs are fed from a color palette RAM (data is loaded by the user). The RAM contains 16 locations (each 12 bits wide). Each 4-bit nibble of each RAM address can be individually loaded, so that every address location can have any one of a possible 4096 codes. The DAC output levels are determined by the contents of the selected RAM address (by means of the address inputs).

The MC10320 contains an input register to accept the address and Blanking information, and a second register located between the RAM and the DAC inputs. This arrangement ensures that the RAM data is presented to the 3 DACs simultaneously, which ensures the DAC outputs will transition simultaneously. The registers are toggled by the P_{CLK} input's rising edge.

The $\overline{BLANK}$ input overrides the RAM data to the DACs, and forces the outputs to the Blanking level. The $\overline{SYNC}$ input goes directly to the Green DAC, bypassing the RAM and the latches, forcing the green DAC output to shift. The combination of $\overline{BLANK}$ and $\overline{SYNC}$ produce the video sync level.

Referring to the Block Diagram, the input stage (circuitry to the left of the Supply Option Translators) and the output stage (to the right of the Translators) can be operated at different supply voltages. The only restriction is that the output stage cannot be more positive than the input stage.

INPUTS

Address, P_{CLK}, $\overline{BLANK}$

The Address, P_{CLK} (pixel clock), and $\overline{BLANK}$ inputs are the "high speed" inputs capable of the maximum pixel clock rates mentioned above. The Address and $\overline{BLANK}$ are latched into the input register on the rising edge of the P_{CLK}, as long as the required setup and hold times are adhered to. The data at that RAM address (or the $\overline{BLANK}$ signal) is then presented to the DAC inputs on the next P_{CLK} rising edge.

The $\overline{BLANK}$ input, when taken to a Logic "0" and clocked in as described above, will override the RAM data presented to the DACs, and force the 3 DAC outputs to the Blanking level (see Figure 2).

These 6 input pins can accept either TTL or ECL signals. With the Threshold Control pin (Pin 11) connected to V_{EE1}, the inputs are TTL compatible with respect to V_{EE1}, having a nominal threshold of 1.5 volts above V_{EE1}, independent of V_{CC1}. With Pin 11 connected to V_{CC1}, the inputs are fully compatible with the 10KH family of ECL devices, having a nominal threshold of 1.3 volts below V_{CC1}, independent of V_{EE1}.

Figure 3 depicts a typical input stage configuration, and Figure 4 indicates the typical input current. Figure 4 applies to both ECL and TTL modes of operation. The inputs should be kept within the range of V_{EE1} to V_{CC1}. If an input is taken more than 0.3 volt below V_{EE1}, or more than 0.5 volts above V_{CC1}, excessive currents will flow through that input, and the DAC output waveforms will be distorted.

$\overline{SYNC}$

The $\overline{SYNC}$ input goes directly to the green DAC, independent of the clock. When taken to a Logic "0", the output current at VG is forced to increase by 6.1 x I_{SET}. For a standard EIA-343-A system, the shift is 7.63 mA, resulting in a 286 mV change in the output voltage. The $\overline{SYNC}$ input does **not** override the RAM data, requiring that the $\overline{BLANK}$ input have been asserted (Logic "0") previously in order to obtain a proper video sync level. The $\overline{SYNC}$ input does not affect the red or blue DACs.

The $\overline{SYNC}$ input is always TTL compatible, with a nominal threshold of 1.5 volts above V_{EE1}, independent of V_{CC1}.

Figure 3 depicts the input stage configuration, and Figure 4 indicates the typical input current. The input should be kept within the range of V_{EE1} to V_{CC1}. If the input is taken more than 0.3 volt below V_{EE1}, or more than 0.5 volts above V_{CC1}, excessive currents will flow through the input, and the DAC output waveforms will be distorted.

DATA (1–4), $\overline{WR}$, $\overline{WB}$, $\overline{WG}$

The data (D0, D1, D2, D3), and $\overline{WRITE}$ inputs are the "low speed" inputs, as they do not have to operate at the same high speed as the above mentioned inputs. These inputs are independent of the P_{CLK}, although they are normally used in conjunction with the clock.

Pins 25–28 are the data inputs to the color palette RAM, and are used for updating the RAM information. The information is written into the RAM at the address which was previously clocked into the input register, while the appropriate $\overline{WRITE}$ input is low, and then latched in when the $\overline{WRITE}$ input is taken high. The required data setup and hold times (mentioned in the Timing Characteristics) are with respect to the rising edge of the $\overline{WRITE}$ input. If the same data is to be loaded into different nibbles (color sections) of the same address, the appropriate $\overline{WRITE}$ inputs may be taken low simultaneously, or sequentially. $\overline{WR}$, $\overline{WB}$, and $\overline{WG}$ control the loading of data into the red, blue and green nibbles respectively.

The data and $\overline{WRITE}$ inputs are always TTL compatible, with a nominal threshold of 1.5 volts above V_{EE1}, independent of V_{CC1}.

In most applications, it will be advantageous to set the Blanking level while updating the RAM. If Blanking is not set, the DAC outputs will change unpredictably while new data is being written into the RAM.

Figure 3 depicts a typical input stage configuration, and Figure 4 indicates the typical input current. The inputs should be kept within the range of V_{EE1} to V_{CC1}. If an input is taken more than 0.3 volt below V_{EE1}, or more than 0.5 volts above V_{CC1}, excessive currents will flow through the input, and the DAC output waveforms will be distorted.

FIGURE 3 — TYPICAL INPUT STAGE

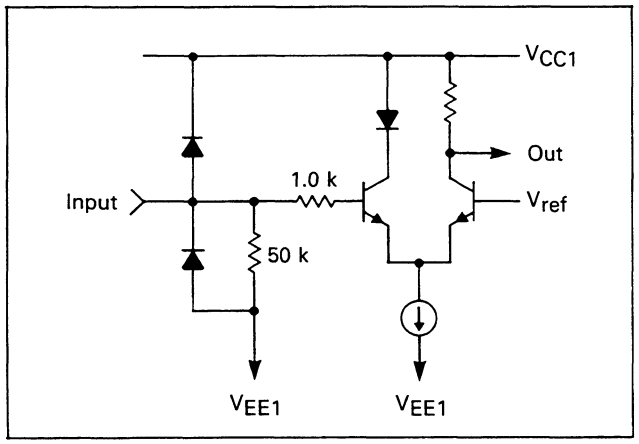
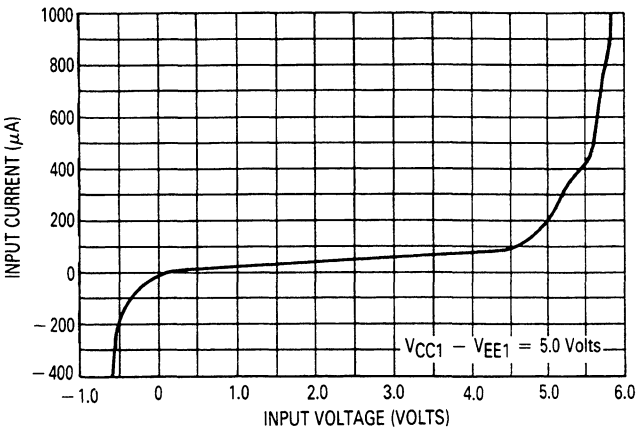


FIGURE 4 — INPUT CURRENT AT PINS 1–3, 5–10, 23, 25–28



THRESHOLD CONTROL

The Threshold Control input (Pin 11) is to be connected directly to V_{CC1} to set Pins 5–10 to ECL compatibility, or directly to V_{EE1} to set the pins to TTL compatibility. A series resistor should not be used with this input, and it should not be connected to any other voltage as an incorrect threshold will result at Pins 5–10. Bias current at Pin 11 is approximately 400 μA out of the pin when at V_{EE1}, and 0 μA when at V_{CC1}. If the pin is taken more than 0.3 volt below V_{EE1}, excessive currents will flow through this input, and the DAC output waveforms will be distorted.

OUTPUTS

The six DAC outputs (VB, $\overline{VB}$, VG, $\overline{VG}$, VR, $\overline{VR}$) at Pins 13–18 are high impedance current sink outputs, with the current flow **into** the pins, never out. VG, VB, and VR provide the conventional video polarity (sync down), while the complementary outputs provide a "sync up" waveform. The output loads must be connected from the outputs to V_{CC2}, or to a pullup voltage, such that the output voltages are within ±2.0 volts of V_{CC2}. Unused outputs **must** be connected to V_{CC2}, and not left open.

The output current (for the gray scale) at Pins 13, 15, and 17 is related to the digital inputs (of the DACs) and the reference current (I_{SET} at Pin 21, equal to 1.25 V/ R_{SET}) by the following equation:

$$I_{OUT(GS)} = \frac{(15\text{-}A) \times I_{SET} \times 14.63}{16} \qquad \text{(nominal value)}$$

where A = binary value of the digital input (0–15). A digital input of 1111 (15) produces no output current, and therefore the most positive output voltage, referred to as "Reference White." An input code of 0000 (0) results in the maximum current, and therefore the gray scale's most negative output voltage, referred to as "Reference Black."

After the $\overline{BLANK}$ input is asserted and clocked in as described above, the RAM data to the DACs is overriden, and the output current is set at:

$$I_{OUT(BLANK)} = I_{SET} \times 14.864 \qquad \text{(nominal value)}$$

When the $\overline{SYNC}$ input is asserted, the output current at VG is increased by:

$$\Delta I_{OUT(SYNC)} = I_{SET} \times 6.1 \qquad \text{(nominal value)}$$

The four outputs of the red and blue DACs are not affected by $\overline{SYNC}$. The current increase at VG results regardless of the digital input to the Green DAC. To obtain the correct (EIA-343-A) sync level, the $\overline{BLANK}$ output level must have previously been set. Otherwise the green output will simply shift by the above amount from the grey scale level in effect at the time the $\overline{SYNC}$ input was asserted. If both $\overline{BLANK}$ and $\overline{SYNC}$ are asserted, the output current at VG is:

$$I_{OUT(SYNC)} = I_{SET} \times 20.97 \qquad \text{(nominal value)}$$

The sum of the currents into each pair of outputs is a constant equal to [20.93 x I_{SET}] for the VG/$\overline{VG}$ pair, and [14.824 x I_{SET}] for the VR/$\overline{VR}$, and VB/$\overline{VB}$ pairs. Table 1 summarizes the above information.

The voltage levels generated at the outputs depend on the value of I_{SET} and the load impedance. An R_{SET} of 1.0 kΩ (I_{SET} = 1.25 mA), and a load of 37.5 Ω (doubly terminated 75 Ω system) at each output will generate the standard EIA-343-A levels. The output voltages must be kept within the range of +2.0 to −2.0 volts **with respect to V_{CC2}**. If any part of the output's waveform is outside this range, its linearity will be affected.

TABLE 1

Video Level	Output Current (mA) at:			
	VR, VB	VG	$\overline{VR}$, $\overline{VB}$	$\overline{VG}$
Gray Scale	$\left(\frac{(15\text{-}A) \times I_{SET}}{1.09}\right)$	Same as VB, VR	$\left(\frac{(A) \times I_{SET}}{1.09} + 1.06\ I_{SET}\right)$	$\left(\frac{(A) \times I_{SET}}{1.09} + 7.17\ I_{SET}\right)$
Blank	$I_{SET} \times 14.824$	Same as VB, VR	0 mA	$I_{SET} \times 6.1$
Sync + Blank	$I_{SET} \times 14.824$	$I_{SET} \times 20.93$	0 mA	0 mA

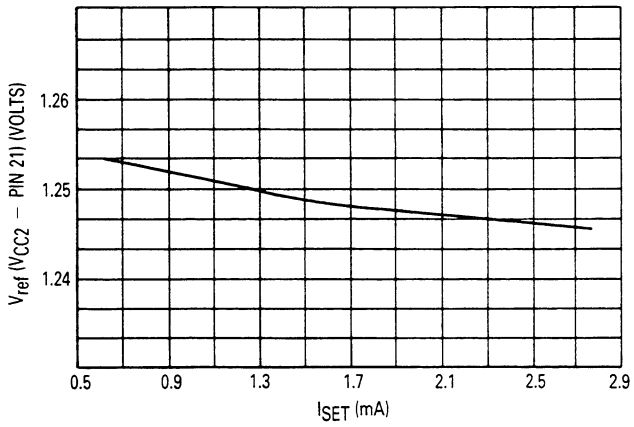
A = DAC digital input (binary value), I_{SET} is the current into Pin 21.

REFERENCE VOLTAGE (R_{SET})

The reference current for the DACs is supplied from an internal band-gap reference with a typical TC of ≈ ±50 ppm/°C. The voltage at R_{SET} (Pin 21) is a constant 1.25 volts below V_{CC2}, and an external resistor R_{SET} is to be connected from V_{CC2} to Pin 21. The current I_{SET} is therefore equal to 1.25 V/R_{SET}. Internally, equal reference currents are supplied to the three DACs such that their outputs are matched within ±3.0%.

R_{SET} should normally be between 500 Ω and 2.0 kΩ. With values less than 500 Ω, the current at Pin 21 approaches an upper limit, resulting in a nonlinear relationship for the MC10320. With values greater than 2.0 kΩ, instability and oscillations of the reference amplifier will result. For this reason, current to Pin 21 should not be supplied from a current source. Additionally, the resistor should be noninductive (non-wirewound). Metal film resistors, available with low TCs, are recommended. The resistor should be physically adjacent to the MC10320 to avoid the inductive effects of long PC board tracks. Figure 5 indicates the voltage/current characteristics at Pin 21.

FIGURE 5 — V_{ref} versus I_{SET}



POWER SUPPLIES

The MC10320 may be used in a single or dual supply system, depending on the system logic levels, and/or the output requirements (See the Applications Section). Table 2 indicates permissable configurations. The only restriction is that the output stage (V_{CC2}/V_{EE2}) cannot be more positive than the input stage. The positive supplies may range from +4.5 to +5.5 volts, and negative supplies may range from −4.5 to −5.72 volts.

TABLE 2

System	V_{CC1}	V_{EE1}	V_{CC2}	V_{EE2}
Single Supply	+5.0 V	Gnd	+5.0 V	Gnd
Single Supply	Gnd	−5.0 V	Gnd	−5.0 V
Dual Supply	+5.0 V	Gnd	Gnd	−5.0 V

The current requirement for the input stage (I_{CC1}) is typically 50 mA, and the majority of that current (+0, −4.0 mA) flows out of V_{EE1}. The current requirement for the output stage (I_{CC2}) is typically 28 mA. Out of V_{EE2} flows that current, plus the current due to the outputs and I_{SET}. In a typical application the output currents total ≈63 mA, and I_{SET} is ≈1.25 mA, giving a total I_{EE2} of ≈92 mA.

The minimum voltage at V_{CC1} for memory retention is ≈1.5 volts.

Proper bypassing of the supplies **at the IC** is critical due to the high frequencies involved. Further information can be found in the Applications section.

TIMING

Timing diagrams for the Read (display) mode and the Write (RAM update) mode are shown in Figure 2.

In the READ mode, the clock may be any frequency up to 125 MHz for the MC10320, and up to 90 MHz for the MC10320-1. Duty cycle is not important as long as the minimum low and high times are observed. On each clock's rising edge, a new address is clocked in, and the previous address' information is supplied to the DACs from the look-up table. If the $\overline{BLANK}$ line is taken to a Logic "0", it will override the information to the DACs on the next clock rising edge, and the 3 DACs will be taken to the blanking level. The $\overline{SYNC}$ input, when taken to a Logic "0", drives the Green DAC directly with only a small internal propagation delay. The output of the Green DAC will then change with respect to the last address input. For this reason, the $\overline{SYNC}$ input should normally be used only after asserting the $\overline{BLANK}$ input.

In the WRITE mode, the clock is used only to enter the address where the new data is to be written. The P_{CLK} input may continue to toggle if the address inputs are stable during the write period, or the clock may be stopped while writing. Data is then entered into each of 3 color sections of that address by taking low the appropriate WRITE lines ($\overline{WR}$, $\overline{WG}$, $\overline{WB}$). If the same four bits are to be stored in different color locations of the same address, the appropriate WRITE lines may be taken low simultaneously. If the $\overline{BLANK}$ input is held low during the Write operation, the DAC outputs will be held in a known state.

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device can result in an incorrect output due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10320 can cause incorrect operation if that noise does not have a clear path to ac ground.

The power supply pins at both the input and output sections of the MC10320 must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present among digital circuits) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the output waveforms can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7805.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10320.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10320 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10320 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC10320.

The two V_{EE1} pins (4 and 22) **must** be connected directly together. Likewise, the two V_{EE2} pins (12 and 20) **must** be connected directly together. Any long path between them can cause stability problems due to the inductance (@ 125 MHz) of the PC tracks. The ground return for the analog signals must be noise free.

PC Board Layout

Due to the high frequencies involved, and in particular, the fast edges of the various digital signals, proper PC board layout is imperative. A solid ground plane is necessary in order to have known transmission characteristics, and also to minimize coupling of the digital signals into the analog section. Use of wire wrapped boards should definitely be avoided.

Each PC track should be considered a transmission line, and if they are of any considerable length (more than a few inches), they should be terminated according to transmission line theory. Otherwise reflections back to the signal sources can occur, disrupting their operation. Additionally, the overshoots and undershoots which will occur at the MC10320's input pins can cause its operation to be disrupted, resulting in an incorrect output.

Additional information regarding the transmission characteristics of PC board tracks can be found in Motorola's MECL System Design Handbook (HB205R1).

Input Configurations

The unique configuration of the MC10320's power supply system permits its use in an all TTL, or all ECL, or mixed TTL/ECL environments, with the secondary capability of having the output levels be above or below ground. For standard TTL inputs refer to Figure 7. For systems using "above ground ECL" (ECL circuitry operated between ground and +5.0 volts, rather than −5.2 volts), refer to Figure 8. The MC10H350 translators will change the above ground ECL levels to the TTL levels required by the $\overline{\text{SYNC}}$, Data and $\overline{\text{WRITE}}$ inputs, while the Threshold Control will set the thresholds of the Address, Clock and $\overline{\text{BLANK}}$ inputs to the ECL levels. For standard (below ground) ECL levels, refer to Figure 9. Since V_{CC2} cannot be more positive than V_{CC1}, they are both connected to ground level in this case.

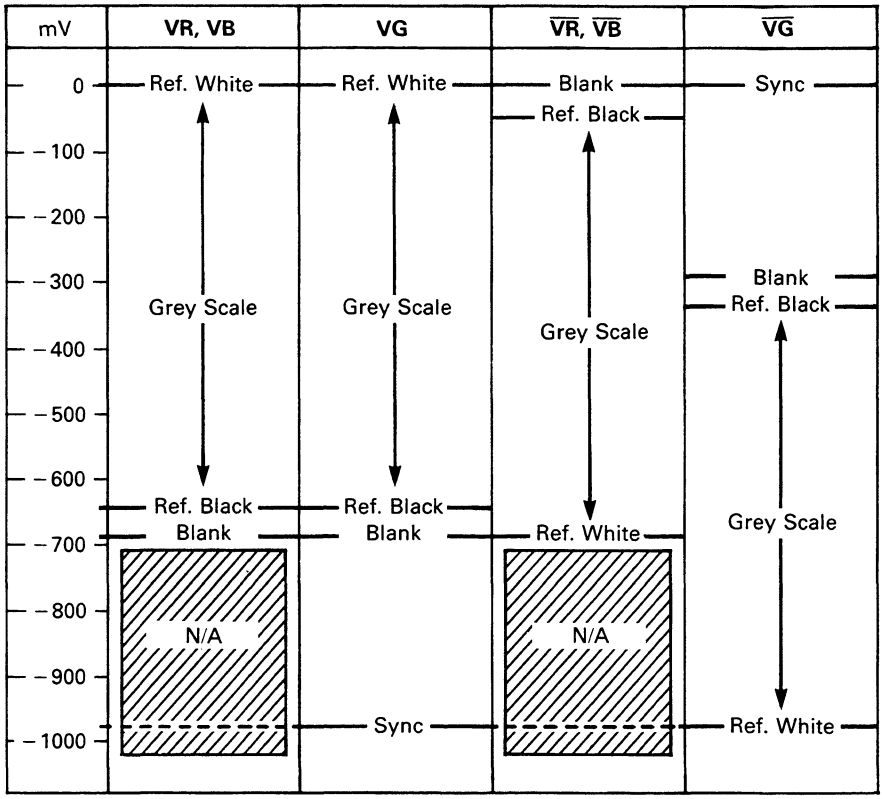
In the case where all inputs are above ground, but the low speed inputs (Data, $\overline{\text{WRITE}}$, and $\overline{\text{SYNC}}$) are connected to TTL circuits, while the high speed inputs are connected to above ground ECL circuits, refer to Figure 10. In the case where the low speed inputs are connected to standard TTL, and the high speed inputs are connected to standard (below ground) ECL, refer to Figure 11.

Output Configurations

The output waveforms may be above or below ground, depending on the choice of supply voltages for V_{CC2} and V_{EE2}, but the output voltages are always referenced to V_{CC2}. In Figure 12, the outputs are referenced to +5.0 V, and produce a 1.0 volt p-p waveform when used with a doubly terminated 75 Ω load, and an R_{SET} of 1.0 kΩ. The +5.0 volt supply is the "ac ground" in this case. If the outputs must be referenced to system ground rather than the +5.0 volt supply, the circuit of Figure 13 will provide the required level shifting. Figure 14 provides ground referenced outputs with a range of 0 to −1.0 volt. In Figure 15, the outputs are pulled up to a voltage different from V_{CC2}, providing an offset (+1.0 volt offset in the figure). In Figure 15 the complementary outputs should be connected to the +1.0 volt pullup voltage. The voltage at VR, VG, and VB (and the complementary outputs) must always lie within the range of ±2.0 volts with respect to V_{CC2}.

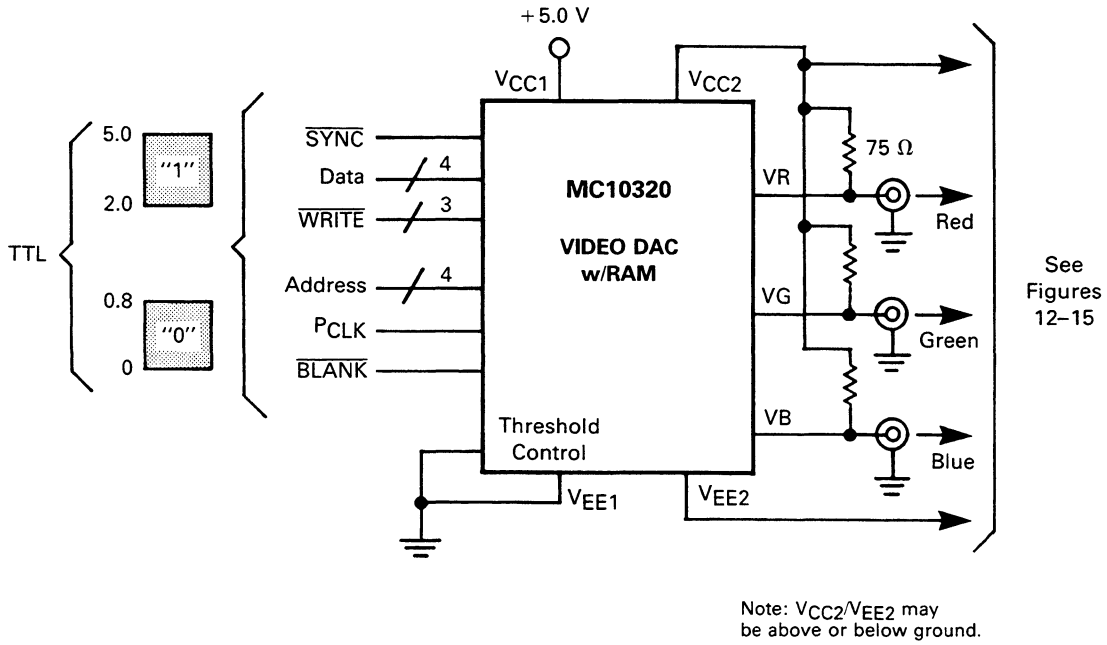
Figure 6 illustrates the output voltage range, with respect to V_{CC2} or a pullup voltage, of the six outputs (R_L = 37.5 Ω, R_{SET} = 1.0 kΩ):

FIGURE 6 — OUTPUT LEVELS



Note: R_{SET} = 1.0 k, R_L = 37.5 Ω, above values are typical.

FIGURE 7 — TTL INPUTS



Note: V_{CC2}/V_{EE2} may be above or below ground.

FIGURE 8 — ABOVE GROUND ECL INPUTS

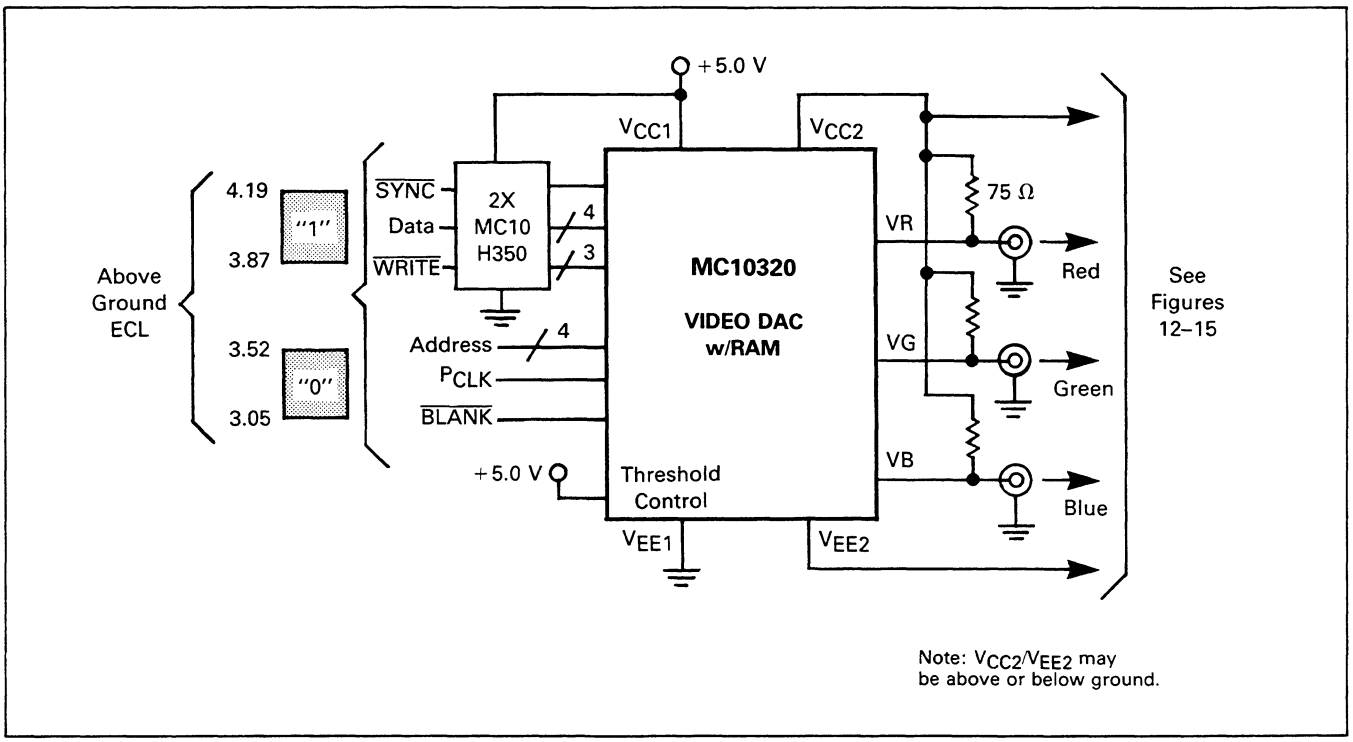


FIGURE 9 — STANDARD ECL INPUTS

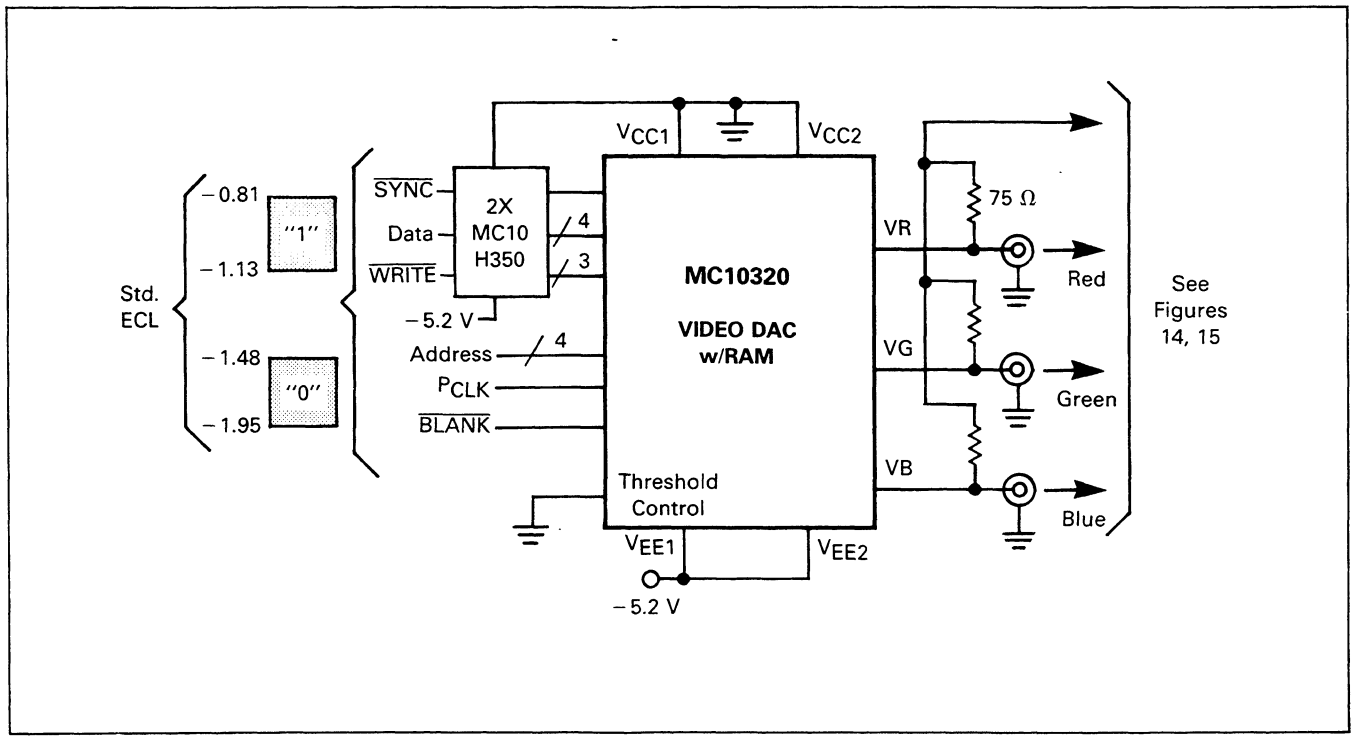


FIGURE 10 — LOW SPEED INPUTS @ TTL, HIGH SPEED INPUTS @ ABOVE GROUND ECL

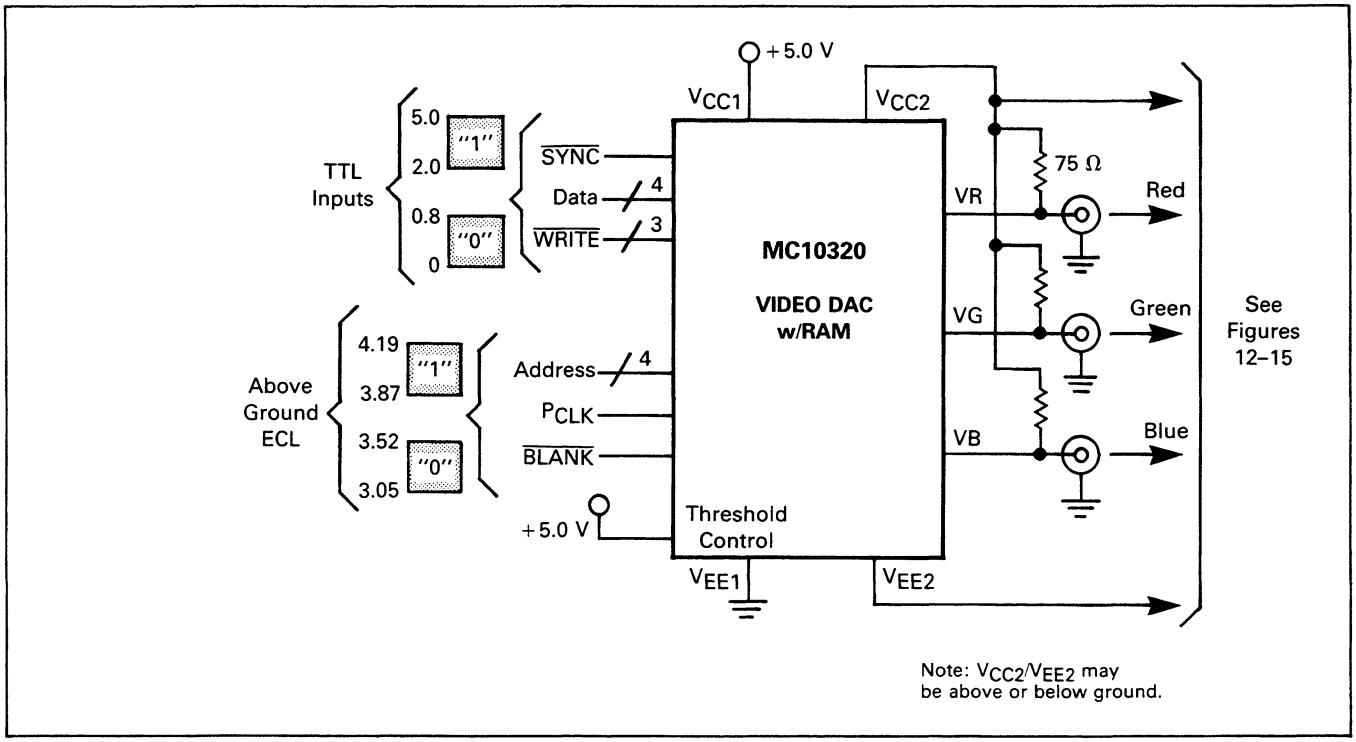


FIGURE 11 — LOW SPEED INPUTS @ TTL, HIGH SPEED INPUTS @ STANDARD ECL

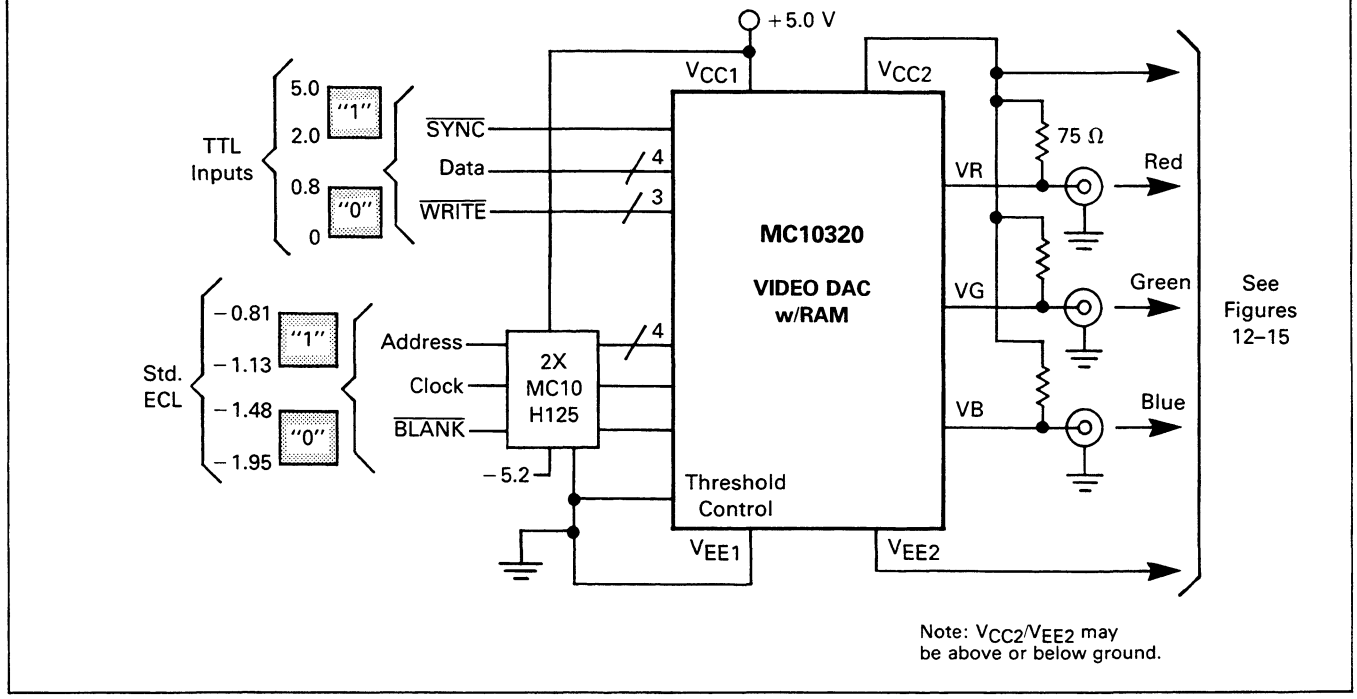


FIGURE 12 — SINGLE +5.0 VOLT SUPPLY, OUTPUTS ABOVE GROUND

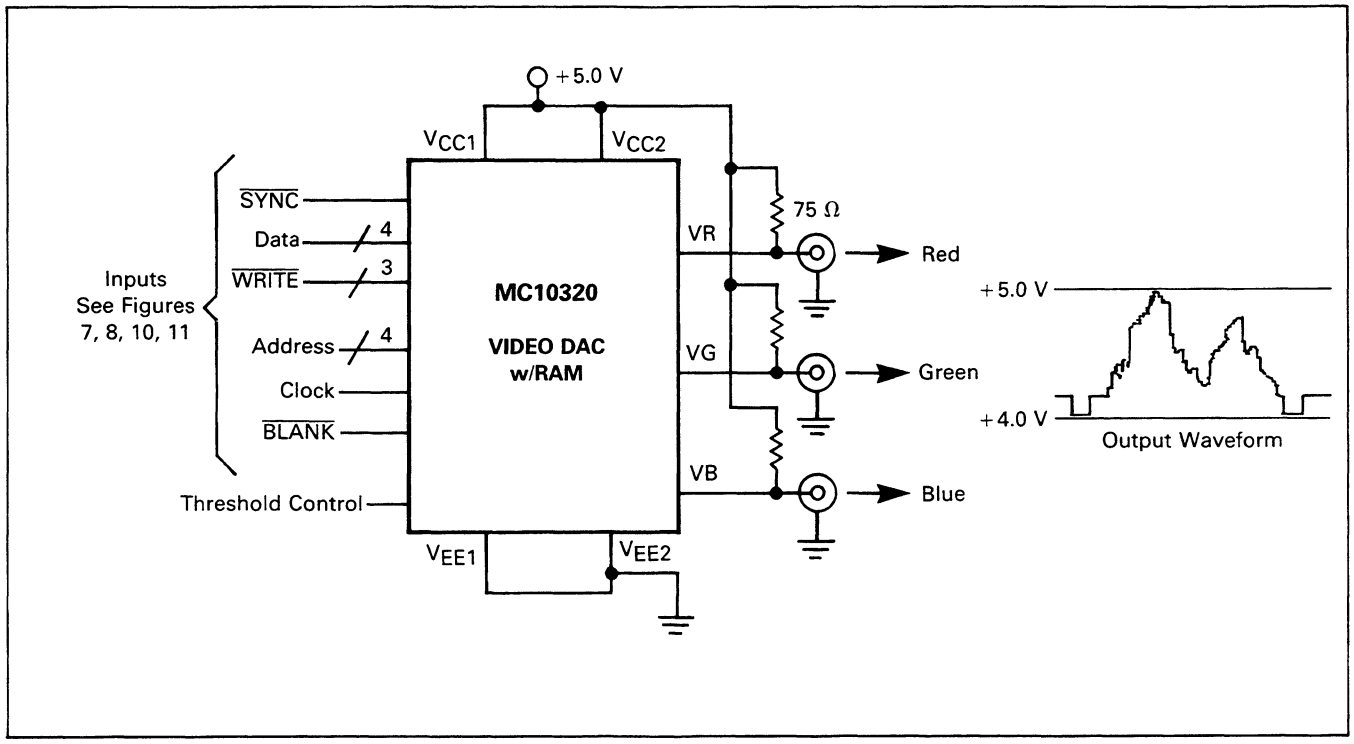


FIGURE 13 — SINGLE +5.0 VOLT SUPPLY, OUTPUTS REFERENCED TO GROUND

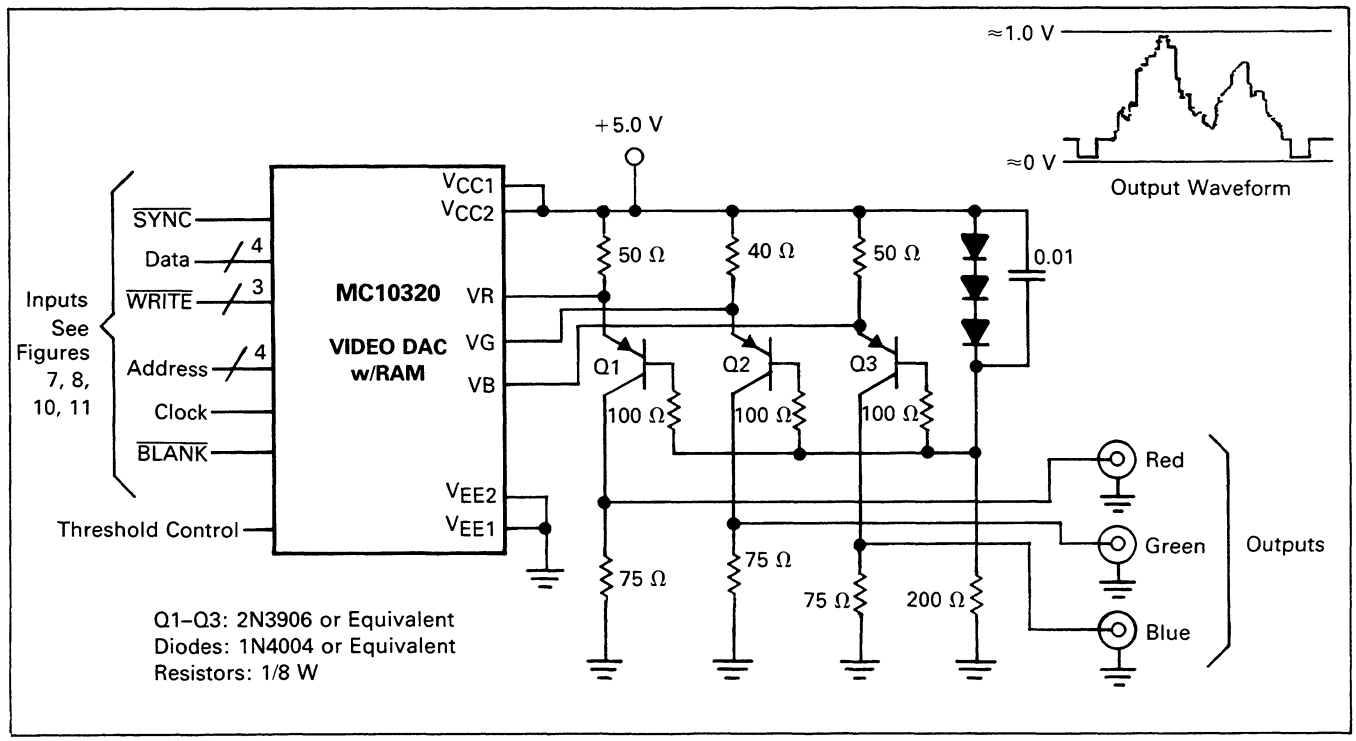


FIGURE 14 — SINGLE OR DUAL SUPPLY, OUTPUTS BELOW GROUND

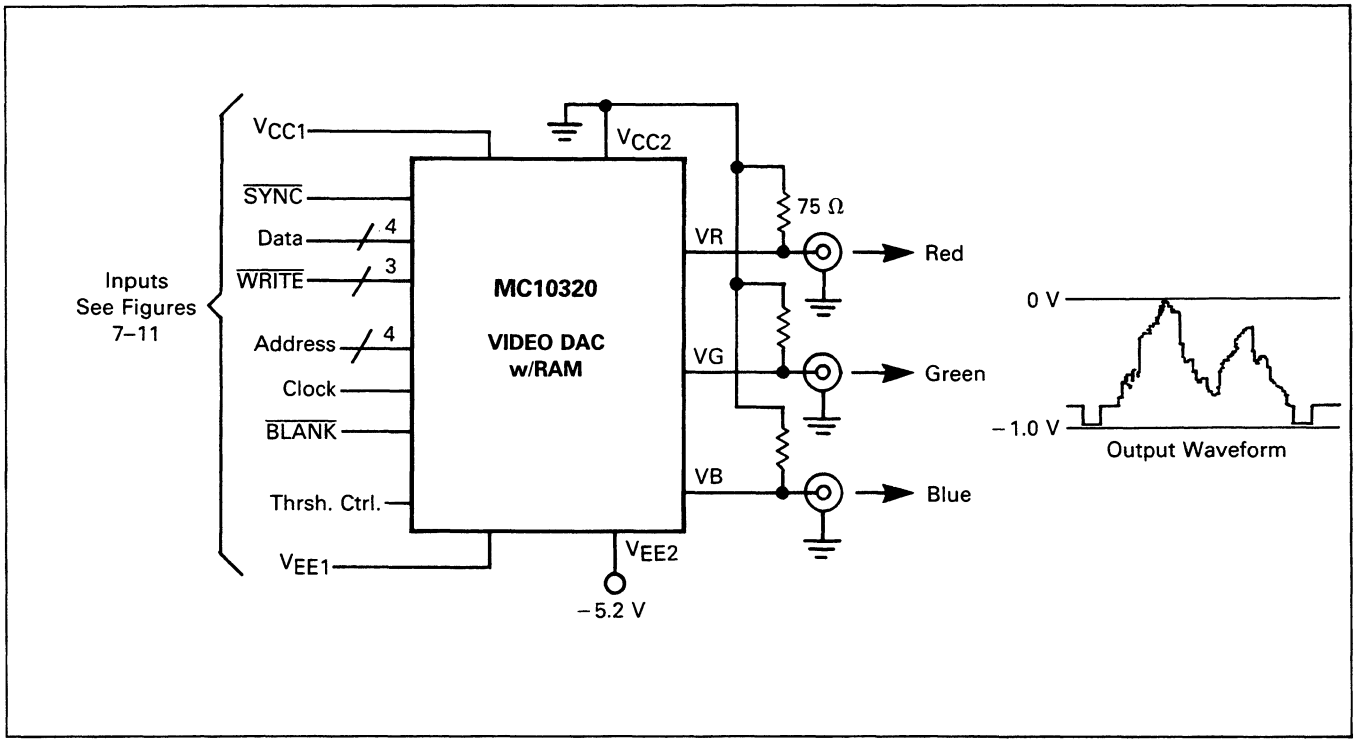
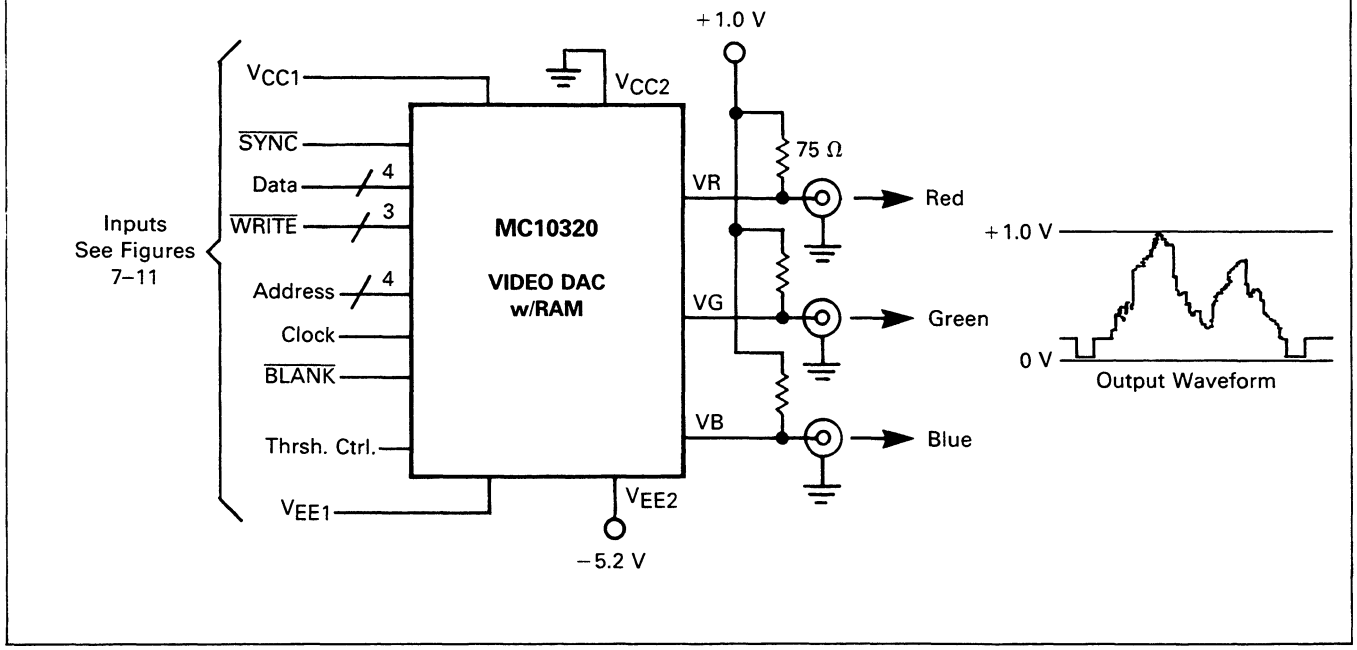


FIGURE 15 — SINGLE OR DUAL SUPPLY, OUTPUTS ABOVE GROUND, REFERENCED TO GROUND



GLOSSARY

BANDGAP REFERENCE — A temperature stable voltage reference circuit based on the predictable base-emitter voltage of a transistor.

BIPOLAR INPUT/OUTPUT — A mode of operation whereby the analog input (of an A/D), or output (of a DAC), includes both negative and positive values. Examples are −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

DAC CURRENT GAIN — The internal gain the DAC applied to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.

DIFFERENTIAL GAIN — In video systems, differential gain is a component's change in gain as a function of luminance level. In a color picture, saturation will be distorted if the differential gain is not zero.

DIFFERENTIAL NON-LINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n. This error must be within ±1 LSB for proper operation.

DIFFERENTIAL PHASE — In video systems, differential phase is the change in the phase modulation of the chrominance signal as a function of the luminance level. The hue in a color picture will be distorted if the differential phase is not zero.

ECL — Emitter coupled logic.

FULL SCALE RANGE (Actual) — The difference between the actual minimum and maximum end points of the analog input (of an A/D), or output (of a DAC).

FULL SCALE RANGE (Ideal) — The difference between the actual minimum and maximum end points of the analog input (of an A/D), or output (of a DAC), plus one LSB.

GAIN ERROR — The difference between the actual and theoretical gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

GLITCH AREA — The energy content of a glitch, specified in volt-seconds. It is the area under the curve of the glitch waveform.

GREY CODE — Also known as **reflected binary code,** it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NON-LINEARITY — The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing. Non-monotonicity occurs if the differential non-linearity exceeds −1 LSB.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative output voltage (of an DAC), while all ones corresponds to the most positive output.

OUTPUT COMPLIANCE — The maximum voltage range to which the DAC outputs can be subjected, and still meet all of the specifications.

POWER SUPPLY REJECTION RATIO — The ability of a device to reject noise and/or ripple on the power supply pins from appearing at the outputs. An ac measurement, this parameter is usually expressed in dB rejection.

POWER SUPPLY SENSITIVITY — The change in a data converters performance with changes in the power supply voltage(s). A dc measurement, this parameter is usually expressed in percent of full scale versus a percent change in the power supply voltage.

PROPAGATION DELAY — For a video DAC, the time from when the clock input crosses its threshold to when the DAC output(s) reach the 50% point of the transition.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

RESOLUTION — The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A/D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

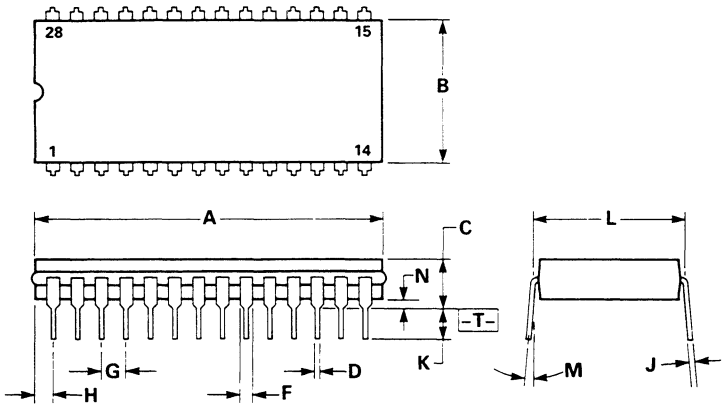
SETTLING TIME — For a video DAC, the time required for the output to change (and settle in) from an initial ±1/2 LSB error band to the final ±1/2 LSB error band.

TTL — Transistor-transistor logic.

TWO'S COMPLEMENT CODE — A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeroes, plus a carry. It is the same as Offset Binary Code, with the MSB inverted.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +10 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.

OUTLINE DIMENSIONS



L SUFFIX
CERAMIC PACKAGE
CASE 733-04

NOTES:
1. DIM [-A-] IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   [⌖] ϕ 0.25 (0.010) Ⓜ [T] [A] Ⓜ
3. [-T-] IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING & TOLERANCING PER Y14.5, 1982.
7. CONTROLLING DIM: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

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