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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC10318P

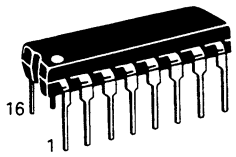
HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

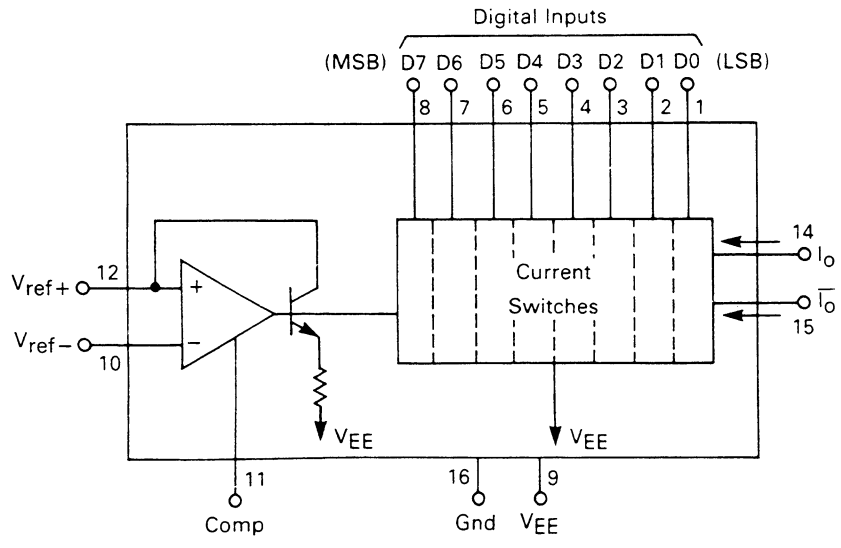
The MC10318 is a high-speed D/A converter capable of data conversion rates in excess of 25 MHz. The digital inputs are compatible with MECL 10,000 Series Logic. Complementary current outputs provide up to 56 mA full scale capability. The MC10318 is 8-bit accurate, and over temperature to meet the requirements of many applications, including: high-speed instrumentation and test equipment, storage oscilliscopes, display processing, radar systems, and digital video systems (broadcast and receiver applications).

- Fast Settling Time — 10 ns (Typ to ±0.19%)
- 8-Bit Accurate (0.19%)
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: −1.3 V to +2.5 V
- Single MECL Supply: −5.2 V
- Standard 16-Pin Dual-In-Line Package



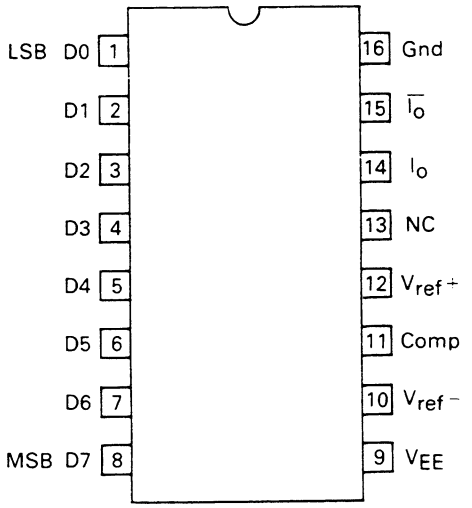
P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



PIN CONNECTIONS

(TOP VIEW)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{EE}	−6.0 to +0.5	Vdc
Digital Input Voltage	V_I	0 to V_{EE}	Vdc
Applied Output Voltage	V_O	+5.0 to V_{EE}	Vdc
Reference Current	$I_{ref}(12)$	5.0	mA
Output Current	I_{FS}	−75	mA
Reference Amplifier Input Range	V_{ref}	+0.5 to V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{ref}(D)$	±5.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+130	°C
Thermal Resistance, Junction to Ambient — Still Air With 500 LFPM	$R\theta_{JA}$	67 50	°C/W

DC CHARACTERISTICS (V_{EE} = −5.2 V, ±5% T_A = 0°C to +70°C after thermal equilibrium is reached.)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Nonlinearity (Integral) (Pin 14 or 15) (@ I_{FS} = 51 mA, 25.5 mA)		—	—	—	±0.19	%/FS
Zero Scale Output Current (Pin 14 or 15) (T_A = 25°C)	10	I_{ZS}	—	5.0	50	μA
Zero Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C 25°C < T_A < 70°C		$I_{ZS}/\Delta T$	 — —	 ±17 ±2.0	 — —	nA/°C
Full Scale Output Current (Pin 14 or 15) (I_{ref} = 3.2 mA, D0–D7 = 1)	10	I_{FS}	−46	−51	−56	mA
Full Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta I_{FS}/°C$	 — —	 ±50 ±10	 — —	ppm/°C
Full Scale Output Sensitivity to Power Supply Variations (Pin 14 or 15) (−4.94 V < V_{EE} < −5.46 V)		I_{FSPSS}	—	±0.005	±0.02	%/%
Full Scale Symmetry ($I_{FS} - \overline{I_{FS}}$)	10	I_{FSS}	—	±21	±100	μA
Output Voltage Compliance (Pin 14 or 15) Full Scale Current Change ≤ 1/2 LSB (Specified Nonlinearity) (T_A = 25°C)		V_{OC}	−1.3	—	+2.5	V
Output Resistance (Pin 14 or 15) (T_A = 25°C)	12	R_O	—	69	—	kΩ
Reference Amplifier Offset Voltage (T_A = 25°C)		V_{IO}	—	±3.2	—	mV
Reference Amplifier Offset Voltage Temperature Drift 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta V_{IO}/\Delta T$	 — —	 ±10 ±4.0	 — —	μV/°C
Reference Amplifier Bias Current (Pin 10) (I_{ref} = 3.2 mA)		I_{IB}	—	4.0	15	μA
Reference Amplifier Bias Current Temperature Drift (I_{ref} = 3.2 mA) 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta I_{IB}/\Delta T$	 — —	 −40 −10	 — —	nA/°C
Reference Amplifier Common Mode Range (V_{EE} = −5.2 V) (T_A = 25°C)		V_{ICR}	—	±1.15	—	V
Reference Amplifier Common Mode Rejection Ratio (T_A = 25°C) (I_{ref} = 3.2 mA, V_{ICR} = 0 to −2.0 V, Pins 1–8 = Logic 1)		V_{ICMRR}	—	58	—	dB
Reference Amplifier Input Impedance (Pin 10) (T_A = 25°C)		R_{IN}	—	1.0	—	MΩ
Power Supply Current (Pins 1 thru 8 Open, I_{ref} = 3.2 mA, Includes $I_O + \overline{I_O}$)		I_{EE}	—	90	130	mA

AC CHARACTERISTICS (T_A = 25°C, V_{EE} = −5.2 V, ±5%)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Feedthrough Current — All Bits Off	9	I_{FC}				μA p-p
f = 10 kHz			—	2.0	—	
f = 100 kHz			—	18	—	
Distortion — (@ I_O)						%
(Sinewave applied to reference amplifier Input, D0–D7 = Logic 1)						
C = 0.01 μF, f = 20 kHz		THD	—	1.0	—	
C = 0.01 μF, f = 65 kHz		THD	—	5.0	—	
C = 0.001 μF, f = 340 kHz		THD	—	1.0	—	
C = 0.001 μF, f = 600 kHz		THD	—	2.0	—	
C = 240 pF, f = 600 kHz		THD	—	0.8	—	
Reference Amplifier Slew Rate (Step change at Pin 10, all bits on)	13					mA/μs
C = 0.01 μF			—	0.5	—	
C = 0.001 μF			—	5.0	—	
C = 240 pF			—	20	—	
Settling Time (to ±0.19% of Full Scale)	1,22	t_s				ns
1 LSB Change			—	7.0	—	
All Bits Switched			—	10	—	
Propagation Delay	2	t_p	—	5.0	—	ns
Output Glitch Energy (with De-Skewing Capacitors) (Input Change: 01111111 ⟷ 10000000)			—	50	—	LSB-ns
Glitch Duration			—	5.0	—	ns

DIGITAL INPUT VOLTAGE LEVELS				
Volts (See Note)				
T_A	V_{IH}max	V_{IHA}min	V_{ILA}max	V_{IL}min
0°C	−0.845	−1.151	−1.516	−1.868
25°C	−0.810	−1.105	−1.505	−1.850
70°C	−0.727	−1.052	−1.480	−1.830

FUNCTIONAL PIN DESCRIPTION

D0–D7 (Pins 1-8) The eight ECL digital inputs compatible with MECL 10,000 series devices. Logic "0" is nominally −1.8 V, and Logic "1" is nominally −0.9 V.

V_{ref-} (Pin 10) The high impendance input of the reference amplifier. This input is normally grounded, but may be used for ac applications involving modulation, digitally controlled gain, etc. Normal operating range is from ground to V_{EE} + 2.9 V (nominally −2.3 V).

V_{ref+} (Pin 12) The noninverting input of the reference amplifier. The inverted output of the reference amplifier is internally fed back to this input, thus causing it to track Pin 10. A nominal 3.2 mA is to be supplied to this pin from an external (stable and noise free) voltage source and current setting resistor.

Comp. (Pin 11) A nominal 0.01 μF capacitor is connected to this pin and to ground to stabilize the reference amplifier. Lower values of capacitor may be used if a good PC board layout is used, where frequencies higher than 10 kHz are applied to the reference amplifier.

I_O, $\overline{I_O}$ (Pins 14,15) The complementary current outputs. Current flow is into the DAC and varies linearily with I_{ref} and the digital input code. I_{out} increases as the digital input increases. Output compliance range is −1.3 V to +2.5 V.

V_{EE} (Pin 9) The power supply pin. V_{EE} is nominal −5.2 V, ±5%.

Gnd (Pin 16) The ground pin. This line should be as noise-free as possible in order to obtain a noise-free output.

NOTE: V_{EE} = −5.2 V, ±5% Inputs are MECL 10,000 compatible within the temperature and power supply ranges listed. See MECL System Design Handbook for further details. See Fig 19 in this data sheet.

FIGURE 1 — SETTLING TIME

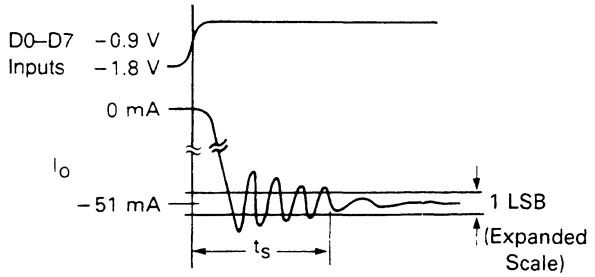
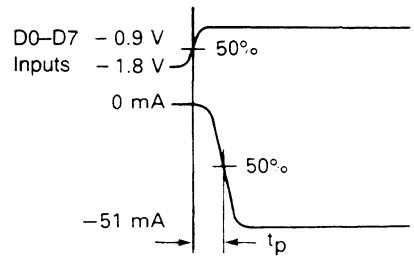


FIGURE 2 — PROPAGATION DELAY



REFERENCE AMPLIFIER RESPONSE

Inverting Input (V_{ref_-})
Test Circuit of Fig. 14

Noninverting Input (V_{ref_+})
Test Circuit of Fig. 11

FIGURE 3 — FREQUENCY RESPONSE

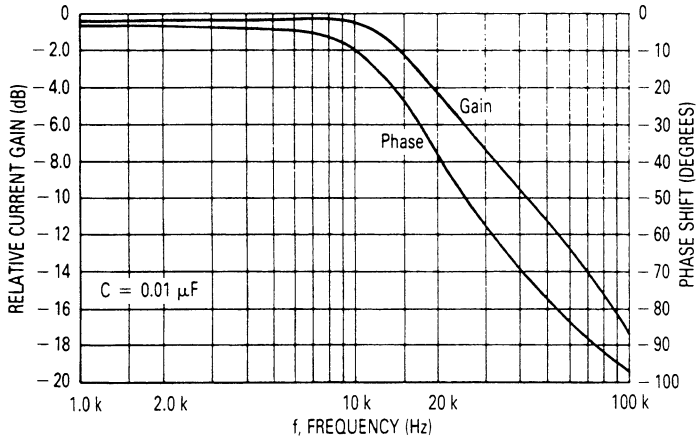


FIGURE 4 — FREQUENCY RESPONSE

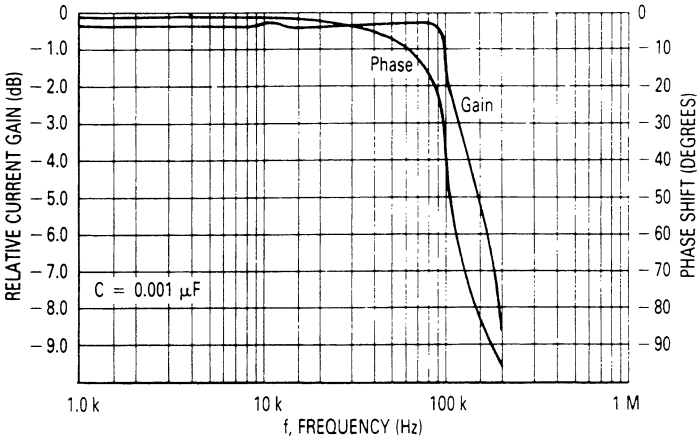


FIGURE 5 — FREQUENCY RESPONSE

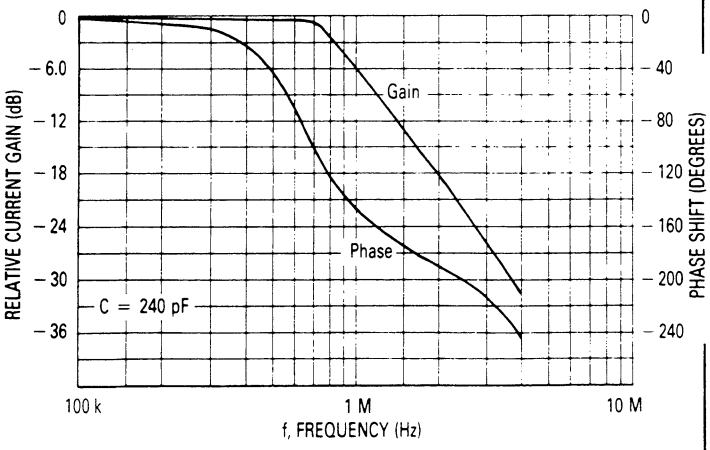


FIGURE 6 — FREQUENCY RESPONSE

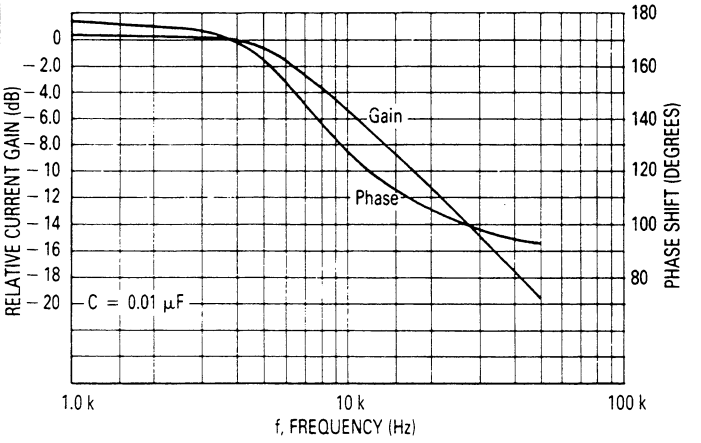


FIGURE 7 — FREQUENCY RESPONSE

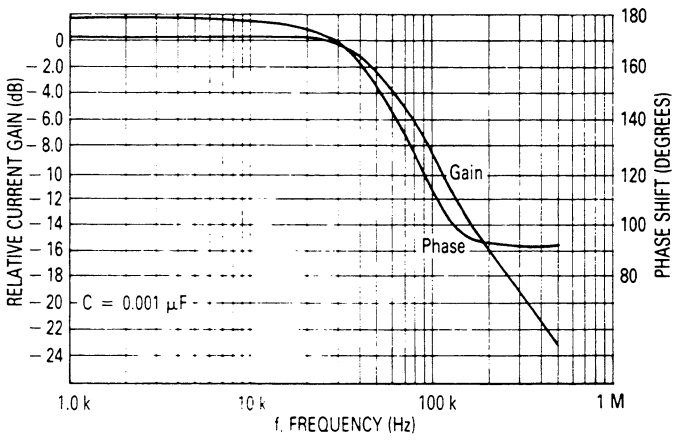
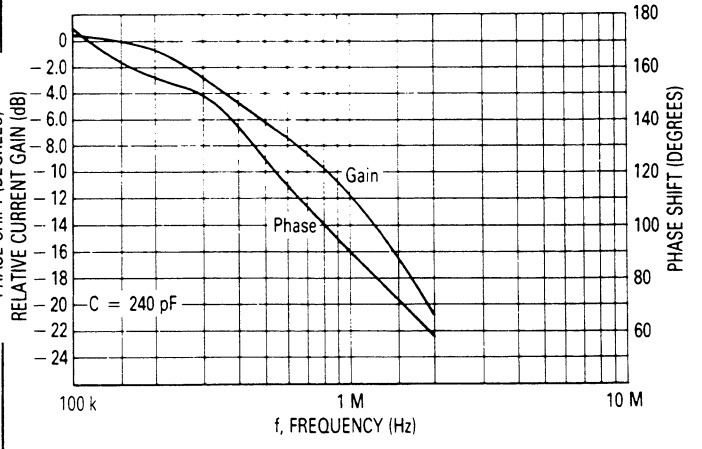
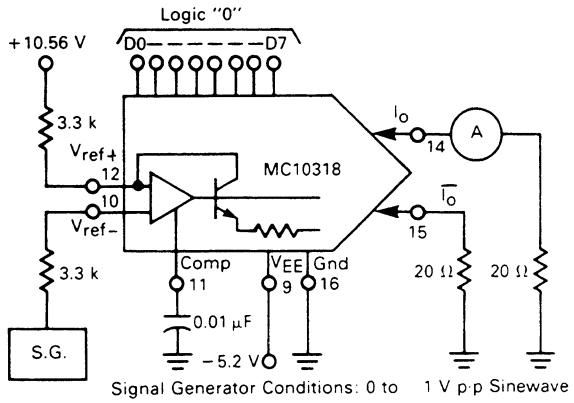


FIGURE 8 — FREQUENCY RESPONSE



TEST CIRCUITS

FIGURE 9 — FEEDTHROUGH MEASUREMENT



Signal Generator Conditions: 0 to 1 V p-p Sinewave

FIGURE 10 — ZERO/FULL SCALE CURRENT

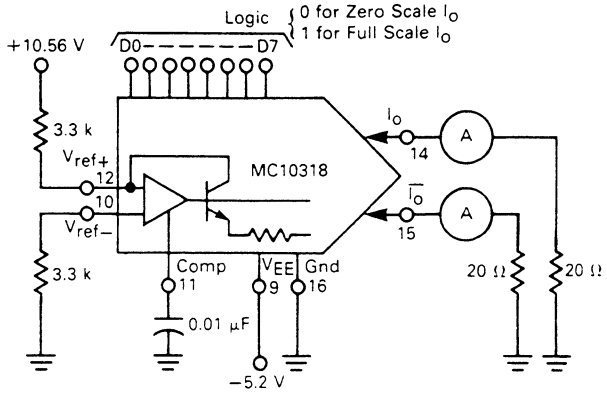
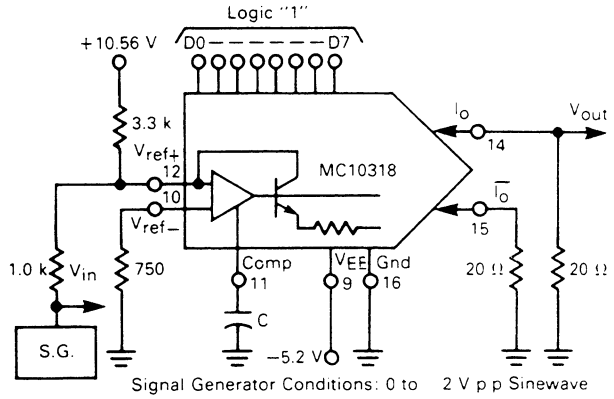


FIGURE 11 — GAIN/PHASE MEASUREMENT



Signal Generator Conditions: 0 to 2 V p-p Sinewave

Reference dB Level: See Text

See Figures 6–8

FIGURE 12 — OUTPUT RESISTANCE

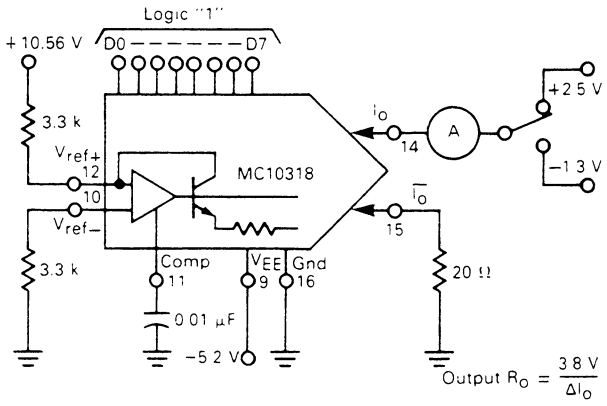
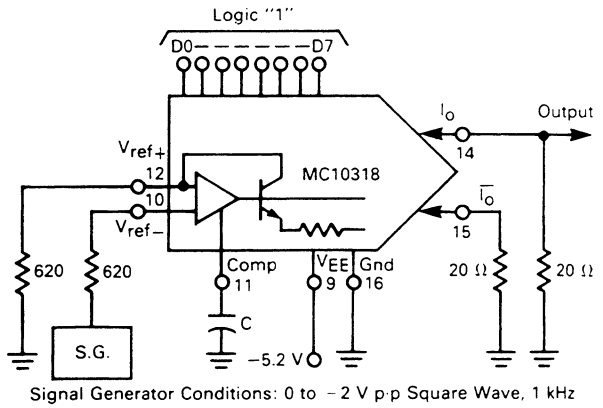
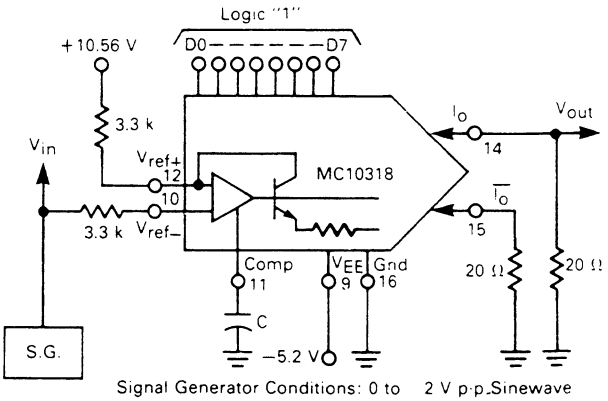


FIGURE 13 — REFERENCE AMPLIFIER SLEW RATE



Signal Generator Conditions: 0 to –2 V p-p Square Wave, 1 kHz

FIGURE 14 — GAIN/PHASE MEASUREMENT



Signal Generator Conditions: 0 to 2 V p-p Sinewave

Reference dB Level: See Text

See Figures 3–5

OPERATIONAL INFORMATION

Typical DAC Operation

The MC10318 is designed to be operated with an I_{ref} (Pin 12) of 3.2 mA, resulting in a full scale output current (I_O) of 51 mA when D0 through D7 are at a Logical "1" (−0.9 V). The transfer equation for I_O is therefore:

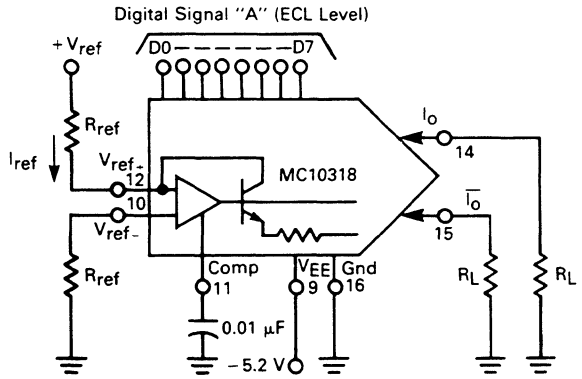
$$I_O = I_{ref} \times 16 \times \frac{A}{256}$$

("A" is the binary value of the digital input).

Typically V_{ref+} (Pin 10) is connected to Ground, and I_{ref} is supplied to V_{ref-} (Pin 12) by means of an external supply V_r (see Figure 15). A resistor inserted between Pin 10 and Ground will minimize temperature drift, and should have a value equivalent to that connected to Pin 12. Any noise or ripple present on the reference current will be present on the output current, and the stability of the reference directly affects the output current's stability. The ground connection for V_{ref+} should be chosen with care so as not to pick up noise (digital or otherwise).

The complementary outputs (I_O and $\overline{I_O}$) are high impedance current sources having a compliance range of 3.8 V (−1.3 to +2.5 V). I_O increases with increasing digital input, while $\overline{I_O}$ decreases. Their sum is a constant equal to 15.94 x I_{ref}. Neither output can be left open — an unused output must be connected to ground or a load resistor. Typically both outputs should be loaded similarly for best speed and accuracy performance. A compensation capacitor must be connected between Pin 11 and Ground to stabilize the amplifier. A 0.01 μF ceramic is satisfactory for most applications, and should be located physically close to the device. The ground side of the capacitor should be noise-free. When operated as above, the output(s) will be controlled by the digital inputs, and the MC10318 can be used for various functions such as waveform generation, process control, ADC conversion, and others.

FIGURE 15 — TYPICAL OPERATION



Common Mode Range — AC Operation

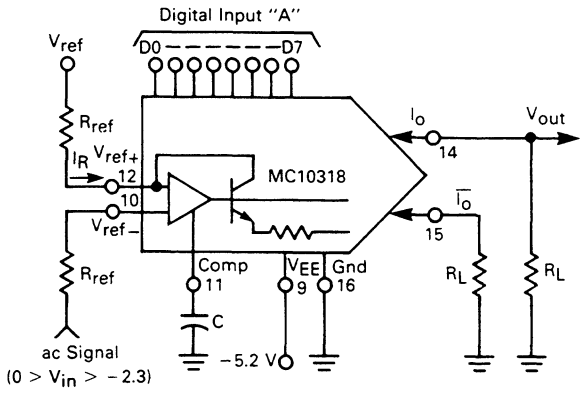
The reference amplifier inputs (Pins 10 and 12) may be used to control the output current in conjunction with the digital inputs for applications such as digitally controlled gain of an ac signal, digitally controlled amplitude modulation, and others. Either the positive or negative input of the reference amplifier may be used, depending on the application. There are, however, differences in the manner in which an ac signal is to be applied.

1) When applying a signal to the V_{ref-} (Pin 10) input (See Figure 16), the signal must be kept within the range of 0 to −2.3 V. The input has a high impedance (typically 1 Megohm). The V_{ref-} pin (Pin 12) will track this signal, causing I_{ref} to vary, in turn causing I_O and $\overline{I_O}$ to vary. The ac component of I_O (and $\overline{I_O}$) will be in phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A \times R_L}{16 \times R_R}$$

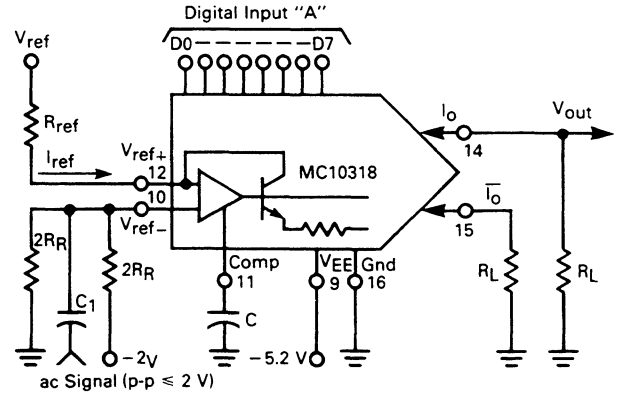
Applying the above to the test circuit of Figure 14 yields a gain of 0.0966, which is the 0 dB reference level for the curves of Figures 3–5.

FIGURE 16 — AC OPERATION, NONINVERTING



If the peak values of the applied ac signal cannot be kept within the above mentioned voltage range, an alternate circuit is shown in Figure 17.

FIGURE 17 — AC OPERATION, NONINVERTING (ALTERNATE)



The compensation capacitor (Pin 11) of Figures 16 and 17 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 10 kHz are to be applied to the reference input, a smaller value capacitor will be necessary as indicated by Figures 3–5. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

2) When applying a signal to the V_{ref} (Pin 12) input (see Figure 18), the effect is a direct modulation of the reference current supplied by V_{ref}. Pin 12 is a virtual ground, and therefore the current I_{ref} is equal to:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} + \frac{V_i}{R_i}$$

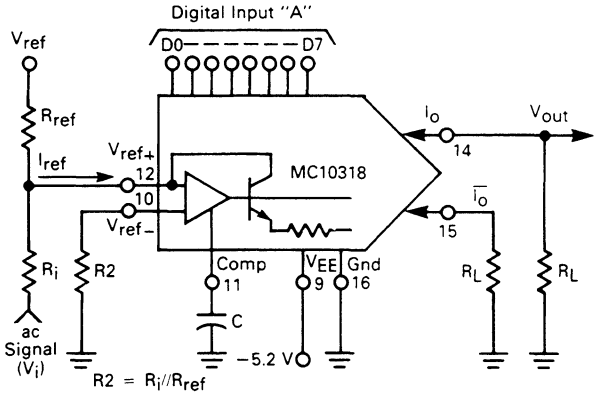
I_O and $\overline{I_O}$ will vary with the reference current, but the ac component will be 180° out of phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_i} = \frac{-A \times R_L}{16 \times R_i}$$

Applying the above to the test circuit of Figure 11 yields a gain of −0.3188, which is the 0 dB reference level for the curves of Figures 6–8.

The reference current I_{ref} must always flow **into** Pin 12, requiring that the values of V_{ref}, R_{ref}, R_i, and V_i be chosen so as to guarantee this.

FIGURE 18 — AC OPERATION, INVERTING

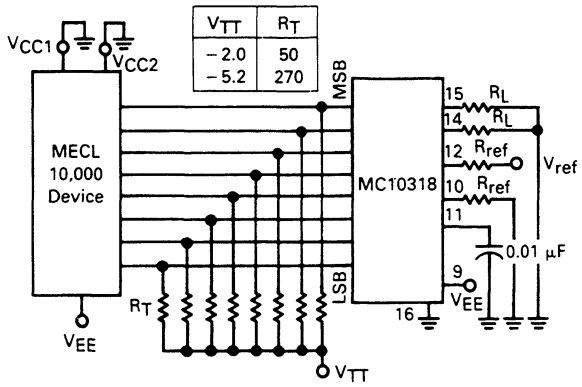


The compensation capacitor (Pin 11) of Figure 18 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 4 kHz are to be applied, a smaller value capacitor will be necessary as indicated by Figures 6–8. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

DIGITAL INTERFACE

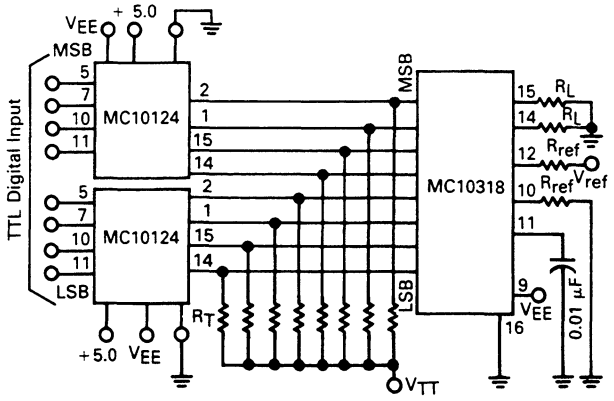
The digital inputs (Pins 1–8) are compatible with MECL 10,000 series devices over the temperature and V_{EE} range listed on page 3. Standard MECL 10,000 design guidelines apply, and should be implemented. Maximum speed response requires careful PC board layout and choice of components. See Motorola's MECL System Design Handbook for a complete explanation of specifications and characteristics. Figure 19 shows a typical ECL interconnection with recommended values for optimum speed performance. Other values of R_T and V_{TT} may be used, but at a slight increase in overall propagation delay. Unused inputs should not be left open, but should be connected to a Logic 0 (−1.8 V), or a Logic 1 (−0.9 V). Resistors R_T should be connected at the receiving end of the interconnection, i.e. physically located adjacent to the MC10318 inputs, for best speed performance.

FIGURE 19 — STANDARD MECL INTERFACE



Interfacing a TTL system to the MC10318 is easily accomplished by the use of two MC10124 devices (see Figure 20).

FIGURE 20 — TTL INTERFACE



OUTPUT CHARACTERISTICS

The MC10318 DAC has been designed specifically for high speed operation by incorporating ECL structured inputs, bit switching circuits which are small in size and

simple in operation, and high-current complementary outputs (which permits current steering rather than on-off switching). In this manner, very short propagation delays and settling times are possible.

Output Glitch

All DAC's will produce a glitch at the output when various bits are switched in opposite directions, due to differences in transition times of the switching transistors. During the switching period, typically the output current will momentarily seek a value other than the desired final value, and then return to and settle at the final value. This glitch can be several LSBs in magnitude, but of a very short duration (5–6 ns). In some instances, the output current may overshoot, and then undershoot before reaching the final value, resulting in a "glitch doublet."

The glitch is most apparent when switching the higher order bits, and in the case of the MC10318, the maximum glitch generally occurs when switching bit D5 and the lower 5 bits (typically 85 LSB·ns). Switching bit D6 and the lower 6 bits produces a similar but slightly reduced glitch. Switching bit D7 and the seven lower bits (major carry transition) results in a glitch of typically 50 LSB·ns, with an amplitude of 17 LSBs. Switching of lower order bits while maintaining the higher ones constant produces glitches typically of less than 1 LSB in magnitude, and less than 10 ns in duration, and are generally not considered to be of significance.

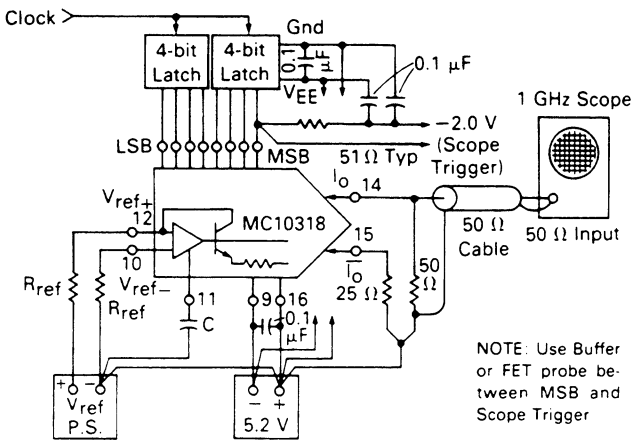
Glitches can be removed from the output by filtering, or by using a sample-and-hold circuit on the output, or by using de-skewing capacitors on the higher order bits.

Output glitch is generally specified in terms of glitch energy, which is the area under the curve of the waveform. Most glitches appear as a triangle, and so the area is simply ½ × t × ΔI, where t is the duration of the glitch, and ΔI is the amplitude normalized in terms of LSBs. In the case of a glitch doublet, having both positive and negative amplitude, the areas are summed algebraically. It is possible, therefore to have a glitch with zero energy, although having amplitudes of several LSB's.

In applications where the output glitch is of concern, steps can be taken to minimize its magnitude. The two main factors to consider are: 1) That the 8 bits of data reach the MC10318 simultaneously; and 2) that the PC board layout prevent noise from reaching the MC10318.

It is obvious that if the updated 8 bits are not received by the DAC simultaneously, even an ideal DAC will not produce an ideal waveform. Where simultaneous transmission by the sending device(s) cannot be guaranteed (such as two cascaded counters), latches should be used ahead of the MC10318. The latches should then be clocked after their inputs have settled. Suggested latches are the MC10133/MC10153/MC10168 at the ECL level, and the SN74LS273 at the TTL level.

FIGURE 21 — PRECISION HIGH-SPEED MEASUREMENTS



Nonlinearity

Integral nonlinearity has been specified, rather than differential nonlinearity, as this is a better indicator of the maximum error to be expected. Integral nonlinearity is measured by comparing the **actual** output (at each digital value) with the expected ideal value. The expected values lie along a straight line between zero and the full scale output current. The MC10318 will not differ from the **ideal** value by more than the specified nonlinearity.

PC Board Layout

A proper PC board layout is very important in order to obtain the full benefits of the MC10318's high-speed characteristics. Each of the current paths (I_O, $\overline{I_O}$, I_{EE}, I_{ref}, etc.) must be carefully considered to avoid interference, and isolation from other circuits on the board (particularly digital) is essential. Bypassing of all supplies is, of course, necessary, and in some cases, bypassing to V_{EE} may be more beneficial than bypassing to Ground. Sockets should be avoided as the extra pin-to-pin capacitance can slow down the ECL edges and/or the output settling time. PC board layout should include the following guidelines:

1) A dedicated ground track from the power supply to Pin 16 (Gnd);
2) A single dedicated ground track from the power supply to the **two** load resistors associated with I_O and $\overline{I_O}$ — this results in a constant dc current in this track;
3) A separate ground for the circuitry associated with V_{ref-}, V_{ref+}, and Comp (Pins 10–12). Any noise on this ground will feed through the reference amplifier and show up on the output;
4) The compensation capacitor must be physically adjacent to Pin 11;
5) Bypass V_{EE} (Pin 9) with a 0.1 μF to the ground line feeding the load resistors;
6) Provide proper terminations at the inputs — the suggested values for R_T and V_{TT} will provide best speed response;

7) Bypass V_{TT} to V_{EE} **and** to Ground with 0.1 μF capacitors;
8) If the power supplies are not on the same PC board with the MC10318, bypass V_{EE} and V_{TT} to Ground with (minimum) 10 μF and 0.1 μF where the supply voltages enter the PC board;
9) Use of a ground plane is mandatory in all high speed applications;
10) Keep all TTL circuitry tracks separate from the MC10318 by means of ground tracks and/or ground planes.

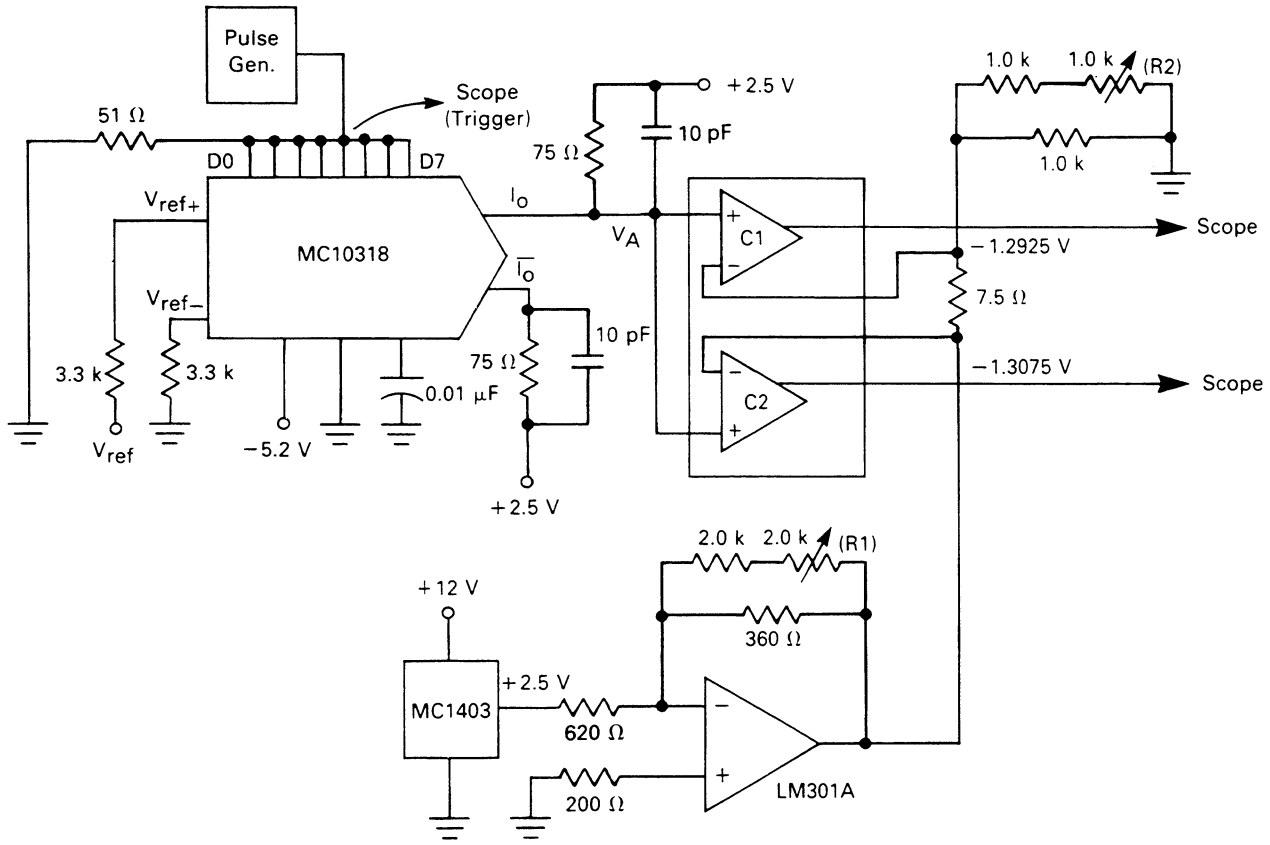
Many of the above points have to do with isolating the device from all other circuitry, since most applications involve using the MC10318 (which is 50% analog) in a (noisy) digital circuit. If the output voltage swing is typically 1 volt, then 1 LSB is approximately 4 mV. Since TTL circuitry can easily generate 50 mV noise on the ground line, the need for isolation is apparent.

The above points are not the only ones to be considered by the designer, as each application will have its own individual additional requirements.

Propagation Delay

The propagation delay is measured from the 50% point of the input transition to the 50% point of the output transition. Since the typical propagation delay is on the order of 5 ns, see Figure 21 and the information in Settling Time if this parameter is to be measured. Switching 1 LSB or all of the bits simultaneously produces no significant difference in propagation delay.

FIGURE 22 — SETTLING TIME MEASUREMENT



NOTES:
1) Pulse generator outputs −0.9 V to −1.8 V, t_r and $t_f \approx 2$ ns.
2) Adjust V_{ref} for full scale output at $V_A = -1.3000$ V.
3) Adjust R1 for −1.3075 V at input of lower comparator.
4) Adjust R2 for −1.2925 V at input of upper comparator.
5) R1, R2 are 20 turn trimpots.
6) Keep all wiring as short, tidy as possible — isolate all digital and analog supplies, grounds, signal lines, etc.
7) Heavily bypass all supplies at each device, and reference (−) inputs to the comparators.
8) Comparators are high-speed devices, such as AM687ADL.
9) Account for comparator offset when setting reference values.

Settling Time

The settling time is defined as the time from the 50% point of the input transition to the point at which the output enters into **and** stays within ± ½LSB (the error band) of the final value. Minimum settling time occurs when the output enters the error band at the maximum slew rate. and then settles out within the band. In actuality, however, the output's slew rate will lessen prior to entering the error band, and then may exit and enter the band once or twice as it settles to its final value. The settling time is determined by the last time the output enters the error band. See Figure 1.

When testing for settling time, the measurement technique used will have an effect on the result. Simply connecting scope probes to an input and output is generally not satisfactory due to the capacitive loading (typically 10–20 pF) of the probes. The rise (fall) time of an ECL input can be significantly increased by such a probe, with the result that the inputs of the MC10318 may be skewed from each other, which, in turn, affects the output. However, probes with low input capacitance, on the order of 2 pF or less (such as FET probes), can be used with very little degradation of the waveforms. The overall propagation delay of the probe (from tip to scope input) must be taken into account, as this can be on the order of 10 ns.

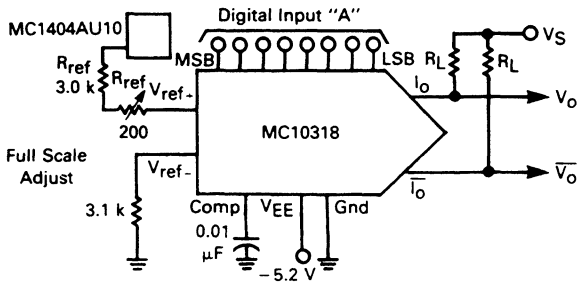
When attempting to view the output on a scope, several factors need to be considered. If the output swing is a full scale transition (e.g., 1.0 V), 1 LSB is 3.9 mV. The scope's amplifier must then be set at a sensitive range (5 mV/cm or 10 mV/cm), with the result that the scope's amplifier will be saturated when the MC10318's output is at the initial value. When the device inputs are switched, the output approaches the final value, but the scope's amplifier will require some time to come out of saturation, and then may overshoot, causing a false indication. In order to overcome this problem, the MC10318 was tested for settling time by connecting the output to a dual high-speed comparator configured as a window detector. The window is 1 LSB wide, centered about the final value. The outputs of the comparators are then monitored on a scope, as they indicate when the MC10318 output is settled within the error band. Propagation delays of the comparators, scope probes, and cable lengths are taken into account. See Figure 22. This method of monitoring the DAC's output, although indirect, does not cause changes to the output waveform because of probe loading, characteristics of the scope, or noise which the probe (and cable) may pick up.

APPLICATIONS

Voltage Output

There are two methods of converting the current output of the MC10318 to voltage outputs, depending on the voltage swing desired. For a limited range (<3.8 V p-p) the circuit of Figure 23 can be used.

FIGURE 23 — VOLTAGE OUTPUT

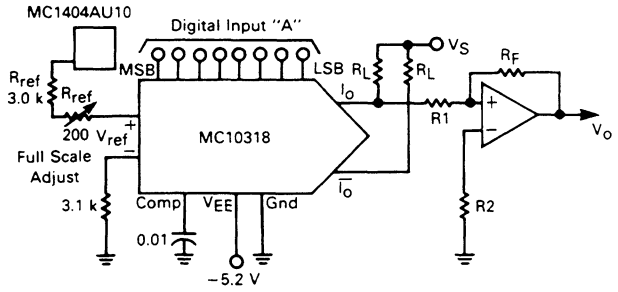


V_S	R_L	V_o	$\overline{V_o}$
0 V	25.5	0 to −1.3 V	−1.3 V to 0 V
+2.5	49	+2.5 to 0 V	0 to +2.5 V
+2.5	74.5	+2.5 to −1.3 V	−1.3 to +2.5 V
+1.0	39	+1.0 to −1.0 V	−1.0 to +1.0 V

$$V_o = -\frac{V_{ref} \times A \times R_L}{R_{ref} \times 16} + V_S$$

Where a larger voltage swing is required, an op amp is required at the output. The choice of op amp will be based on whether accuracy or speed is of primary importance. Where repeatable and stable accuracy is required, the op amp characteristics to consider are open-loop gain, offset voltage, bias current, and temperature drift. Where speed is paramount, a wideband amplifier should be used. Slew rate, propagation delay, and settling time of the op amp are the primary factors to evaluate. The PC board should be designed for high frequency operation, possibly using Microstrip or Stripline techniques. See Figure 24 for a suggested circuit.

FIGURE 24 — VOLTAGE OUTPUT



R_{ref}	R_L	V_S	R1	R_F	V_o
3125	20	0	1.0 k	5.0 k	0 to +5
3125	20	0	1.0 k	10 k	0 to +10
3125	40	+1.02	2.0 k	10 k	−5 to +5
3125	40	+1.02	2.0 k	20 k	−10 to +10

$$V_o = \frac{V_{ref} \cdot A \cdot R_L \cdot R_F}{R_{ref} \cdot 16 \cdot (R1 + R_L)} \quad \frac{V_S \cdot R_F}{(R1 + R_L)}$$

Connecting I_o and $\overline{I_o}$ as shown in the above figures places a constant dc load (51 mA) on the V_S supply, thus facilitating its design. The Gain Adjust resistor should be a 20 turn trimpot, as this will result in one turn equaling approximately 1 LSB of adjustment (for the recommended values in the figure). All of the resistors should have similar temperature coefficients for best temperature stability.

WAVEFORM GENERATION

FIGURE 25 — SAWTOOTH GENERATOR

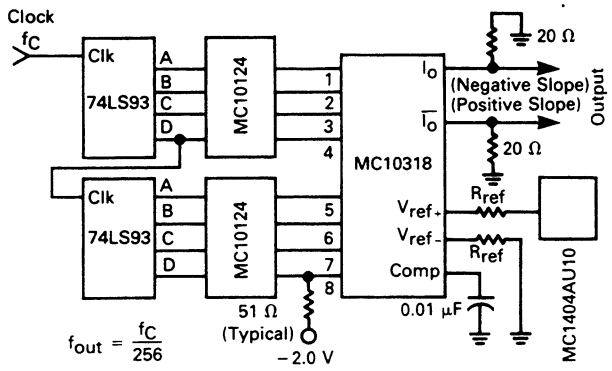


FIGURE 26 — TRIANGLE GENERATOR

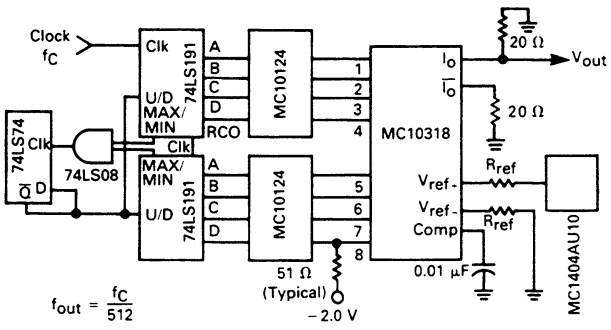
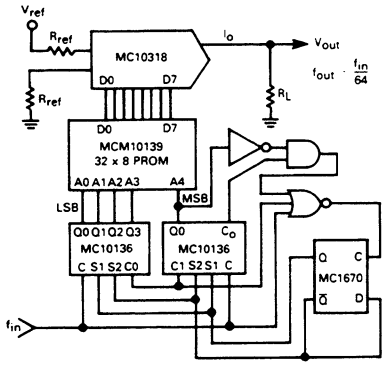
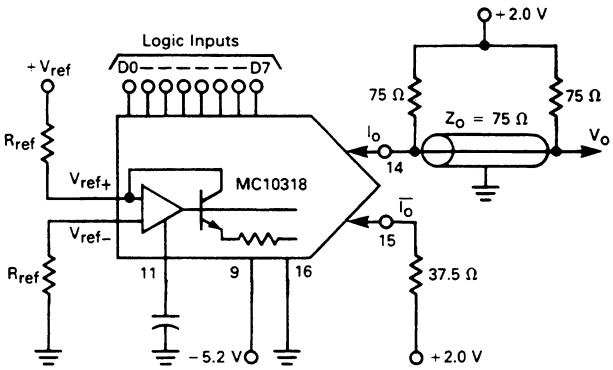


FIGURE 27 — SINEWAVE GENERATOR



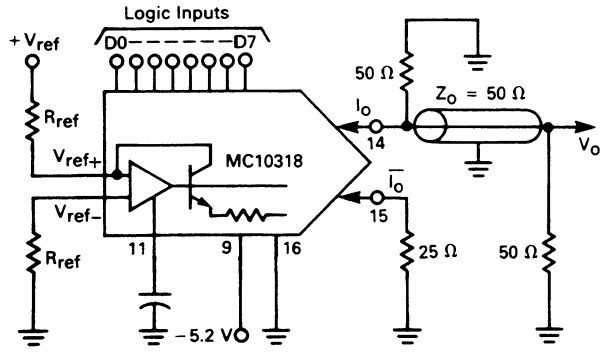
PROM CONTENTS			
Address	Output	Address	Output
00	00	10	80
01	01	11	8C
02	03	12	98
03	06	13	A4
04	0A	14	B0
05	0F	15	BC
06	15	16	C6
07	1D	17	D0
08	25	18	DA
09	2F	19	E2
0A	39	1A	E9
0B	44	1B	F1
0C	4F	1C	F6
0D	5B	1D	FA
0E	67	1E	FD
0F	73	1F	FE

FIGURE 28 — OUTPUT CONNECTED TO 75 Ω LINE



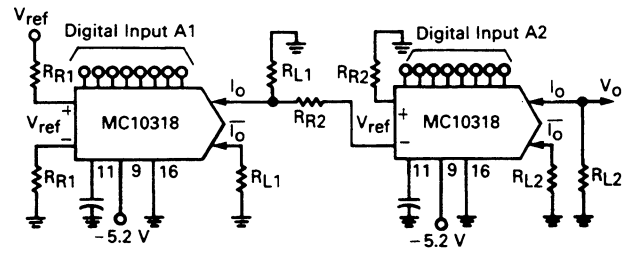
NOTE: Terminating Resistors and Z_O must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 29 — OUTPUT CONNECTED TO 50 Ω LINE



NOTE: Terminating Resistors and Z_O must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 30 — DIGITAL MULTIPLICATION



Suggested Values	
V_{ref}	+10 V
R_{R1}	3079*
R_{L1}	20
R_{R2}	330
R_{L2}	20

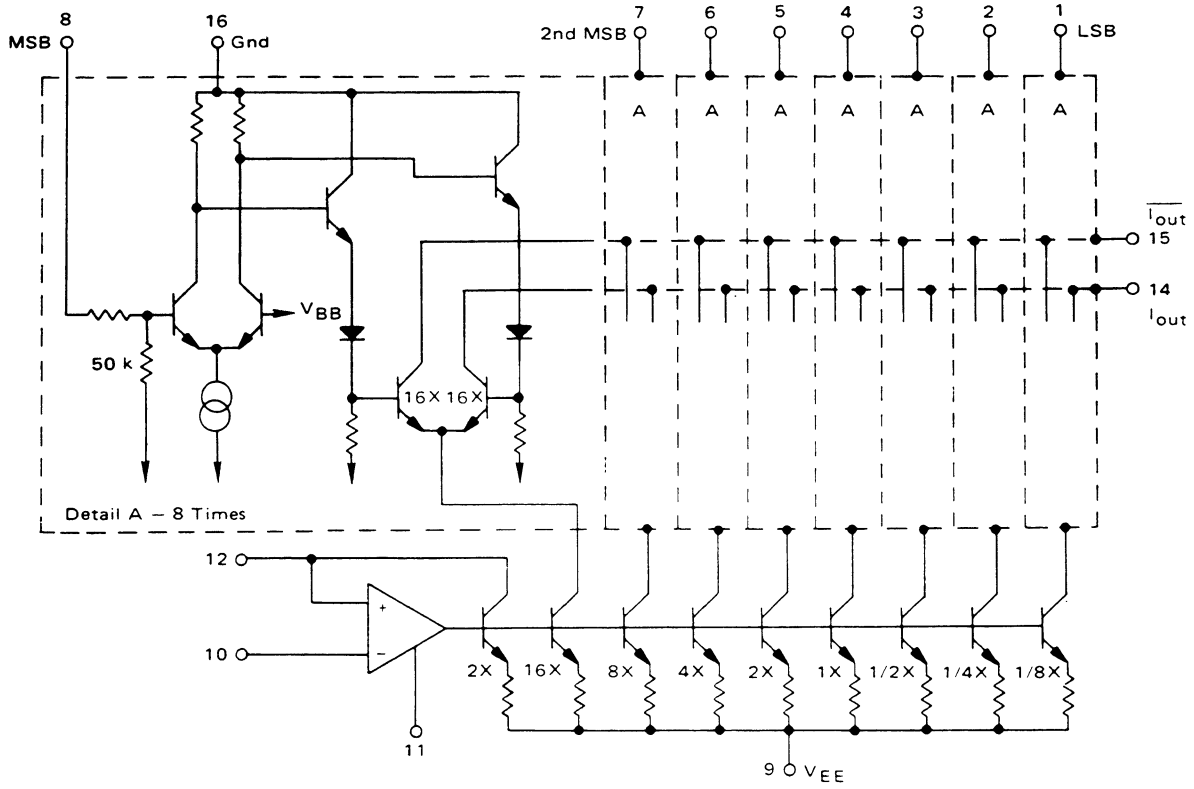
$$V_O = -\frac{A1 \times A2 \times V_{ref} \times R_{L1} \times R_{L2}}{R_{R1} \times R_{R2} \times 256} = -K \times A1 \times A2$$

(With suggested values, V_O range is 0 to −1.0 V)

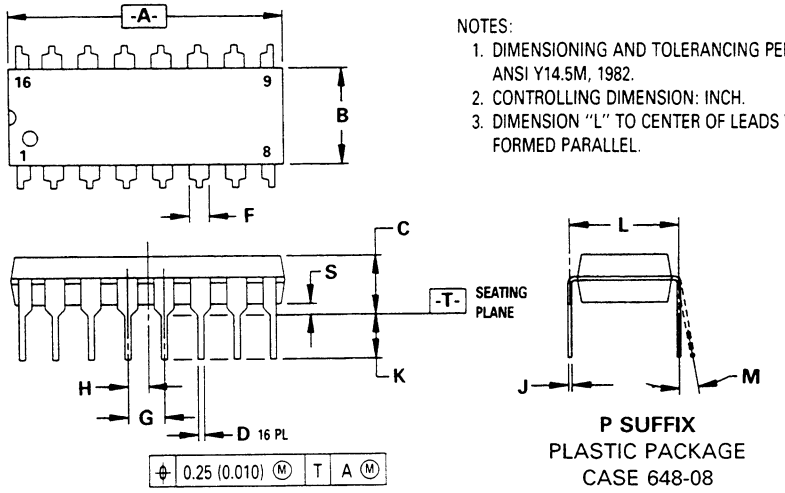
* 3.0 k Resistor + 100 Ω Trimpot

NOTES:
1) When generating waveforms at low frequencies, filtering the output is recommended to smooth out the steps.
2) In many applications, bipolar voltage output may be obtained by monitoring the differential voltage at Pins 14 and 15 (with equal load resistors).
3) When connecting the outputs to transmission lines (See Figures 28 and 29), proper transmission line theory and techniques must be used for optimum performance.

FIGURE 31 — MC10318 EQUIVALENT CIRCUIT



OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

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